T3 AND R3 TELEVISION TERMINALS FOR L3 CARRIER SYSTEM

CONTENTS

1. GENERAL

1.01 This section describes the T3 transmitting and R3 receiving terminal equipment used at the circuit ends of an L3 coaxial cable system for the transmission of television signals. The quality of transmission is such that three pairs of terminals can be satisfactorily operated in tandem. Maintenance procedures for these terminals are given in Section 359-090-500.

1.02 This section is reissued to include additional information, and also to bring the information covered in Issue 2 up-to-date with the system currently in use. Since this reissue covers a general revision, arrows ordinarily used to indicate changes have been omitted.

1.03 The overall L3 carrier system is described in Section 359-010-100. For purposes of discussion, however, the frequency allocations of the telephone and television bands of the L3 system are given in this section. (See Fig. 1.) A guard band in which no signals are transmitted separates the television band from the telephone band. This dead space provides adequate margin for the filters at television and telephone terminal dropoff points to effectively separate the two bands and prevent the interference that each band would otherwise produce in the other. As shown in Fig. 1, the L3 pilot frequencies and the television carrier frequency are indicated by arrow markers. Fig. 2 is a block diagram of a typical connecting arrangement of L3 coaxial cable facilities employing T3 and R3 television terminals.

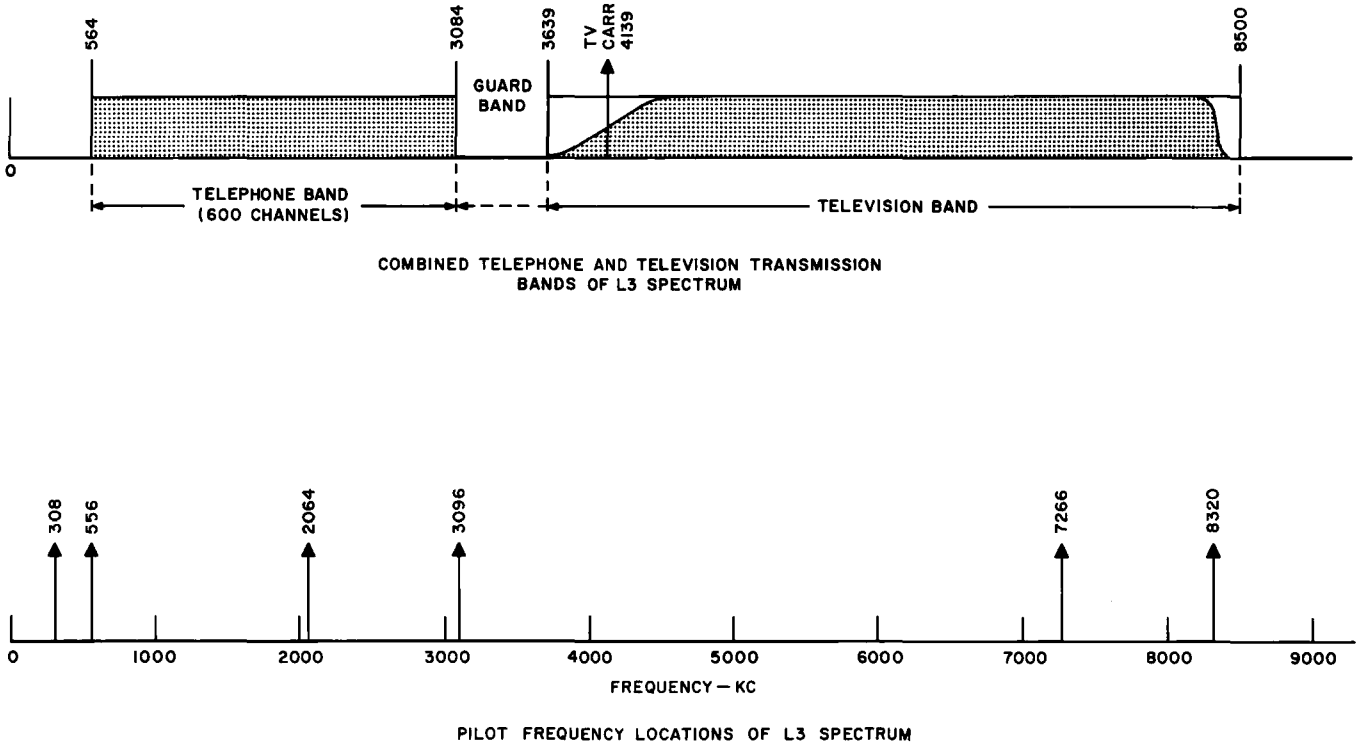


Fig. 1 — Frequency Allocations for L3 Carrier System

2. TRANSMISSION CONSIDERATIONS

A. Modulation and Demodulation

2.01 The primary function of the T3 transmitting terminal is to translate a video signal in the 0- to 4.2-mc range to the frequency spectrum allocated to television for transmission over the L3 coaxial cable system. The R3 receiving terminal accepts the output from the coaxial cable system and demodulates it to recover the original video signal.

2.02 The manner in which transmission of television signals is accomplished is shown in Fig. 3. A video signal is supplied to the modulator through a low-pass filter which limits the highest video frequencies to about 4.2 mc.

2.03 The modulator is also supplied with a 4.139-mc carrier which, when modulated by the video signal, produces a sideband on each side of the carrier frequency. The upper sideband extends from 4.139 mc to approximately 8.34 mc and the lower sideband extends from 4.139 mc to the zero-frequency axis. A "foldover" effect occurs at the zero-frequency axis for video frequencies that are higher than the 4.139-mc carrier frequency. This foldover is of no consequence because most of the lower sideband is rejected during a later step in the process.

2.04 Certain other products are generated during modulation which, if not suppressed, would fall back into the desired upper sideband and cause visible picture distortion. These products occur when the video signal modulates the third harmonic of the carrier frequency to also produce sidebands. At the higher video frequencies, the lower sideband of the carrier-frequency third harmonic overlaps the upper sideband of the carrier fundamental. Provision is made in the modulator for suppressing these undesired products. Sidebands of the second harmonic of the carrier can also cause picture distortion, but these undesired products tend to be suppressed by modulator balance.

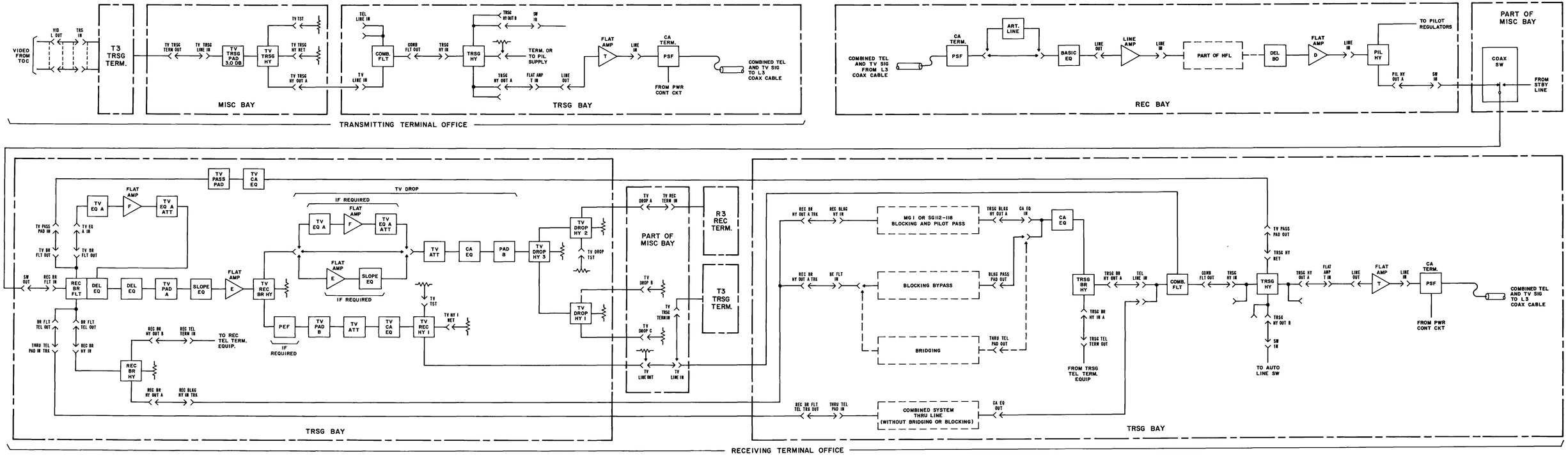


Fig. 2 — Typical Connecting Arrangement of Television Terminals

2.05 Since the energy contained in either of the two principle sidebands completely defines the video signal, most of the lower sideband is rejected in order to conserve space in the overall band of frequencies provided by the L3 coaxial cable system. Thus, by utilizing a carrier of 4.139 mc, the modulator achieves in one step the required frequency translation for placing the upper sideband and a portion of the lower sideband within the band allocated for television transmission.

2.06 Since most of the energy contained in the video signal occurs in relatively low-frequency components, it is essential that the sideband frequencies in the vicinity of the carrier are transmitted. A filter which passes one sideband without attenuation while completely rejecting the other is neither feasible in design nor practical in application. Excessive phase distortion would result from the use of a filter that exhibits a sharp cutoff characteristic. Instead, a filter with a gradual cutoff which is symmetrical about the carrier is used. The symmetrical response function is essential to recovery of the original modulating signal.

2.07 The vestigial filter following the modulator provides the necessary band shaping by completely suppressing the lower sideband except for the frequency components that are within 500 kc of the television carrier frequency. These frequencies are only partly suppressed, as are the corresponding frequencies in the upper sideband. The bandwidth of the signal at the output of the vestigial filter ranges from about 3.64 mc to about 8.34 mc, and is essentially the bandwidth of the signal transmitted over the high-frequency line. The symmetrical response function of the vestigial filter makes possible (during demodulation) a voltage addition equal to unity of corresponding frequency components on each side of the carrier frequency. If the cutoff characteristic were not symmetrical, the detected signal would not be flat over the video band of frequencies.

2.08 The receiving terminal accepts this signal and demodulates it, utilizing a locally generated carrier of 4.139 mc. The demodulator output consists of two sidebands, the upper sideband extending from about 8 to about 12.5 mc and the lower sideband extending from virtually dc to

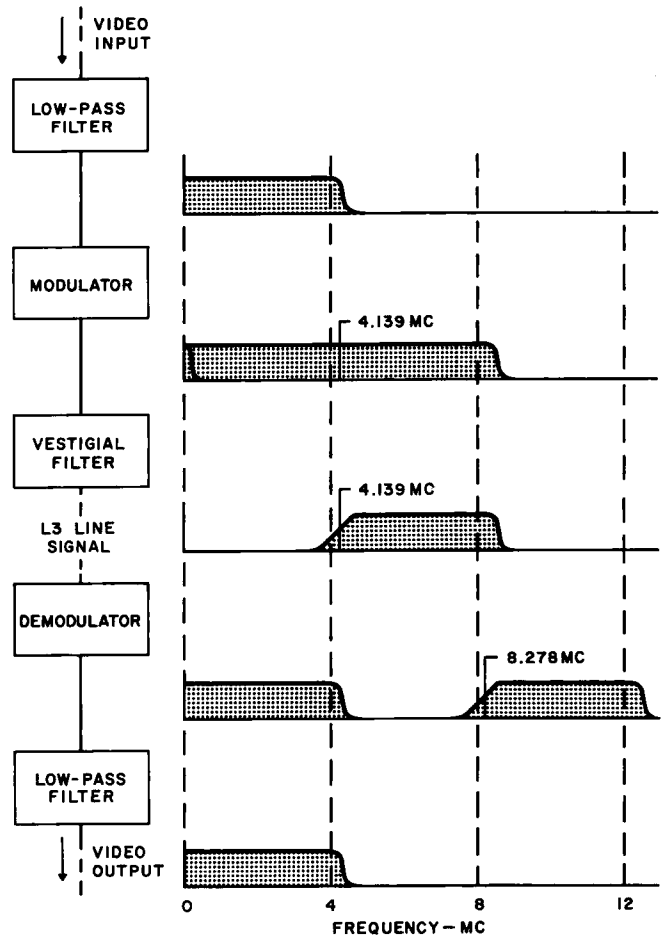


Fig. 3 — Frequency Translations for T3 Transmitting and R3 Receiving Television Terminals

4.2 mc. Voltage addition of the energy in the vestigial and upper sidebands received over the high-frequency line occurs during the demodulation process in such a manner that the lower sideband of the output of the demodulator is a replica of the original video signal.

2.09 The upper sideband is rejected by a low-pass filter following the demodulator while the energy in the lower sideband is accepted. The lower sideband is the desired video output signal.

B. The Modulation Process

2.10 The modulator used in the transmitting terminal is of the basic double-balanced lattice-type illustrated in Fig. 4. As shown in the figure, the modulator consists of four varistors

arranged to produce a double-sideband output signal when supplied with high-amplitude carrier and low-amplitude video input signals. Because it is double-balanced, neither the carrier nor the video signal appears in the output.

2.11 Fig. 5 shows the manner in which the modulator functions for positive and negative excursions of the carrier signal. Electron flow is shown by the direction of the arrows. During the positive half of the carrier cycle, varistors 1 and 2 conduct to effectively short-circuit the carrier input transformer secondary while varistors 3 and 4 are open-circuited. During the negative half of the carrier cycle, varistors 3 and 4 conduct while 1 and 2 are open-circuited. Under idealized conditions, no carrier current flows in the output transformer primary winding. In effect, the high-amplitude carrier switches the pairs of varistors (1 and 2 or 3 and 4) between a conducting or nonconducting condition.

2.12 When both carrier and video signals are supplied to the modulator, electron flow is as shown in Fig. 6A through 6D. During the positive half of the carrier cycle, the impedance of varistors 1 and 2 is zero because of the carrier current flowing through them. If the video signal during this time is such that terminal A is positive with respect to terminal B (see Fig. 6A), the video signal current will flow from terminal B through the upper half of the output transformer primary winding and then divide equally between varistors 1 and 2. The currents then flow through the carrier input transformer secondary winding to terminal A. Since the video signal currents flowing in the carrier transformer secondary are in opposite directions, they cancel. The current flowing through the upper half of the output transformer primary, however, produces an output across the secondary winding. During the negative half of the carrier cycle, the video signal current flows through the lower half of the output transformer primary winding as shown in Fig. 6B. The reversal in the direction of video signal current in the output transformer occurs at the carrier rate regardless of the polarity of the video signal at terminals A and B. Fig. 6C and 6D show video signal currents through the modulator for positive and negative excursion of the carrier cycle when terminal A is negative

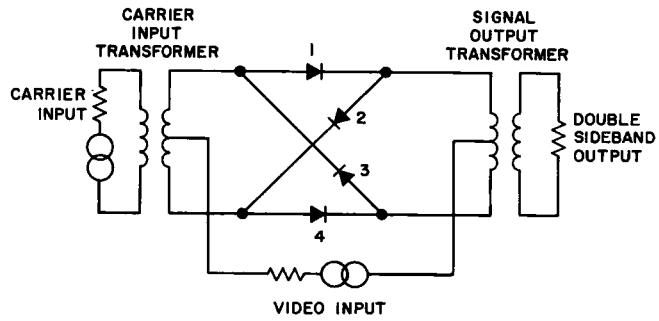


Fig. 4 — Basic Double-Balanced Lattice Modulator, Simplified Schematic Diagram

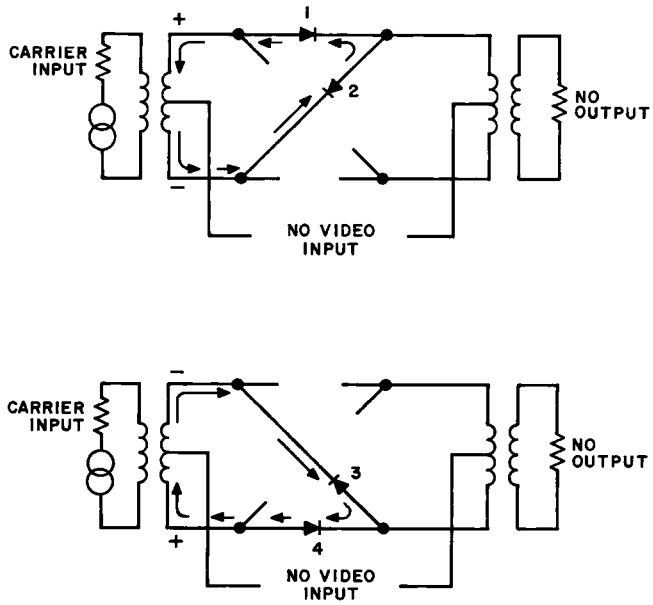


Fig. 5 — Electron Flow Through Varistors During Positive and Negative Halves of Carrier Cycle

with respect to terminal B. The current flowing in the primary winding of the output transformer induces a current in the secondary which flows first in one direction during one half of the carrier cycle, and then in the other direction during the other half. The modulator, therefore, functions as a reversing switch operating at the carrier frequency. The voltage appearing across the modulator output is a wave whose amplitude varies in proportion to the amplitude of the video signal.

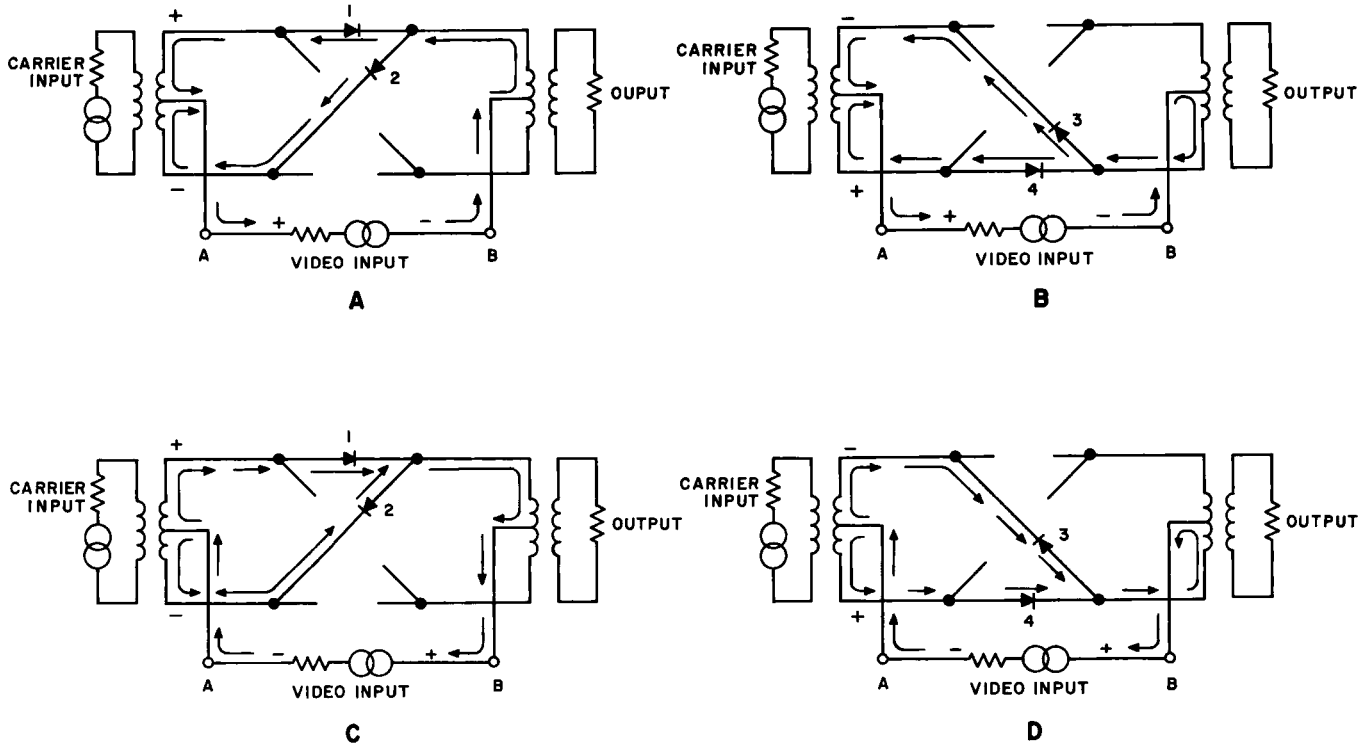


Fig.6 — Video Signal Electron Flow Through Varistors During Positive and Negative Halves of Carrier Cycle

2.13 Fig. 7 illustrates the output current from a perfectly balanced modulator for various levels of modulating voltage. A sine wave is used for purposes of illustration. Under conditions of perfect balance, the modulator produces no output at either the carrier frequency or the modulating frequency, but does produce an output corresponding to the sums and differences of the carrier and modulating frequencies. The sums correspond to the upper sideband, the differences correspond to the lower sideband, and the amplitude corresponds to the amplitude of the modulating voltage. Other products are also generated because the output current waveform approximates a square wave and therefore contains all odd harmonics of the carrier frequency and their associated sidebands. As shown in Fig. 7, the output current reverses direction whenever the modulating voltage crosses the zero axis.

2.14 Fig. 8 shows the modulator output for both low-level and high-level modulating signals superimposed on a dc voltage. In this case, carrier voltage is present in the output in proportion to the value of the dc voltage, and the sideband amplitude is in proportion to the values of the modulating voltage and dc voltage. A reversal in the direction of current does not occur until the modulating signal crosses the zero axis. One envelope of the modulated output waveform is shown emphasized to simplify identification of the modulating voltage.

2.15 One of the primary requirements for the transmission of television signals is optimum signal-to-noise performance. This requirement is met by transmitting a carrier having a constant amplitude during the synchronizing intervals of the video signal, and also during periods when no signal is transmitted. Transmission of carrier also makes possible phase synchronization of the locally generated carrier used for demodulation at the receiving terminal.

2.16 Transmission of energy at the carrier frequency is made possible by the carrier level control circuit in the transmitting terminal. This circuit samples the modulator output and derives

from the vertical synchronizing pulses a dc control voltage. This voltage varies as the peak amplitude of the carrier at the synchronizing intervals varies.

2.17 The dc control voltage is then fed back to the modulator in such a way that the video signal is superimposed on the dc. The peak carrier output from the modulator therefore remains constant at synchronizing intervals for all video signals ranging from a black picture (consisting of synchronizing pulses only) to maximum white.

2.18 During no-signal conditions, the circuit samples the modulator output continuously and develops a dc control voltage which maintains the carrier at the same amplitude as the amplitude at synchronizing intervals when a video signal is present.

C. Nature of the Modulated Signal

2.19 Fig. 9 illustrates the modulated carrier output signal for different video input signals. In the absence of an input signal, the carrier level control circuit unbalances the modulator

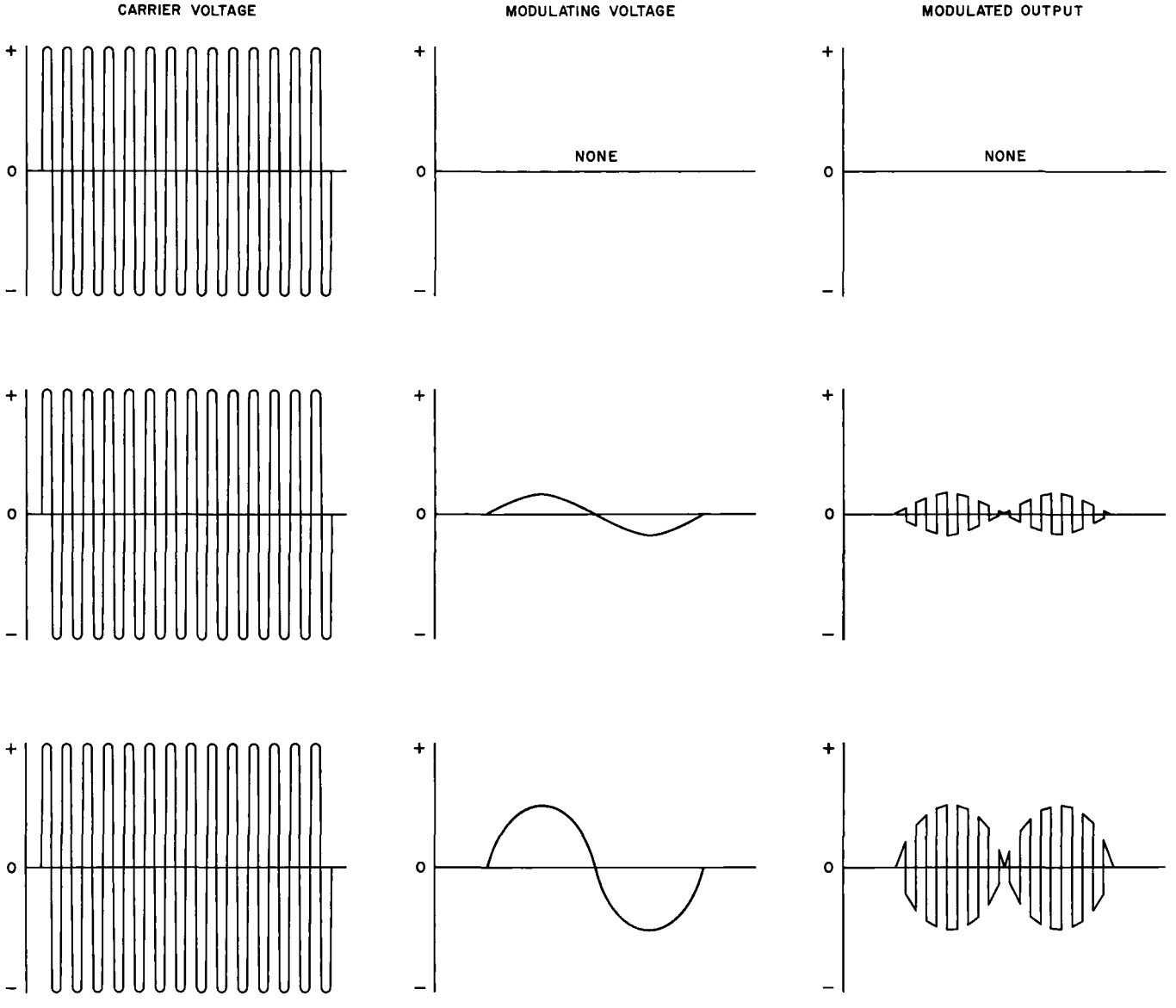


Fig. 7 — Typical Balanced Modulator Output for Various Levels of Input

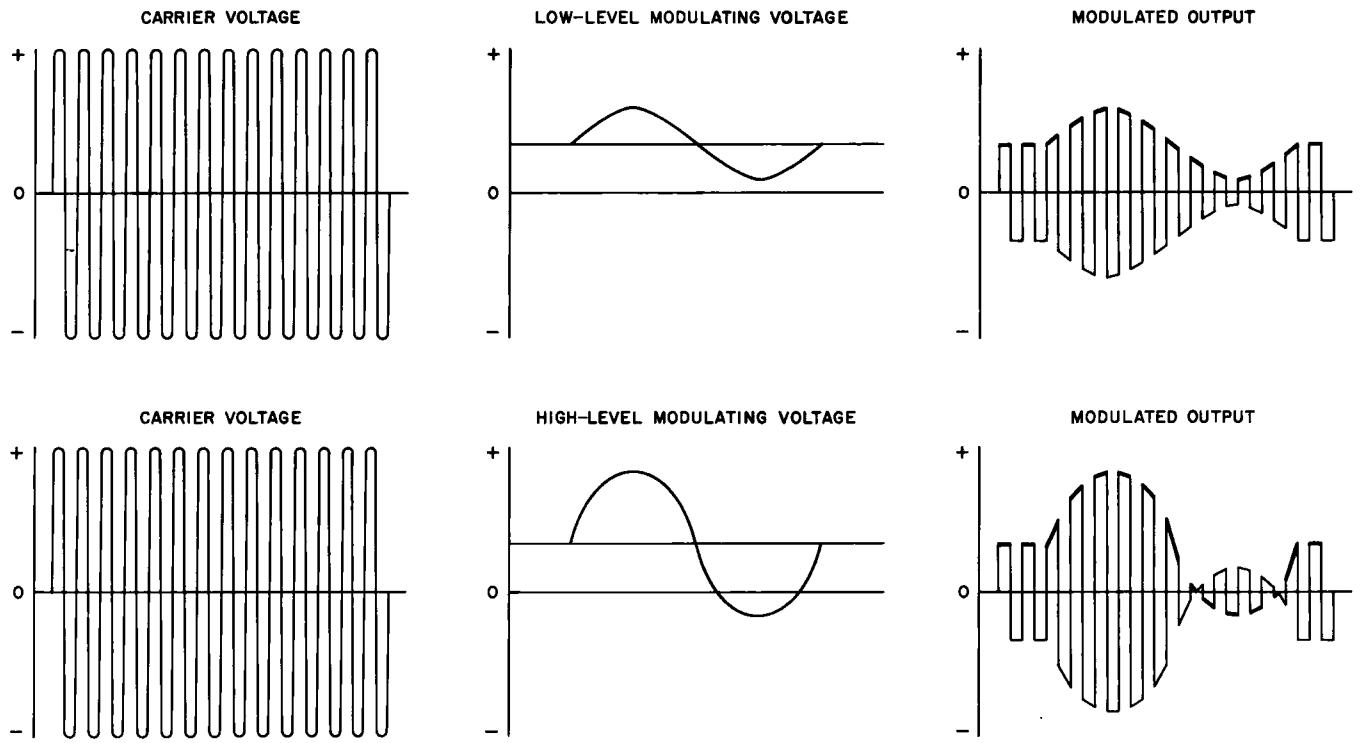


Fig. 8 — Typical Balanced Modulator Output for Various Levels of Input Superimposed on a DC Voltage

to produce a carrier having a constant amplitude as shown in Fig. 9A. When the input to the modulator is a negative-going synchronizing pulse, the output is as shown in Fig. 9B. The extreme of the sync tip corresponds to the no-signal condition (Fig. 9A) in which the modulator carrier output is maximum.

2.20 For the case of a low-amplitude video signal in which the maximum amplitude does not exceed a certain shade of grey, the corresponding modulator output is that of a 100 percent modulated carrier. This waveform is shown in Fig. 9C and is produced in the same manner as the low-level waveform of Fig. 8.

2.21 A full-amplitude video signal, having brightness gradations ranging from black to maximum white, produces the waveform shown in Fig. 9D and is produced in the same manner as the high-level waveform of Fig. 8. One envelope is shown emphasized to simplify identification of the video signal waveshape. The peak-to-peak amplitude at synchronizing intervals is the same as that shown in Fig. 9A, 9B, and 9C. Fig. 9E shows the waveform for a video signal having a peak-to-peak amplitude 3 db above normal. This waveform has a peak-to-peak amplitude between synchronizing intervals which exceeds the amplitude during the synchronizing interval. The waveforms of Fig. 9D and 9E produce a maximum ratio of information to peak carrier amplitude and are the optimum signals to transmit from a signal-to-noise standpoint.

2.22 Modulated signals of the form shown in Fig. 9B and 9C can be detected by rectification, i.e., envelope detection. However, rectification of the waveforms of Fig. 9D and 9E produces a spurious envelope in such a way that video signals exceeding the degree of modulation referred to as 100 percent appear inverted. It is therefore necessary to use a product demodulator (also called a homodyne detector) to recover the video signal. This type of demodulator functions similarly to the modulator. It is driven by a locally generated carrier which is synchronous in ***frequency*** and ***phase*** with the carrier component of the received signal.

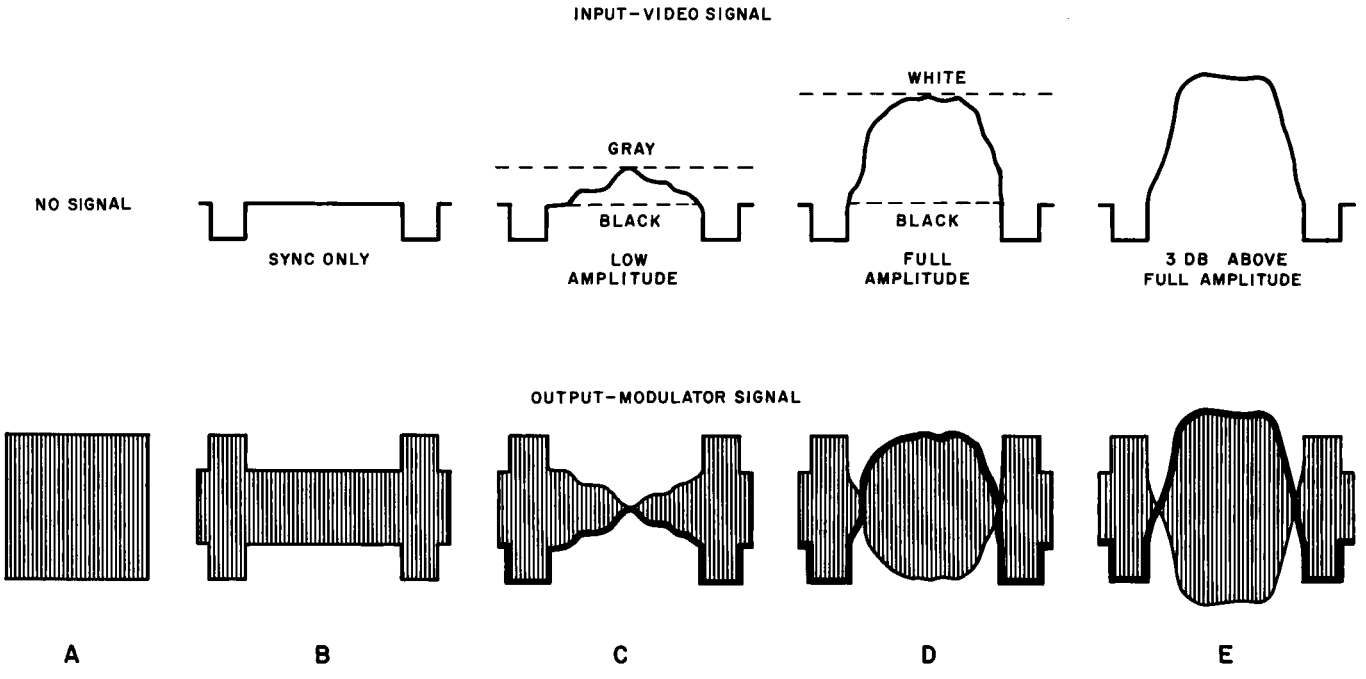


Fig. 9 — Nature of Modulated Signal

2.23 When the locally supplied carrier phase is correct, the homodyne detector is capable of perfectly demodulating without distortion a double sideband, single sideband, or vestigial sideband signal.

2.24 Excess carrier ratio is a term which is used to describe the degree of modulation employed in the transmission of television signals. It is equal to the peak carrier amplitude (measured during the synchronizing interval) divided by the sync tip-to-white amplitude of the modulating signal. An excess carrier ratio (ECR) of 1.0 corresponds to the degree of modulation referred to as 100 percent. Lesser degrees of modulation, for a given carrier amplitude, result in an ECR greater than 1.0 while a higher degree of modulation results in an ECR of less than 1.0. ECR can also be defined with reference to Fig. 10. Fig. 10A illustrates a window signal used as a video modulating signal. For purposes of discussion, its amplitude from sync tip to maximum white is considered to have a value of 1.0. This signal, when used to modulate a carrier having a peak amplitude of 1.2 during the sync interval, produces a waveform with an ECR equal to 1.2. The corresponding index of modulation is equal to 0.8 (80 percent modulation). Fig. 10B illustrates this waveform. By subtracting the 20 percent excess carrier, i.e., by reducing the peak carrier amplitude to 1.0 while maintaining the amplitude of the modulating signal constant, the ECR becomes 1.0 and the corresponding index of modulation becomes 1.0 (100 percent modulation). This waveform is shown in Fig. 10C. The reduction in carrier amplitude results in an improvement in signal-to-noise performance over the waveform of Fig. 10B even though its relative peak-to-peak amplitude is less. A further improvement in signal-to-noise performance is effected by a further reduction, or subtraction, of carrier. As shown in Fig. 10D, the peak amplitude of the modulated wave is half the amplitude of the modulating signal. The ECR in this case is 0.5 and the index of modulation is 2.0 (200 percent modulation). This waveform exhibits the same foldover effect as that of Fig. 9D, and occurs for all degrees of modulation which exceed 100 percent.

2.25 The waveform of Fig. 10D is repeated in Fig. 10E, but in this case the desired envelope waveshape is emphasized to illustrate the waveform produced after demodulation. As shown in the figure, the ***peak-to-peak*** amplitude of the modulated carrier is equal to that of the modulating signal. This particular ratio of carrier to

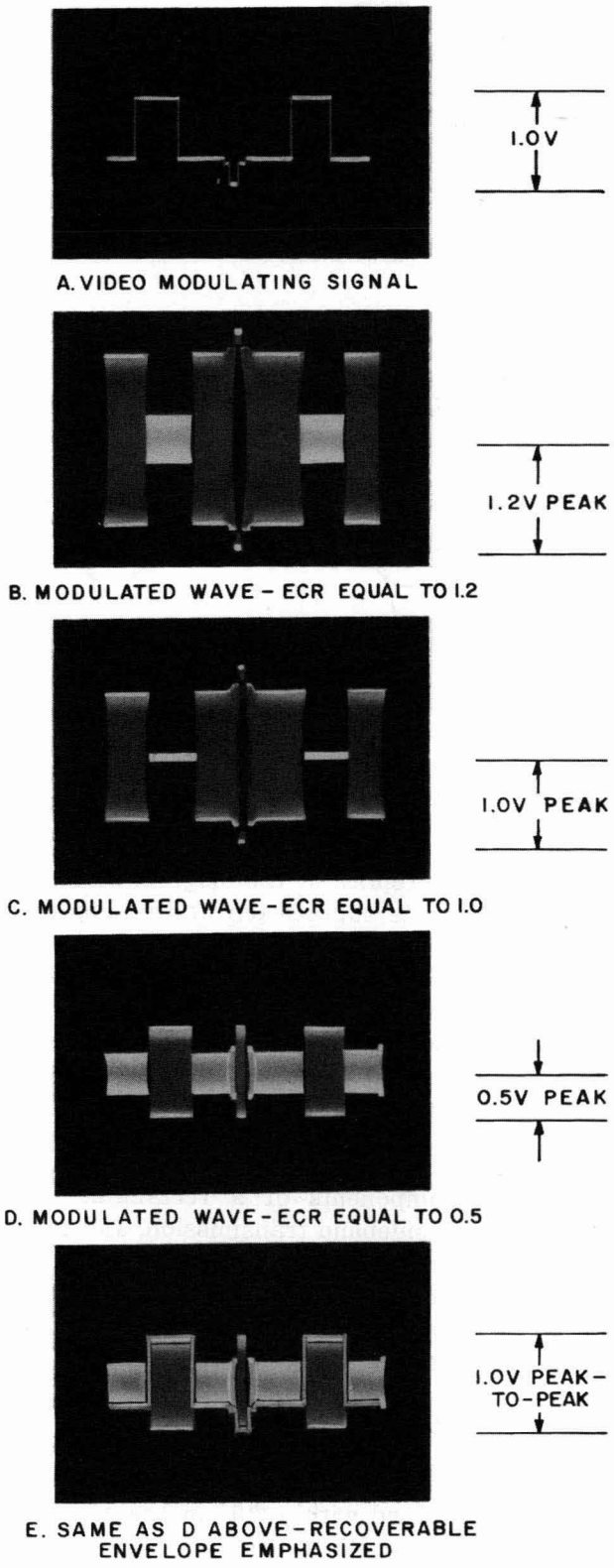


Fig. 10 — Carrier Waves Modulated by a Constant Amplitude Video Signal

modulating signal amplitude (0.5) is the least that can be employed while still preserving the original modulating signal waveshape. It is the optimum value from a signal-to-noise standpoint, since the transmitted wave contains a maximum ratio of information to carrier.

D. The Detection Process

2.26 As described in 2.06, a vestigial sideband signal has a symmetrical cutoff characteristic in the region of the carrier. The response function illustrated in Fig. 11A represents idealized conditions for vestigial sideband transmission. The main sideband extends from the carrier frequency F_C to the upper cutoff F_U. The vestige of the lower sideband extends from F_C to the lower cutoff F_L. At frequencies in the cutoff region $F_C \pm F_V$, the band shape is such that the two voltages at corresponding frequencies on each side of the carrier add to a constant value. This summing is accomplished by the demodulator and produces an output having a flat response over the video band of frequencies.

2.27 The response function of the vestigial filter can be considered to be the sum of the two response functions of Fig. 11B and 11C, which have even and odd symmetry, respectively, about

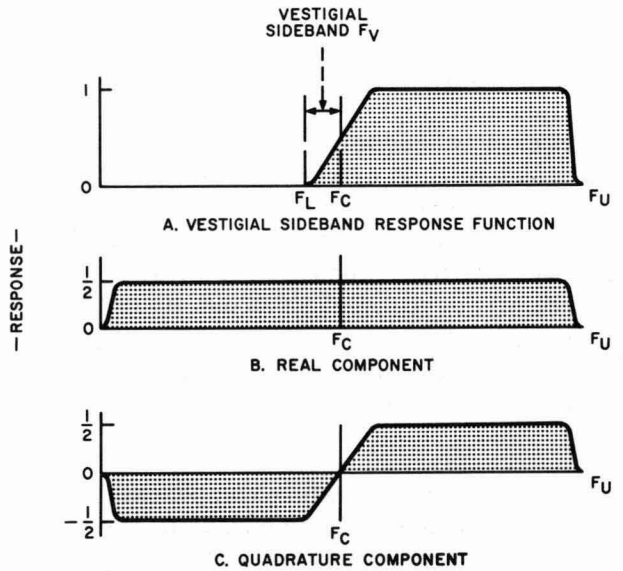


Fig. 11 — Response Functions, Vestigial Sideband Transmission

the carrier frequency F_C. The component of Fig. 11B represents the normal double-sideband output from the modulator and the component of Fig. 11C represents the output of the modulator supplied with signal and carrier voltages, each shifted in phase by 90°, and with the amplitude attenuated symmetrically in the region of the carrier. The output of a circuit having the response function of Fig. 11C is called the quadrature component and is a distortion term inherent in vestigial sideband transmission. It is related to the normal (or real) output depending on the shape of the vestigial sideband.

2.28 Homodyne detection makes possible the recovery of the real component while completely suppressing the quadrature component. For purposes of discussion, a complex wave consisting of three discrete frequencies is illustrated in Fig. 12A. Each frequency is of different amplitude and phase with respect to the others. The dashed line represents the sum of the ***sines*** of the three frequencies, multiplied by appropriate constants (depending on the maximum amplitude of each frequency). This wave, when used to modulate a carrier frequency having an amplitude of ***cos Ct*** (where C is carrier angular frequency and t is time), produces the ***real component*** at the output of the vestigial filter.

2.29 Fig. 12B illustrates the same three frequencies, each with the same amplitude as corresponding frequencies of Fig. 12A. In this case, however, the dashed line represents the sum of ***cosines*** of the three frequencies (each multiplied by appropriate constants). This wave, when used to modulate a carrier frequency having an amplitude of ***sin Ct,*** produces the ***quadrature component*** in the vestigial sideband signal. The effect is that signal and carrier voltages are each shifted in phase by 90°. The real component of the vestigial sideband signal is, therefore, a ***sine*** function of the modulating voltage which multiplies ***cos Ct*** and the quadrature component of a ***cosine*** function which multiplies ***sin Ct.***

2.30 Real and quadrature components also exist in the demodulator output in the same relationship. If the locally generated carrier is supplied to the demodulator exactly in phase with the real component of the vestigial sideband signal, the real component appears in the output as

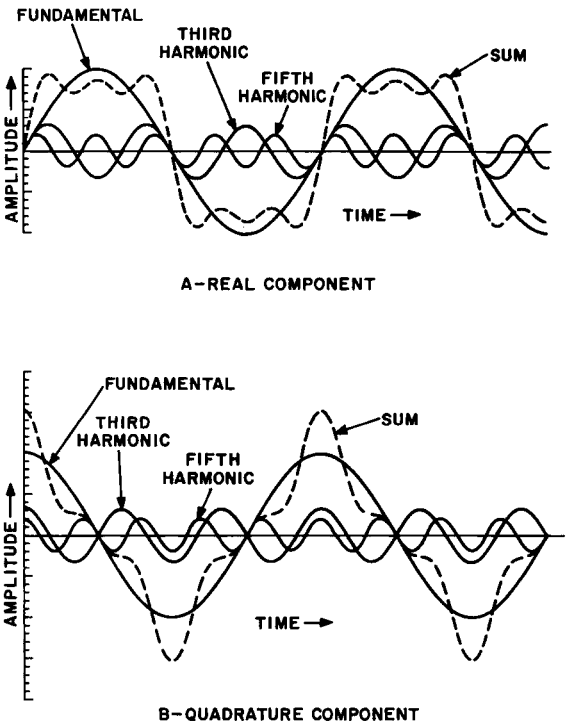


Fig. 12 — Real and Quadrature Components of Complex Wave

an undistorted replica of the original modulating voltage. Complete suppression of the quadrature component occurs when the phase difference between the modulating and demodulating carriers is 0°, since the quadrature component multiplied by sin 0° is zero. It is the inherent 90° shift of carrier and signal voltages in the quadrature component that makes possible the suppression.

2.31 Fig. 13A illustrates the real and quadrature components of a rectangular pulse after vestigial sideband transmission, and typically represents transmission of a composite video signal. Fig. 13B illustrates the waveform at the output of the demodulator when supplied with carrier having some phase error.

2.32 To suppress the quadrature component to barely perceptible values, it is necessary that the phase angle of the locally generated carrier be maintained within 2.5° of the modulating carrier frequency. When three pairs of terminals are operated in tandem, the demodulator in each of the three receiving terminals contributes to the overall quadrature distortion. To prevent the total

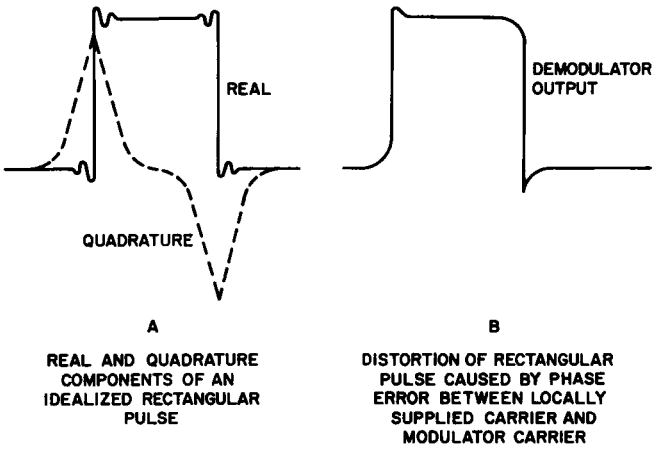


Fig. 13 — Idealized Rectangular Pulse Waveshapes, Vestigial Sideband Transmission

distortion for three pairs of terminals operated in tandem from exceeding threshold value, the phase angle of the locally generated carrier supplied each demodulator must be held to within 1.44° of the original modulating carrier frequency (derived by dividing 2.5° by the square root of 3).

2.33 Although the locally generated carrier is synchronous in phase and frequency with the carrier used for modulation, the overmodulated nature of the received signal makes the polarity of the video signal indeterminate. Thus, the 180° reversals that occur in polarity when the picture signal exceeds 100 percent modulation, i.e., changes from average black to average white, would (unless otherwise prevented) cause sudden video polarity reversals at the demodulator output. A squaring circuit is provided in the carrier frequency control circuit at the receiving terminal to convert the sudden 180° reversals into 360° changes. These changes are also indeterminate in an average-phase detector, and consequently, the phase-synchronized carrier supply will lock and remain stably locked to the average phase of the squared signal. No instantaneous reversals in polarity can occur.

2.34 The squaring operation, however, eliminates any basis for determining the original polarity of the video signal, and the locally generated carrier can lock to either polarity relative to the received signal. Consequently, the demodulator video output signal can be of either polarity, and either condition is equally possible. Reversals in polarity are most likely to occur during switching operations or occasions when different types of signals, such as sine waves or certain test signals, are applied.

2.35 A polarity reversing circuit (polarizer) is provided ahead of the output line connections at the receiving terminal. This circuit constantly monitors the polarity of the video output signal. Whenever the polarity changes, the polarizer circuit functions to correct it.

E. Pilot Suppression

2.36 Two of the L3 pilot frequencies (7266 kc and 8320 kc) fall in the L3 television band. It is essential that these frequencies are transmitted over the L3 system without interference from the television signal. However, these pilot frequencies, if not suppressed at the receiving terminal, will be demodulated down to 3127 kc and 4181 kc and appear as high-frequency bar patterns in the picture signal.

2.37 A 2-section filter unit, modified to provide only one section, is used at the transmitting terminal to remove from the television signal two very narrow bands of energy centered at the two pilot frequencies. An identical unit, also modified to provide only one section, is used at the receiving terminal to remove the two pilot frequencies from the received signal. At L3 terminal stations where transmitting and receiving terminals are connected in tandem, the pilot suppression filters are supplied in the L3 connecting equipment, and a pad replaces the pilot suppression unit in the receiving terminal.

3. GENERAL DESCRIPTION OF TERMINALS

A. General

3.01 The T3 and R3 television terminals are contained in separate bays, and each consists of transmission and associated power and alarm equipment. The transmission equipment for each of the terminals is shown in simplified block diagrams, Fig. 14 and 15.

3.02 Transmission levels shown in Fig. 14 and 15 are nominal values and are given in terms of dbv for the balanced 124-ohm video sections of the terminals and in dbm for the unbalanced 75-ohm carrier sections. Jacks, which are interconnected by patch plugs, and their designations are shown in the figures. Removal of a patch plug permits measurement of signal levels at various points in the transmission paths.

3.03 The levels are specified in dbv for full-amplitude video signals in the video sections of the terminals because the waveforms of television signals are dependent on picture content. For such signals, a 1.0-volt peak-to-peak video signal corresponds to 0 dbv. The levels shown are also useful during troubleshooting when using sine waves as test signals. For sine waves, a 0-dbv signal (1.0 volt peak-to-peak across 124 ohms) is equivalent to a 0-dbm signal (1.0 milliwatt across 124 ohms). The relationship is apparent since a sine wave of 1.0 milliwatt (mw) develops an rms, or effective, value of 0.353 volt across 124 ohms. This value corresponds to 0.5 volt peak (or 1.0 volt peak-to-peak). The nominal video input signal level to the transmitting terminal is —9.0 dbv (0.35 volt peak-to-peak) and, for a sine-wave input signal, is equal to —9.0 dbm (0.123 volt rms or 0.35 volt peak-to-peak). A transmission measuring set (37B TMS) can be used to measure sine-wave test signals in terms of dbv in the video sections of the two terminals provided that a 124- to 75-ohm repeat coil is used and allowance is made for loss in the repeat coil, and provided also that appropriate attenuation is used for signal levels which exceed 0 dbv (0 dbm on the 37B TMS).

3.04 The levels shown in the carrier sections of the transmitting terminal are for unmodulated carrier except where two numbers are given, for example, $\overline{-13 \mid -15}$ at the transmitting terminal output. In this case, the unmodulated carrier level, i.e., with no input applied, is represented by the first number and is —13 dbm. For a sine-wave input signal of —9 dbv (between 1 and 4 mc), the modulated output level is represented by the second number and is —15 dbm. The levels shown in the carrier sections of the receiving terminal are also for unmodulated carrier except where two numbers are given. As in the transmitting terminal, the second number represents the nominal power for a full-amplitude sideband signal. A 37B TMS can be used to measure transmission levels in the carrier sections of both terminals provided only sine-wave test signals are measured and appropriate attenuation is used ahead of the 37B TMS for signal levels which exceed 0 dbm. A 124- to 75-ohm repeat coil is not required since the 37B TMS is calibrated for use in 75-ohm circuits.

B. T3 Transmitting Terminal

3.05 The 0- to 4.3-mc video signal from the television operating center (TOC) is supplied over a 124-ohm balanced cable to the transmitting terminal input. (See Fig. 14.) An input low-pass filter (part of FLT 1) limits the bandwidth to about 4.2 mc. The filter output is then supplied via the clipper (CLPR) circuit to the video amplifier (VID AMPL).

3.06 The clipper circuit is a shunt device bridged across the 124-ohm balanced connection between the filter output and video amplifier input. This circuit limits the amplitude of the video signal to a certain maximum value and therefore limits the maximum amplitude of the picture portion of the transmitted television signal. Its function is to protect the telephone message channels in the L3 band from interference caused by high transmission levels in the L3 television band. Normal amplitude video signals are not affected by the clipper circuit.

3.07 The video amplifier raises the level of the signal, then supplies the signal to the modulator (MOD). The modulator is composed primarily of two sections (Mod 1 and Mod 2), one of which modulates the video signal (V) with a 4.139-mc carrier (C). The desired output from this section (Mod 1) is a double-sideband signal consisting of components which are the sums and differences of the carrier and video frequencies ($C \pm V$). Undesired products are also present, the most detrimental of which are the sums and differences of the carrier-frequency third harmonic and the video frequencies ($3C \pm V$). It is the function of the other section (Mod 2) to produce an output which cancels the undesired $3C \pm V$ components from the first. The second section modulates the video signal (V) with a 12.47-mc carrier ($3C$) to produce an output ($3C \pm V$). The outputs of the two sections are then combined in a hybrid coil within the modulator unit such that the $3C \pm V$ components cancel.

3.08 The 4.139-mc carrier is generated in the carrier supply (CARR SUP) circuit and supplied via the carrier hybrid (CARR HYB) to the first modulator section. Because the section acts as a reversing switch on alternate half-cycles of the carrier frequency, odd harmonics of the 4.139-mc carrier frequency are generated and are therefore present as a backup product in the carrier hybrid. The carrier hybrid couples this energy to the carrier harmonic supply (CARR HRM SUP) for synchronization purposes. The carrier harmonic supply has a free-running frequency of approximately 12.417 mc and will stably lock to the third harmonic of the 4.139-mc carrier. The output of the carrier harmonic supply ($3C$) is fed to the second section of the modulator which produces the $3C \pm V$ output.

3.09 The 4.139-mc carrier from the carrier supply circuit is also supplied, via the carrier hybrid, to the carrier level control (CARR LEV CONT) circuit. This circuit continuously samples the output from the modulator and combines the sample with the 4.139-mc signal from the carrier supply circuit. The modulator output and the 4.139-mc carrier are added in phase, which results in a modulated wave having an amplitude substantially less than 100 percent. The carrier level control circuit derives a dc voltage from this wave at synchronizing intervals and feeds it back to the modulator through the video amplifier. As the amplitude at synchronizing intervals varies, the dc voltage varies proportionately and a constant peak-to-peak carrier amplitude is maintained.

3.10 The double-sideband output of the modulator, from which the carrier level control circuit derives its modulated input, is fed to the vestigial (VESTL) filter (part of FLT 1). This filter shapes the double-sideband signal into the 3.6- to 8.3-mc (approximately) vestigial transmission band. A pilot elimination filter (PEF), following the vestigial filter, removes two narrow bands of energy centered at 7266 kc and 8320 kc. The removal of energy is necessary to prevent the transmitted television signal from causing interference at the two line pilot frequencies in the L3 television band.

3.11 The signal at the output of the pilot elimination filter is supplied through a variable attenuator (AT2) to the high-frequency amplifier (HF AMPL 1). The attenuator provides a means for adjusting the signal level at the input to the amplifier over a range of 5 db in 0.5-db steps. The amplifier provides a flat gain of 34 db with a flat gain adjustment of ±1 db in 0.2-db steps to allow minor level adjustments.

3.12 The amplifier output is supplied through three variable mop-up equalizers (EQ2, EQ3, and EQ4), a fixed mop-up equalizer (EQ5), and a fixed pad (AT1) to the transmitting terminal output jack (TRS OUT) on the jack panel. The equalizers compensate for residual variations in the frequency characteristic of the terminal. The 4-db pad (AT1) provides effective isolation, when testing, between the fixed equalizer (EQ5) and the TRS OUT jack.

3.13 A patch plug connects the TRS OUT jack to the HF L EQ IN jack, which in turn feeds the signal to a cable equalizer (EQ6). The cable equalizer output is then supplied over a 75-ohm unbalanced connecting cable to the transmitting hybrid in the miscellaneous bay. The equalizer is strap adjusted, depending on the length of the connecting cable, and ensures a flat transmission characteristic at the output of the transmitting hybrid.

C. R3 Receiving Terminal

3.14 The television signal (3.6 to 8.3 mc, approximately) received over the L3 coaxial cable system is supplied from the high-frequency line connecting circuits in the miscellaneous bay through a 75-ohm unbalanced connecting cable to the receiving terminal input. (See Fig. 15.) A cable equalizer (EQ5) in the receiving terminal, which is strap adjusted depending on the length of the connecting cable, ensures a flat transmission characteristic. The equalizer output is then supplied to the high-frequency amplifier (HF AMPL 1).

3.15 The high-frequency amplifier provides a flat gain of 34 db with a flat gain adjustment of ±1 db in 0.2-db steps. The amplified signal is then fed to variable and fixed mop-up equalizers (EQ2 and EQ3, respectively). The equalizers compensate for deviations in the overall transmission characteristic. The output of variable equalizer EQ3 is supplied through a fixed pad (AT1) to the variable attenuator (AT3), which permits an adjustment in signal level of 5 db in 0.5-db steps.

3.16 A pilot elimination filter (PEF) following the variable attenuator suppresses the 7266- and 8320-kc line pilots to prevent them from being demodulated down to the video band and appearing as high-frequency bar patterns in the demodulated signal. At L3 terminal stations the pilot elimination filter is provided in the L3 connecting equipment and a pad (AT5) is provided in the receiving terminal.

3.17 The signal at the output of the pilot elimination filter, or pad, is again amplified in order to raise the signal to a level sufficient to drive the demodulator (DEMOD). The amplifier (HF AMPL 2) is identical to HF AMPL 1. Its output is fed to a hybrid coil (SIG HYB) which divides the signal energy: half to the demodulator and half through a jack arrangement and a low-pass filter (FLT 1) to the carrier frequency control (CARR FREQ CONT) circuit.

3.18 The jack arrangement is located on the branching and control panel, and is provided to facilitate tests and adjustments. Patch plugs are used to interconnect certain pairs designated TST 1, OPR, and TST 2. In normal operation, the jack arrangement is patched for the OPR condition. (See Fig. 15.)

3.19 A 4.139-mc carrier signal, which is generated in the carrier supply (CARR SUP) circuit, is also supplied to the carrier frequency control circuit. This signal is fed from the carrier supply through the carrier hybrid (CARR HYB), and the attenuator and phase shift network (AT4). The carrier frequency control circuit derives from the two input signals a dc voltage which is proportional to the instantaneous phase difference between the incoming carrier frequency and the locally generated 4.139-mc carrier. The dc voltage is fed back to the carrier supply circuit to reduce to a minimum the phase difference between the two carriers. It is essential that the phase difference between the locally generated carrier and the incoming carrier is maintained as nearly as possible to 0° in order that a distortionless video signal is obtained at the output of the demodulator.

3.20 The demodulator circuit is composed of two sections (Demod 1 and Demod 2), one of which demodulates the received television signal (supplied through the signal hybrid) with the 4.139-mc carrier generated in the carrier supply circuit. As in the modulator in the transmitting terminal, this section (Demod 1) produces upper and lower sidebands. The upper sideband extends from about 8 to about 12.5 mc and the lower sideband, which is the principle band of interest, extends from virtually dc to about 4.2 mc. Undesired sidebands are also generated which, if not suppressed, will cause interference products to fall back into the desired video output band. The greatest amount of interference is produced when the received signal (3.6 to 8.3 mc, approximately) is demodulated by the carrier frequency third harmonic (12.417 mc). This unwanted sideband (8.8 to 4.1 mc, approximately) slightly overlaps the desired lower sideband (0 to 4.2 mc) of the fundamental carrier frequency. The result is a bar pattern which occurs at high video frequencies. It is the function of the second section (Demod 2) in the demodulator unit to produce an output for cancelling the undesired products of the first. This is accomplished in the same manner as in Mod 2 of the transmitting terminal. A 12.417-mc signal is generated in the carrier harmonic supply (CARR HRM SUP) circuit and fed through the carrier hybrid to Demod 2. Output from this section is then combined with the output of Demod 1 in a resistance hybrid within the demodulator unit. The Mod 2 output cancels the undesired products present in the Mod 1 output so that the wanted sideband (0 to 4.2 mc) appears undistorted.

3.21 The carrier supression filter (CSF) following the demodulator rejects the upper sideband and passes the lower sideband to the video amplifier (VID AMPL). The signal is amplified, then supplied to the polarizer (POL) circuit. The video line connections between the input and output of the polarizer are made through contacts of a polarity reversing relay within the unit. Polarity recognition circuits, which are bridged across the output side of the video line, monitor the polarity of the signal. Whenever the video signal becomes inverted, the polarity reversing relay functions automatically to interchange the output connections so that the correct polarity is maintained. The signal is then fed to the television operating center through jacks on the jack panel. The jacks (REC OUT and VID L IN) are interconnected, as are other jacks in the terminal, by means of a patch plug.

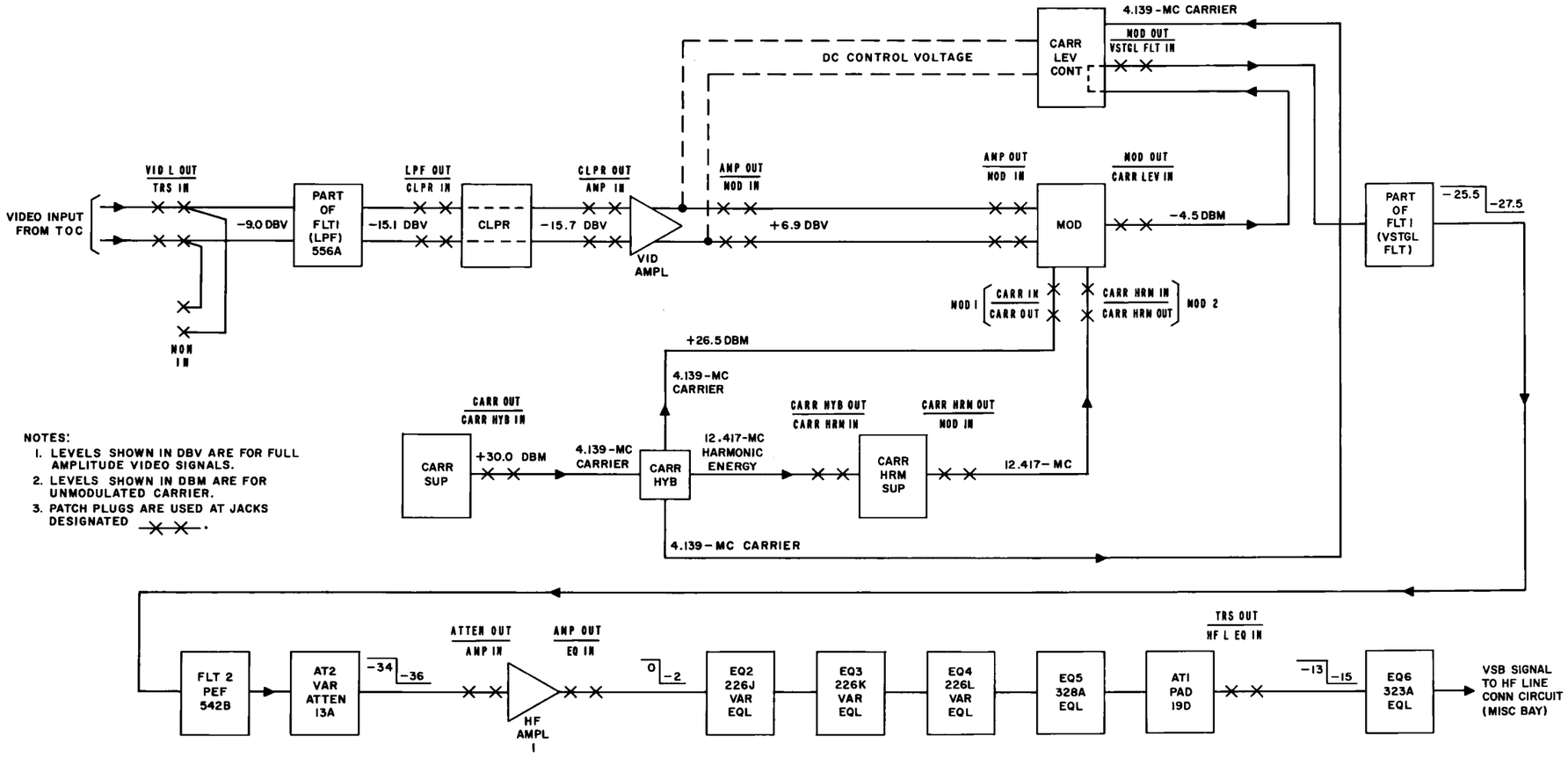
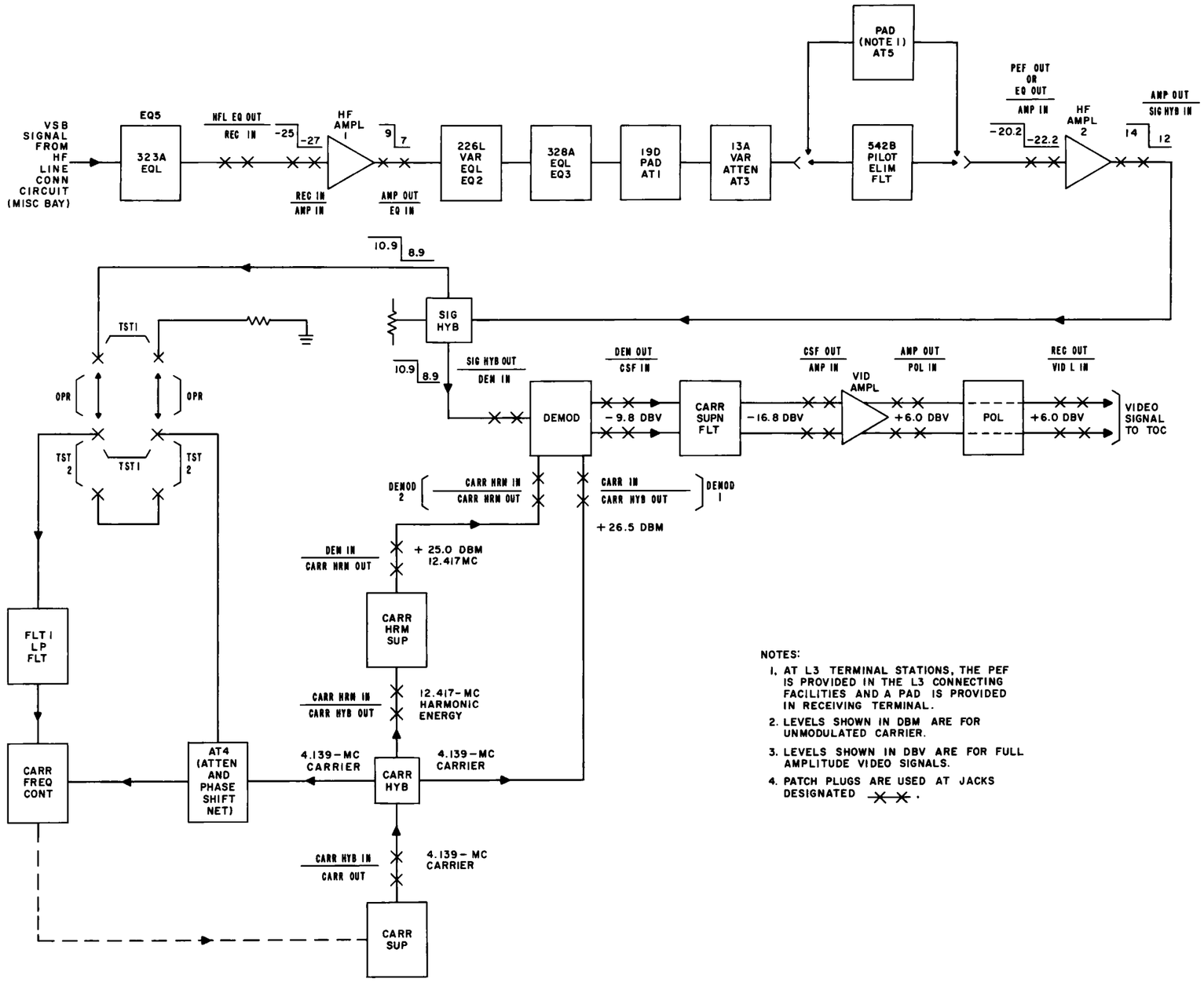


Fig. 14 — T3 Television Transmitting Terminal, Simplified Block Diagram



NOTES:

1. AT L3 TERMINAL STATIONS, THE PEF IS PROVIDED IN THE L3 CONNECTING FACILITIES AND A PAD IS PROVIDED IN RECEIVING TERMINAL.
2. LEVELS SHOWN IN DBM ARE FOR UNMODULATED CARRIER.
3. LEVELS SHOWN IN DBV ARE FOR FULL AMPLITUDE VIDEO SIGNALS.
4. PATCH PLUGS ARE USED AT JACKS DESIGNATED ✕✕.

Fig. 15 — R3 Television Receiving Terminal, Simplified Block Diagram

4. TRANSMITTING TERMINAL EQUIPMENT

A. General

4.01 The transmitting terminal equipment consists of the units shown in Fig. 14. These units are described in the following paragraphs. Several of the units are identical (except for strapping or other connecting arrangements) with some of the units used in the receiving terminal. For this reason, the coverage given in the following paragraphs describes these units with regard to application in either terminal. Differences or optional arrangements, where applicable, are shown in the associated illustrations. The descriptions covering power equipment are given in Part 6, Power Supply Arrangements.

B. Video Clipper

4.02 The video clipper is a shunt device used in the transmitting terminal to limit the peak-to-peak amplitude of the video signal to an adjustable value. The circuit is shown in functional block diagram (Fig. 16) and consists of an input amplifier (A1), a cathode follower and dc inserter (A2), and an unbalanced-to-balanced output amplifier (A3) which is operative only when its input signal exceeds a reference bias. The reference bias is determined by the setting of the THRESHOLD control on the clipper panel. As shown in Fig. 16, the video signal is supplied from the input low-pass filter through a resistor-inductor combination to the video amplifier. Resistors R1, R2, R3, and R4 and the inoperative impedance of the output amplifier (A3) constitute a 0.6-db balanced pad. Inductors L3, L4, L5, and L6 build out the terminations at high frequencies. The clipper circuit which is bridged (shunted) across the 124-ohm balanced line, employs feedback to reduce the bridging (shunt) impedance during periods when the video signal level exceeds threshold value. When the signal amplitude at the input of amplifier A3 is less than threshold value, the feedback loop is open and the bridging impedance of amplifier A1 is high. The loss from the low-pass filter to the video amplifier is then 0.6 db. When the signal at the input of amplifier A3 exceeds threshold value, the feedback loop is closed and the bridging impedance of the clipper is reduced almost to that of a short circuit for those portions of the signal

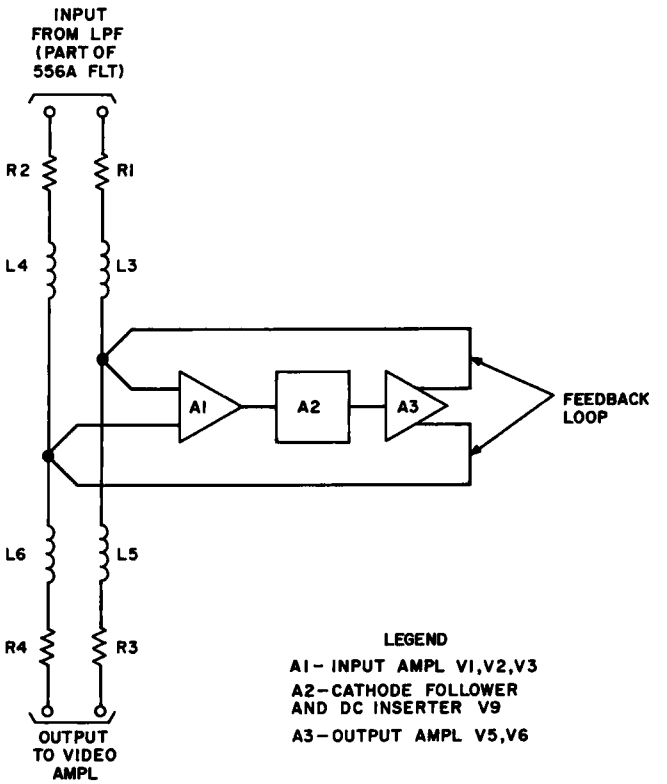


Fig. 16 — Clipper Circuit, Functional Block Diagram

that exceed threshold level. The THRESHOLD control is normally adjusted to limit the video signal to a value 3 db above normal signal level. Limiting action is practically independently of picture content.

4.03 Fig. 17 is a simplified schematic diagram of the clipper circuit. Electron tubes V1, V2, and V3 form a balanced-to-unbalanced amplifier stage with the control grids of V2 and V3 coupled to the 124-ohm transmission line through dc blocking capacitors C1 and C2. Equal but opposite signal voltages are applied to the grids of V2 and V3. If V1 were not provided, each tube would provide equal amplification and half the total output would be developed at the plate of each tube. In a conventional balanced-to-unbalanced amplifier where the output signal is taken from one of the two plate circuits, only half the total output is utilized and the 6-db advantage in voltage gain provided by the other tube is lost. In the clipper circuit, however, tube V1 utilizes the output of V3 to recover the 6-db loss. The output of V3 is supplied to V1, which amplifies the

signal and supplies it back to the cathode of V3. Tube V1 completes a local negative feedback loop around V3 in such a way that the signal voltage at the cathode of V2 is very nearly equal but opposite in polarity to the signal voltage at the grid of V2. The effective drive on V2 is therefore doubled enabling, V2 to produce twice the output in its plate circuit.

4.04 Plate voltage for V1 is obtained from the cathodes of V2 and V3. The cathode current of the two tubes flows through the parallel combination of V1 and R64. Resistor R64 is required because V1 is capable of conducting only half the total cathode current of V2 and V3. The cathode bias is held at about 100 volts and is determined by the dc potentials supplied to the grids. For V2, the grid voltage is established by resistors R10, R11, R19, and R68. The screen currents of V2 and V3, and the current drain through the THRESHOLD control (R46) also influences the dc voltage at the grid of V2. These connections help stabilize the operation of V2 and V3 against circuit and tube variations. They also provide some local signal feedback which reduces low-frequency waveform distortion. The dc grid voltage for V3 is supplied from the voltage divider formed by resistors R14 and R16 connected between ground and the plate of V3. The operating point of V3 is stabilized by the dc feedback from the plate.

4.05 The output of the balanced-to-unbalanced amplifier is taken from the plate of V2 and directly coupled to the cathode follower section of double triode tube V9. The direct coupling reduces interstage capacity to a minimum and permits maximum coupling over the video band. The plate load for V2 consists of resistor R24 in series with interstage peaking coil L2. The grid of the cathode follower is returned to ground through the plate load of V2 in series with the plate power supply.

4.06 The low-impedance output of the cathode follower is supplied through parallel connected capacitors C7 and C13 to the cathode of the dc inserter portion of V9 and to the control grid of V5. The polarity of the video signal on the line is such that the signal at the output of the cathode follower is a wave having synchronizing pulses which are negative-going with respect to the picture portion: i.e., the sync tips of the signal are less positive than the picture portions. The function of the dc inserter is to hold the sync tips to the level determined by the voltage at the junction of resistor R45 and potentiometer R46 (about +150 volts) independent of picture content. The voltage at the grid of V5 therefore never falls below the +150 volts (approximately) at the cathode of the inserter, but can rise above the +150 volts depending on maximum positive excursions of the wave.

4.07 The unbalanced-to-balanced amplifier consists of V5 and V6 and associated components. The amplifier, however, does not function unless the video signal on the line exceeds a certain level determined by the setting of the THRESHOLD control. This control forms part of a voltage divider connected between ground and the +315 volt supply. A positive voltage, normally higher than the voltage at the junction of R45 and R46, is supplied through resistor R39 to the grid of V6. V6 conducts for any setting of the THRESHOLD control and therefore develops cathode bias across resistor R41. This cathode bias is sufficiently high to cut off V5 except when the signal at the grid of V5 overcomes this bias. The THRESHOLD control therefore determines the level at which clipping occurs.

4.08 Whenever the picture portion of the signal at the grid of V5 is of sufficient amplitude to cause V5 to conduct, the signal current of V5 flows through cathode resistor R41 and develops a signal voltage on the cathode of V6. With signal voltage present at the cathode, V6 produces an output complementary to the output of V5. Both V5 and V6 then function as a conventional unbalanced-to-balanced amplifier for signal levels exceeding threshold value.

4.09 The output is coupled to the 124-ohm line through capacitors C14 and C15 and then supplied back to the grids of V2 and V3 in an out-of-phase relationship with the video signal on the line. This negative loop feedback is sufficient to limit the amplitude of the video signal to the level established by the THRESHOLD control setting.

4.10 A network consisting of resistor R52 and inductor L1 in the cathode circuit of V5 prevents a loop sing in the 10- to 20-mc range.

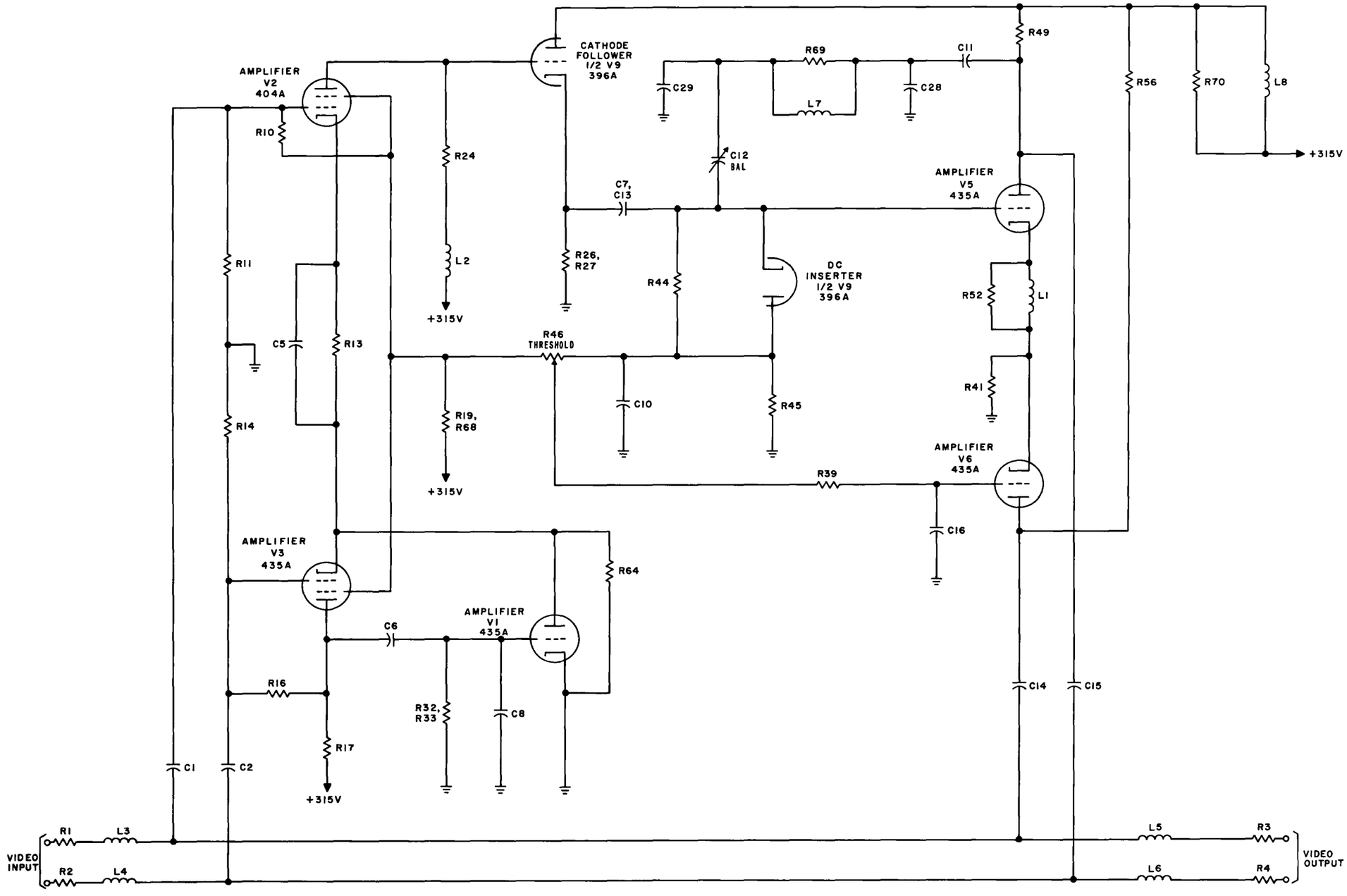


Fig. 17 — Video Clipper, Simplified Schematic Diagram

Resistor R13 and capacitor C5, in the cathode circuit of the input amplifier, help shape the loop characteristic. Capacitors C24 and C25, not shown in Fig. 17, are connected from the plate circuits of V5 and V6 to the grid circuits of V3 and V2, respectively. These capacitors augment the negative loop feedback at high video frequencies during periods when the clipper circuit is operative.

4.11 With a normal amplitude video signal on the line, the video signal at the grid of V5 is insufficient to cause V5 to conduct. However, the parasitic capacity of V5 permits coupling between the grid and cathode at high video frequencies. Since V6 is conducting, this high-frequency current is transmitted to the plate of V6, and hence to the line with very little loss. This unbalanced current produces both a metallic component (current that flows in one direction on one side of a pair of wires and in the opposite direction on the other side of the pair) and a longitudinal component (currents that flow in the same direction on each side of the pair). The metallic component, if not eliminated, produces a transmission characteristic for the clipper circuit during periods when the circuit should be quiescent.

4.12 The metallic component is eliminated by means of a network consisting of capacitors C11, C12, C28, and C29; inductor L7; and resistor R69. The network is connected between the grid and the plate of V5 and simulates the impedance between the grid of V5 and the plate of V6. The variable BAL capacitor C12, when properly adjusted, corresponds to the parasitic grid-cathode capacity of V5. This network eliminates the metallic transmission distortion by supplying to the other side of the balanced line a component which is equal in phase and amplitude. The result, however, is a large longitudinal component. Since the modulator (following the clipper circuit in the transmission path) cannot function properly with a large longitudinal input, the longitudinal component must also be suppressed.

4.13 Longitudinal suppression is achieved by returning the V5 and V6 plate load resistors (R49 and R56) to the plate of V9. A parallel network, which consists of resistor R70 and inductor L8, acts as a plate load for V9 and also provides the means for supplying +315 volt plate power to three tubes. V9 develops a signal across this network which is supplied to each side of the balanced line through the V5 and V6 plate load resistors and the plate-to-line coupling capacitors, C14 and C15. These signal currents are in an equal but opposite relationship to the currents flowing between the grid and the plate of V5 (via the compensating network) and between the grid of V5 and the plate of V6 (via the parasitic grid-cathode capacity of V5 and the electron coupling of V6). Because the currents effectively cancel each other, a minimum of longitudinal current flows into the terminations.

C. Video Amplifier

4.14 The video amplifier is used in the transmitting terminal to raise the video signal at the output of the clipper to a level sufficient to drive the modulator. It is used in the receiving terminal to raise the demodulated signal to the proper terminal output level. Certain wiring options are provided in the video amplifier to permit its use in either the transmitting or receiving television terminal.

4.15 The video amplifier is designed for operation between 124-ohm balanced circuits. It consists of two separate but electrically identical unbalanced amplifiers connected in a push-pull arrangement to form a single balanced amplifier. The video amplifier is a tube-type unit utilizing cathode feedback. It has a fixed gain of 22.5 $\pm$0.6 db and its gain-frequency characteristic is constant to within 0.05 db over the video band of frequencies from 60 cps to 4.2 mc. The amplifier is shock-mounted to reduce its susceptance to microphonic interference. Fig. 18 is a simplified schematic diagram of the video amplifier showing the two unbalanced sections and the manner in which feedback is obtained.

4.16 In order to ensure stability in the video amplifier, the loop gain and phase characteristics are controlled to frequencies far beyond the useful band. The design is such that maximum stability of the forward gain characteristic is achieved along with very low harmonic distortion. The gain, measured between input and output terminals, changes less than 0.1 db at frequencies below 5 mc for an internal gain change (due to tube aging or other variations including irregularities in the plate supply voltage) or 6 db.

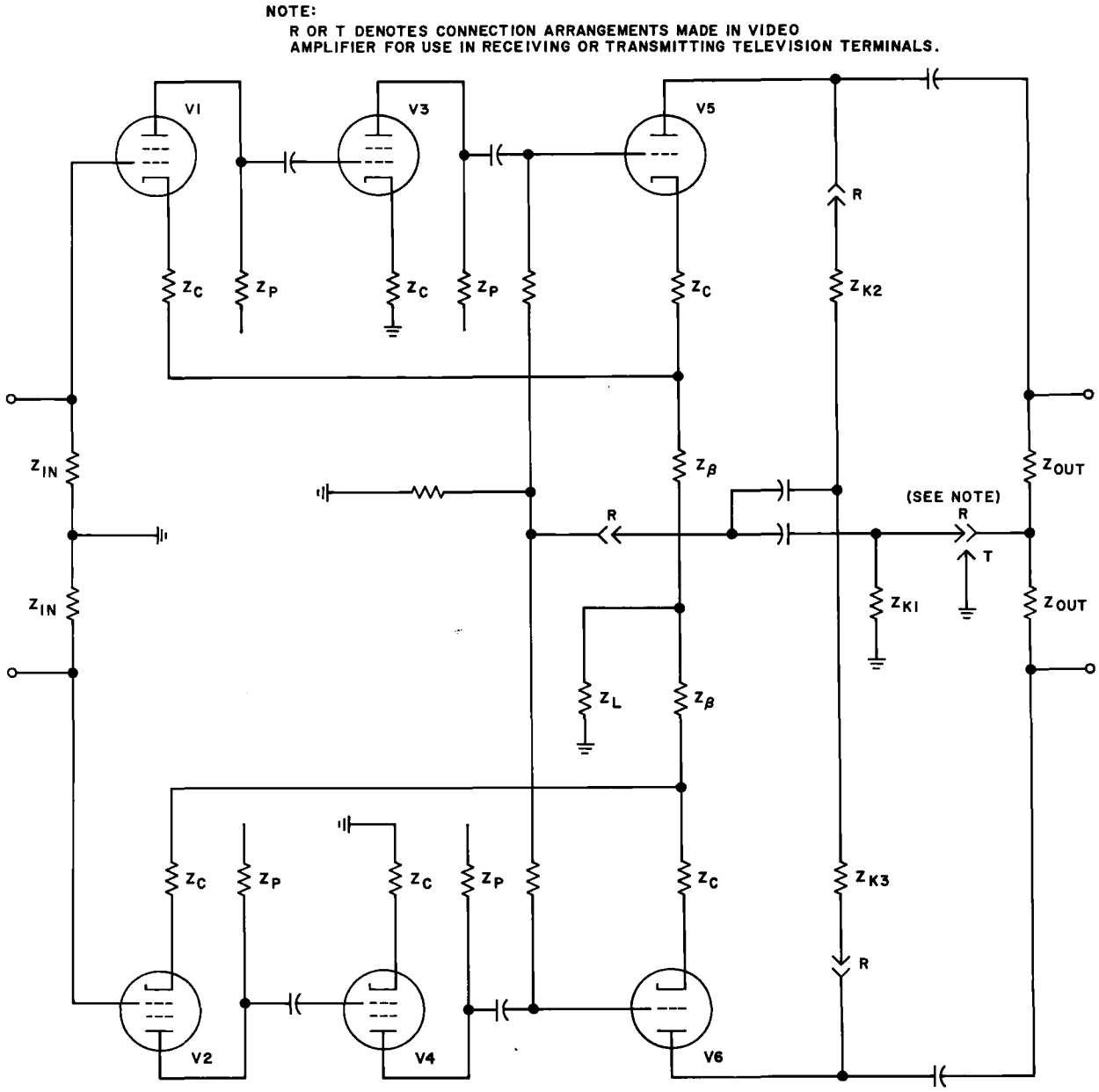


Fig. 18 — Video Amplifier, Simplified Schematic Diagram

4.17 Each unbalanced amplifier consists of three stages. The cathodes of the first and third stages are coupled together, as shown in Fig. 18, to form a feedback loop around each amplifier, and are returned to ground through impedances Z_β and Z_L. Feedback voltages for the two amplifiers are developed across the two Beta networks (Z_β), while impedance Z_L provides longitudinal feedback. Current feedback is also provided by impedance Z_C in the cathode circuit of each stage. The impedance of Z_C varies inversely with frequency. The plate load impedances (Z_P) do not provide feedback but contribute to the overall response function of the amplifier.

4.18 Each of the Beta networks, shown in Fig. 18, has a constant impedance of 2.25 ohms over the entire video band. This constant impedance is obtained by careful electrical

and mechanical design as shown in the cross section and schematic diagram of the network, Fig. 19.

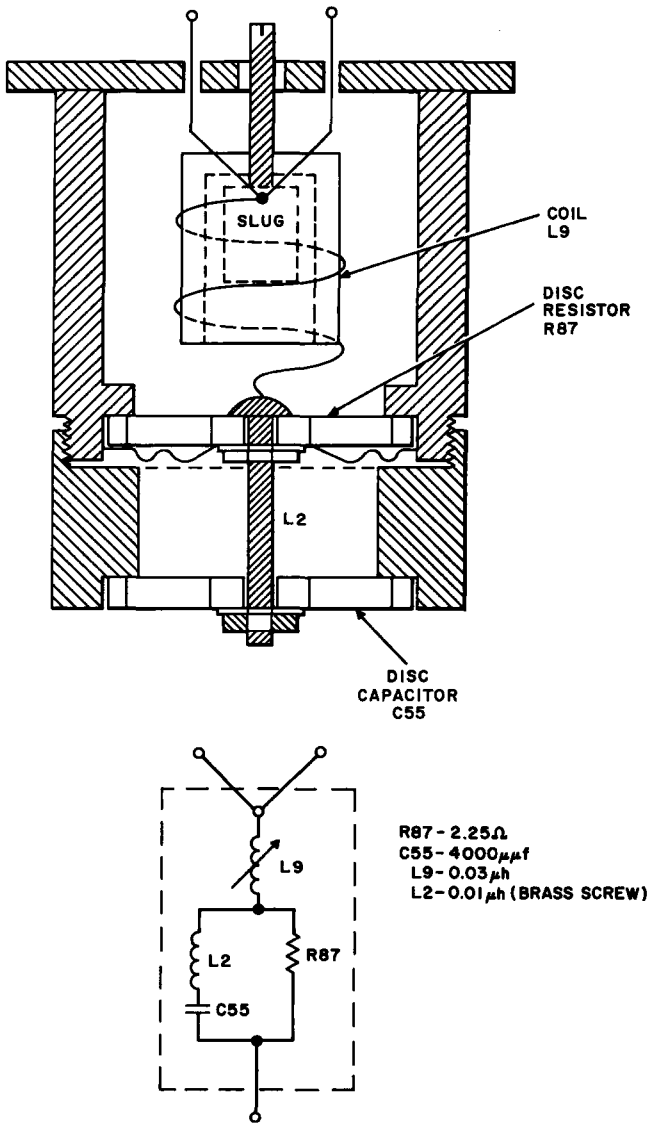


Fig. 19 — Cross Section and Schematic Diagram of Beta Network in Video Amplifier

4.19 Since the signal currents of the two amplifiers flow in opposite directions through Z_L, no signal voltage is developed across this impedance. Longitudinal currents, however, develop a voltage across Z_L which, in the transmitting terminal, provides the greatest amount of suppression at frequencies below about 250 kc. Z_L has an impedance of 27.1 ohms at low frequencies and is bypassed at high frequencies by four 0.006-μf capacitors.

4.20 In the receiving terminal, impedance Z_L is arranged to suppress a longitudinal 4.139-mc carrier leak from the demodulator. Suppression at 4.139 mc is obtained by a parallel resonant circuit adjusted at the factory. Fig. 20 shows the longitudinal transmission characteristic curves for the video amplifiers used in the transmitting and receiving television terminals.

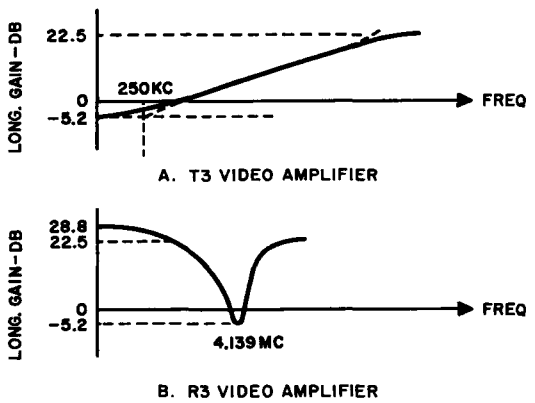


Fig. 20 — Video Amplifier, Longitudinal Transmission Characteristic Curves

4.21 Since the video amplifier, when used in the receiving terminal, is arranged for maximum suppression of longitudinal 4.139-mc carrier leak, impedance Z_L provides no feedback for low-frequency longitudinal currents. The amplifier transmits low-frequency power supply interference, sometimes called "bobble," which, if uncorrected, appears as a low-frequency longitudinal output signal. Impedance Z_{K1}, shown in Fig. 18, offers a high impedance to these low-frequency longitudinal currents. The voltage developed across this impedance is fed back out-of-phase with the longitudinal voltage at the third stage grid of each unbalanced amplifier. This feedback provides suppression of the low-frequency interference. Impedances designated Z_{K2} and Z_{K3} supplement the longitudinal feedback provided by Z_{K1}.

4.22 The video amplifier used in the transmitting terminal does not require impedance Z_{K1}, Z_{K2}, or Z_{K3}. As shown in Fig. 18, the output terminations Z_{OUT} are returned to ground at their junction and Z_{K1}, Z_{K2}, and Z_{K3} are removed from the circuit.

4.23 A somewhat more detailed schematic diagram of one half of the video amplifier is shown in Fig. 21. The video input signal appearing across resistor R89 is supplied to the grid of the first amplifier stage, V1. Coupling is through capacitor C1 and a shaping network which consists of inductor L1, resistors R25 and R27, and capacitor C3. Resistor R27 suppresses parasitic oscillation. The network provides partial control of the feedback, gain, and phase margins over the video band of frequencies.

4.24 When the video amplifier is connected for use in the receiving terminal, the grid of V1 is returned to ground through resistor R23, and operating bias for the tube is developed across cathode resistor R29 in series with the Beta network (L2, L9, C55, and R87) and the longitudinal suppression network (L11, R85, and C51 through C54). Since R87 in the Beta network has a low resistance (2.25 ohms) and inductor L11 in the longitudinal suppression network is essentially a short circuit for direct current, the tube bias is developed primarily across R29.

4.25 When the video amplifier is connected for use in the transmitting terminal, inductor L11 is not used and the cathode of V1 is returned to ground through R29, the Beta network, and resistor R85 in the longitudinal suppression network. In order to establish the proper operating bias for V1, grid resistor R23 is returned to the junction of a voltage divider consisting of resistors R81 and R82.

4.26 Resistor R29 in the cathode circuit of V1 is bypassed at high video frequencies by capacitor C5. At the low video frequencies, the impedance of C5 becomes very large and maximum local feedback is obtained from the RC combination.

4.27 An additional step in the low-frequency end of the response curve is provided by screen dropping resistor R41 and capacitor C17. The RC combination has a time constant of approximately 0.013 second which corresponds to the period of approximately 1 cycle of a 75-cps wave. A longer time constant would result in a greater overall amplifier gain at low frequencies, whereas a shorter time constant would result in a lesser gain. The design of the RC circuit, therefore, is such that a flat overall amplifier response is achieved. Capacitor C15 is the high-frequency bypass. Resistor R39 provides decoupling between capacitors C15 and C17 and prevents oscillation caused by a resonant condition. R37 is an antising resistor.

4.28 At high video frequencies, resistor R31 serves as the plate load for V1. A peaking circuit consisting of inductor L3, capacitor C11, and resistor R33, shapes the $\mu\beta$ gain curve to reduce phase shift to a minimum.

4.29 The high-frequency video signals are coupled through capacitor C19 to the grid of V3, which is returned to ground through series connected resistors R43 and R45. At low video frequencies, resistor R35 serves as the plate load for V1, and coupling to the grid circuit of V3 is through capacitor C9. The connection is made at the junction of grid resistors R43 and R45.

4.30 Capacitor C7 is provided to build out the capacity of C9 (measured between the inside foil and ground) to a value approximately equal to the parasitic capacity (measured between the outside foil and ground).

4.31 A shaping network in the grid circuit of V3, consisting of capacitor C21, inductor L5, and resistor R47, provides partial control of the feedback, gain, and phase margins.

4.32 Electron tube V3 provides the second stage of amplification in the unbalanced amplifier. Cathode bias is developed across resistor R49. Capacitor C23 completely bypasses R49 at the medium and high frequencies, and permits the stage to operate at maximum gain. At the very low video frequencies, the impedance of C23 becomes very large and a step in the $\mu\beta$ gain curve is produced by resistors R49 and R51, and capacitors C23, C25, and C27. The screen circuit of V3 is similar to that of V1 and also produces an RC step in the low-frequency end of the feedback curve. Resistor R53 is the plate load for V3 and resistor R103 is an antising resistor. Coupling to the grid of the triode connected output tube V5 is provided by capacitor C35.

4.33 The grid of V5 is returned to ground through series resistors R61 and R83. When the video amplifier is connected for use in the receiving terminal, bias for the stage is developed primarily across cathode resistor R65 in series with the Beta and longitudinal suppression networks. However, when the video amplifier is arranged for use in the transmitting terminal (inductor L11 in the longitudinal suppression network disconnected), V5 cathode current flows through resistor R65, the Beta network, and resistor R85 in the longitudinal network. Proper grid bias for the stage is then provided by resistors R86 and R83 connected as a voltage divider.

4.34 Cathode resistor R65 is bypassed at high video frequencies by capacitor C37. At low video frequencies, the impedance of C37 becomes very large, and the RC combination provides maximum local feedback. The cathode circuits of V1, V3, and V5 all contribute to maintain the proper shape of the feedback curve.

4.35 V5 functions as a triode connected amplifier with the plate and screen connected together through antising resistors R67 and R71. The output signal appears across plate load resistor R69 and is coupled through capacitor C41 and a shaping network to the output connection terminal. The shaping network consists of inductor L7, resistor R77, and capacitor C43. Resistor R73, at the junction of capacitor C41 and the shaping network, terminates the amplifier in the proper impedance for matching to the line.

4.36 When the video amplifier is used in the receiving terminal, resistor R73 is returned to ground through a longitudinal feedback circuit comprised of resistor R84 and capacitor C49. This circuit corresponds to impedance Z_K in Fig. 18, and is required to suppress low-frequency power supply interference which would otherwise appear as a low-frequency longitudinal output signal. The signal developed across this network is fed back through capacitor C61 to the junction of series-connected grid resistors R61 and R83. Additional feedback is provided by resistor R101 and capacitor C57 in the plate circuit of V5. When the video amplifier is arranged for use in the transmitting terminal, this circuit is not required and the terminating resistor (R73) is returned directly to ground.

4.37 Resistor R75 and capacitor C59 are required when the video amplifier is used in the transmitting terminal. These components provide a means for combining the output current of the carrier level control circuit with the output signal of the video amplifier.

D. Modulator

4.38 The modulator circuit translates a video signal in the 0- to 4.2-mc range to a carrier signal in the L3 television range. The circuit accomplishes the translation by modulating a 4.139-mc carrier with a video signal to produce a double-sideband output. The 4.139-mc carrier is also present in the output depending on the value of the dc voltage supplied to the modulator from the carrier level control circuit. (See 3.09.) Corresponding frequency components appear on each side of the carrier, with the upper sideband extending from 4.139 mc to approximately 8.3 mc and the lower sideband extending from 4.139 mc to approximately zero. The desired output is the upper sideband, the 4.139-mc carrier, and a portion of the lower sideband extending approximately 500 kc below the carrier frequency.

4.39 Another product is also generated which must be suppressed to prevent interference with the demodulated picture signal. This unwanted component is a double-sideband signal produced when the video signal modulates the third harmonic of the 4.139-mc carrier frequency. The lower sideband of this undesired output overlaps the desired upper sideband of the fundamental carrier frequency. (See 3.07.)

4.40 The desired output (with unwanted interference products suppressed) is obtained in a modulator unit which utilizes two separate, double-balanced, lattice-type circuits. (See Fig. 22.) The video input to each circuit is supplied by means of a resistance hybrid with an input impedance which matches the 124-ohm balanced output impedance of the video amplifier. The modulated outputs of the two circuits are connected to a hybrid transformer (T5) which matches a 75-ohm unbalanced output load impedance. Carrier voltages for each of the two modulator sections are supplied from separate sources having 75-ohm unbalanced output impedances.

4.41 The desired output plus the undesired interference product is generated in one of the two modulator sections (Mod 1). The other section (Mod 2) generates an identical interference product as its main output. These two outputs are combined in the hybrid transformer so that the interference products cancel and only the desired output generated by Mod 1 is transmitted through the hybrid.

4.42 The input resistance hybrid consists of resistors R20, R21, and R22, and capacitor C12. The hybrid is designed to supply the video signal to Mod 2 at a level 10 db less than supplied to Mod 1. The difference in power levels is such that the principle output of Mod 2 is of the same amplitude as the unwanted third harmonic products generated in Mod 1. The two interference products, when combined in the output hybrid, are approximately equal in amplitude but opposite in phase and will effectively cancel.

4.43 As shown in Fig. 22, Mod 1 consist of varistor CR1 and associated components connected between transformers T1 and T2. A 4.139-mc high-amplitude carrier voltage from the carrier supply circuit is fed through transformer T1 and resistors R1 and R2 to the modulator. This carrier is modulated by the video signal supplied between the center taps of T1 and T2. The output (which includes the high-level interference product) appears across the secondary winding of T2. It is then supplied via the MOD 1 OUT and HYB IN jacks and associated patch plug, to the output hybrid transformer (T5).

4.44 Mod 2 consists of CR2 and associated components connected between transformers T3 and T4. A 12.417-mc carrier voltage from the carrier harmonic supply circuit is fed through transformer T3 and resistors R15 and R16 to the modulator. As in Mod 1, this carrier is modulated by the video signal connected between the center taps of T3 and T4. The double-sideband output appears across the secondary winding of T4 and is supplied, via the MOD 2 OUT and HYB IN jacks and associated patch plug, to hybrid transformer T5.

4.45 The transmission and impedance characteristics of each modulator circuit necessitate the use of an isolation pad between Mod 1 and transformer T2, and also between Mod 2 and transformer T4. Each pad provides 6.2-db attenuation, but because of dc balance requirements part of the series resistance of each pad is placed on the input side of each modulator. The pad associated with Mod 1 therefore consists of series arms R1 plus R11 and R2 plus R12, and the shunt arm R13. The pad associated with Mod 2 consists of similar components, with R15 plus R17 and R16 plus R18 as series arms, and R24 as the shunt arm. (See Fig. 22.)

4.46 The varistors in the modulator are not perfectly matched and the transformers not perfectly balanced. Consequently, carrier and video signal balancing circuits are required to minimize carrier and video signal leak in the modulator output. Mod 1 utilizes a dc voltage supplied to the carrier branch to balance video leak from the output. Similarly, a dc voltage is supplied to the video branch to balance carrier leak from the output. These dc voltages are derived from the carrier level control circuit and the +190 volt metallic rectifier.

4.47 Fig. 23 is a functional schematic diagram of the modulator unit, part of the carrier level control circuit, and part of the video amplifier. The figure shows the manner in which the dc voltages are supplied to the modulator (Mod 1). Output tubes V8 and V9 in the carrier level control circuit function as dc amplifiers with dc changes on the control grids reflected as dc changes at the cathodes. As shown in the figure, cathode leads designated A and B are connected through resistors R75 and R76 in the video amplifier to output levels designated M and N. When switch S1 in the carrier level control circuit is set to the BAL position, the dc voltages on leads M and N will differ depending on the setting of the CARR BAL 1 control (R62). These two voltages are then supplied over leads M and N to the input resistance hybrid in the modulator. The two voltages divide in the resistance hybrid so that current flows in both Mod 1 and Mod 2. The current flowing in Mod 2, however, results in no significant consequence since the CARR BAL 1 control is adjusted to provide maximum suppression of the 4.139-mc carrier at output hybrid transformer T5. After initial carrier balance is achieved in Mod 1, switch S1 in the carrier level

control circuit is set to OPR. In the operate condition, the carrier level control circuit functions as described in 3.09.

4.48 Video signal leak is balanced from the Mod 1 output by the SIG BAL 1 control. (See Fig. 23.) A dc voltage derived from the +190 volt metallic rectifier is supplied through resistors R5 and R4 to SIG BAL 1 potentiometer R14A. The voltage divides at the movable arm of R14A, depending approximately on the ratio of resistances between each side of the carrier branch and the movable arm. The voltage on one side of the carrier branch can therefore be greater or lesser than or equal to the voltage on the other side, depending on the conditions required for video balance.

4.49 Potentiometer R14B, which is ganged with R14A and driven by the same shaft, provides compensation for dc unbalances caused by the setting of R14A. The dc voltage required for compensation is supplied from the junction of R4 and R5 to the movable arm of R14B. With the movable arm at the midpoint, the voltage at the junction of R9, R10, and R27 will be at its minimum value, but will increase for potentiometer settings on either side of the midpoint. Since the two potentiometers (R14A and R14B) are driven by a common shaft, only one setting of the SIG BAL 1 control is required to achieve video balance.

4.50 The SIG BAL 1 control, in addition to providing a means for balancing video from the output, provides a means for reducing a distortion product. This product is described as $2C - V$: i.e., its frequency is twice the carrier frequency, minus the frequency of the video signal. For a 4-mc video input, $2C - V$ is equal to 2 (4.139 mc) — 4.0 mc, or 4.278 mc. The SIG BAL 1 control is effective in reducing this product, but the best setting of SIG BAL 1 for $2C - V$ is not necessarily the same as the best setting for video balance. A balance against $2C - V$ is important because at the higher video frequencies this product falls into the transmission band. The final setting of SIG BAL 1 must therefore be a compromise between the balance minima.

4.51 Quadrature carrier balance is controlled by adding to the output a small amount of quadrature-phase carrier obtained from a capacity divider. The divider is connected across the secondary winding of carrier input transformer T1, and consists of variable CARR BAL 2 capacitor C1 in series with fixed capacitor C11. (See Fig. 22.) The CARR BAL 2 control permits adjustment of the amount of quadrature-phase carrier supplied to the secondary winding of the Mod 1 output transformer (T2). This control and the CARR BAL 1 control (on the carrier level control circuit) are both adjusted for maximum suppression of 4.139-mc carrier at the MOD OUT jack on the modulator panel. The CARR BAL 2 control, however, introduces a certain amount of quadrature video signal leak in the output of Mod 1, caused by the capacity differential across the secondary of transformer T1. Compensation for this quadrature video signal leak is provided by variable SIG BAL 2 capacitor C2. This capacitor couples a small amount of quadrature-phase video signal voltage from the center tap of T3 to the secondary winding of the Mod 2 output transformer (T4). The voltage is approximately equal in amplitude to the quadrature video signal leak of Mod 1 and the two signals cancel in the modulator output hybrid transformer (T5).

4.52 Other components, shown in Fig. 22, contribute to the proper operation of the modulator. Capacitors C3, C4, and C5 associated with the SIG BAL 1 circuit bypass the dc paths. Resistors R19 and R26 across the input hybrid provide a dc path for the balancing currents and prevent excessive dc voltages from building up on C3, C4, and C5 when the modulator input is unterminated. Capacitors C8 and C10, across the secondary windings of T2 and T4 respectively, are provided to obtain an optimum impedance at the MOD OUT jack (J6). Resistor R23 terminates the unused leg of output hybrid transformer T5.

E. Carrier Level Control Circuit

4.53 The carrier level control circuit functions to maintain the peak carrier output of the modulator constant during the synchronizing time intervals, i.e., during the intervals when no picture information is transmitted. The circuit

controls the carrier level by sampling the modulator output and deriving from this sampling process a dc voltage. This voltage is supplied to the video amplifier, where it is then fed, along with the video signal, to the modulator. The modulated output for various video input signal amplitudes is shown in Fig. 9A through 9E. Fig. 8 shows the manner in which the modulator produces the waveforms of Fig. 9 when the video signal is superimposed on the dc voltage.

4.54 Fig. 24 is a functional block diagram of the carrier level control circuit and associated units. An amplifier whose output is tuned to 4.139 mc and which has a passband of approximately 1 mc is bridged to the modulator output at point A. Unmodulated 4.139-mc carrier from the carrier hybrid is supplied through a phase shifter and attenuator network to the amplifier at point B. At frequencies within the 1-mc passband of the tuned amplifier, the two signals add in the proper phase relationship to produce an output with an index of modulation substantially less than 1 (less than 100 percent).

4.55 The output of the tuned amplifier is supplied to a biased detector which conducts only when the amplitude of the composite signal at synchronizing intervals exceeds a certain value. The transmitted portion (at the output of the biased detector) therefore consists of a carrier wave having an envelope corresponding to the sync tips. Filtering removes the carrier component but the envelope is retained. The envelope is then amplified and supplied to a peak detector to produce a uniform dc voltage that varies in proportion to the variation in peak carrier amplitude during the synchronizing intervals. An unbalanced-to-balanced dc amplifier following the peak detector couples the dc voltage to the grids of a balanced cathode follower, which in turn supplies the dc voltage back to the modulator unit via the video amplifier output circuitry.

4.56 When the picture signal is removed from the terminal, the carrier level control circuit continuously samples the output of the modulator. In the absence of picture information, the modulator output corresponds to the same conditions as those at synchronizing intervals. (See Fig. 9A.) The dc voltage fed back to the modulator is therefore approximately the same as the dc derived during the synchronizing intervals of a composite signal. This dc unbalances the modulator so that the carrier amplitude at the output is very nearly the same as the peak-to-peak amplitude at sync intervals when picture information is present. Since the feedback loop maintains the carrier amplitude constant at the input to the biased detector, it follows that the amplitudes of the signals at points A and B must also be constant. If the amplitude of the signal at point B is changed, the amplitude of the signal at point A will change. The peak-to-peak amplitude of the carrier signal in the modulator output can therefore be set in the absence of video modulation. The CARR LEV control is provided to permit this adjustment.

4.57 Fig. 25 is a simplified schematic of the carrier level control circuit. As shown in the figure, the modulator output is supplied to the vestigial filter through terminal TSC1 and the MOD OUT and VSTGL FLT IN jacks (J1 and J2). The modulator output is also supplied from terminal TSC1 through capacitor C2 to the grid of input amplifier V1. Tubes V1 and V2 and their associated components form a 38-db tuned feedback amplifier. Plate load impedances Z1 and Z2 are each tuned to 4.139 mc and together provide a 1-mc bandpass for the 2-stage amplifier. A large negative feedback from the plate circuit of V2 to the cathode circuit of V1 is obtained through a resistance-capacity dividing network comprised of resistors R10 and R5, and capacitors C11 and C7. Capacitor C30 provides a means for coupling resistor R10 to the plate of V2 while blocking the dc plate voltage from the feedback circuitry. The large negative feedback between V2 and V1 stabilizes the two stages against variations in the interstage gain and also against variations in overall performance caused by tube or component aging.

4.58 Resistor R5 has a high value to ensure that most of the feedback power is dissipated in the cathode of V1 and not in the cathode resistance. Because of the excessive bias developed, the grid is returned through resistor R68 to a voltage divider comprised of resistors R75 and R76. The divider provides a stabilized positive potential of 11 volts to establish correct operating bias for the tube. The voltage divider is connected across gas regulator tube V10, which maintains a constant potential of 100 volts between its

terminals. Tube V2 also operates with stabilized bias. The same voltage divider (R75 and R76) that provides the 11-volt positive potential for the grid of V1 also supplies 11 volts through resistor R15 to the grid of V2. The voltage developed across cathode resistor R16 establishes the correct operating bias.

4.59 A high-level carrier voltage generated in the carrier supply circuit is supplied via the carrier hybrid to terminal TSC2 in the carrier level control circuit. The carrier voltage is then fed through a fixed phase shift network and the CARR LEV control circuitry to the cathode of V1. The phase shift network consists of inductors L2 and L6, capacitors C31 and C32, and resistor R7. It provides a means for supplying the high-level carrier in the proper phase relationship with the signal supplied from the modulator. Variable CARR LEV capacitor C9, in parallel with fixed capacitor C8, provides a means for establishing the proper carrier amplitude. A modulated input signal at the grid, in combination with a high-level carrier at the cathode, produces at the plate of V1 a wave which has a modulation percentage substantially less than 100 because of the added carrier. This high-frequency wave is coupled through capacitor C5 to the grid of V2, where it is amplified and coupled through capacitor C12 to the grid of V3.

4.60 Vacuum tube V3 functions as a biased detector and cathode follower. It also operates with a stabilized positive grid potential of +11 volts supplied through resistor R17 from the junction of resistors R75 and R76. A cathode bias of approximately 52 volts (derived from the cathode of tube V4) fixes the net operating bias of V3 at approximately 41 volts. All positive portions of the composite wave (supplied from the plate of V2 to the grid of V3) that are in excess of 41 volts peak are transmitted through V3 and appear on the cathode. This portion of the amplified wave, which consists only of the modulated tips of the synchronizing pulses, is fed through a low-pass filter (L5, C15, C16, and C17) to the cathode of V4. The wave at this point is a rounded version of the synchronizing pulses with the carrier component removed.

4.61 Tube V4 functions as a high-gain amplifier. Its grid is supplied with a stabilized 50-volt positive potential obtained from a voltage divider connected across gas regulator tube V10. The divider is composed of resistors R21 and R22. With tube V4 conducting continuously, a cathode bias of approximately 52 volts is developed across resistor R30. The net operating bias for the tube is therefore approximately 2 volts. Since the cathodes of V3 and V4 are dc coupled through inductor L5, the cathode of V3 is held at the required 52-volt potential. Capacitor C18 removes any carrier which might otherwise be present at the grid of V4. The plate load for V4 consists of parallel-connected resistors R24 and R25. These resistors also provide the grid return for V5, since direct coupling is used between the two stages. Tube V5 is a dual triode which utilizes only one of the two sections as a peak envelope detector.

4.62 The rounded synchronizing pulse tips supplied to the grid of V5 appear at the cathode These pulses will produce, after filtering, a dc voltage proportional to their peak amplitudes, provided they are all of the same width. However, the pulses supplied to the cathode of V4 from the filter in the cathode circuit of V3 are not of equal width. This variation in pulse width is sufficient to influence the peak value of dc voltage at the output of the filter in the cathode circuit of V5. The effect is minimized by means of a differentiating circuit consisting of capacitor C19 and the effective resistance of R21 arranged to provide feedback. The pulses at the cathode of V5 are supplied via the differentiating circuit back to the grid of V4, tending to produce at the grid of V5 pulses that have a sharp rise time and a fairly rapid decay. Consequently, the tips of these pulses are essentially of the same width when transmitted through V5. They are then integrated by capacitor C20 and parallel-connected resistors R29 and R78. The resulting voltage across capacitor C21 is a uniform dc whose changes in value are a function of only amplitude changes in the synchronizing pulse tips. A voltage divider, consisting of resistors R31 and R32, is connected across capacitor C21. It supplies the dc voltage at the proper value to the grid of V6. Capacitor C28 across resistor R32 removes any carrier which might be present at the grid of V6.

4.63 Vacuum tubes V6 and V7 constitute a conventional unbalanced-to-balanced cathode-coupled dc amplifier. A voltage divider, comprised of resistors R36 and R42 connected between the +190 volt supply and ground, provides a 51-volt

positive potential for the grid of V7. Changes in dc voltage at the grid of V6 appear as changes in cathode bias across common cathode resistor R43. These changes, in turn, change the net operating bias of V7 so that the plate of one tube goes positive whenever the other goes negative. Parallel-connected resistors R80 and R35 provide the plate load for tube V6, and parallel-connected resistors R82 and R37 provide the plate load for V7. The plate of V6 is connected through resistor R44 and the OPR contacts of BAL – OPR key S1 to the grid of tube V8. The grid of V8 is returned to ground through resistor R46. Resistor R44 (connected through the closed OPR contacts of S1) and resistor R46 form a voltage divider which couples any change in dc potential at the plate of V6 to the grid of V8. Similarly, the plate of V7 is connected through resistor R57 and the OPR contacts of S1 to the grid of tube V9. The grid of V9 is returned to ground through resistor R53. Any change in voltage at the plate of V7 is coupled to the grid of V9. Tubes V8 and V9 are cathode followers which supply the dc voltages at their cathodes to the modulator circuit by means of a voltage divider located in the video amplifier.

4.64 A voltage divider composed of resistor R61, CARR BAL 1 potentiometer R62, and resistors R63, R64, and R65, is connected between the +190 volt supply and ground. With BAL – OPR key S1 in the BAL position, the grid of V9 is supplied with a fixed voltage obtained at the junction of resistors R63 and R64. The grid of V8 is connected to the movable arm of the CARR BAL 1 potentiometer, which is adjusted to supply a potential either greater or less than the potential on the grid of V9. The potentiometer is set only during modulator circuit alignment and is adjusted in conjunction with the CARR BAL 2 control (located on the modulator unit) to achieve minimum carrier leak in the modulator output. After proper adjustment, the BAL – OPR key is returned to the OPR position. Carrier output from the modulator is then established by the setting of the CARR LEV control. The BAL – OPR key, in addition to providing the means for disabling the carrier level control circuit during modulator alignment, permits transmission measurements to be made using sine waves as test signals. If the feedback loop is not opened during such tests, by operating the key to the BAL position, large transmission measurement errors will occur.

F. Carrier Supply Circuit

4.65 The carrier supply circuit is used in both the T3 and R3 television terminals to supply the 4.139-mc carrier required for modulation and demodulation. Certain wiring options are provided to permit its use in either of the two terminals.

4.66 The circuit is designed to deliver a 4.139-mc sine wave into a 75-ohm load at a level of approximately +30 dbm. It consists primarily of a bridge-stabilized oscillator and a power amplifier. The oscillator portion utilizes crystal frequency control and thermistor amplitude control. The power amplifier portion utilizes a single-frequency output circuit which matches the plate load impedance of the tube to the 75-ohm impedance of the carrier hybrid. A jack designated CARR TST provides a means for measuring the carrier frequency and also for measuring the power output at a 0-dbm level relative to the +30 dbm carrier output level. Fig. 26 is a simplified schematic diagram of the carrier supply circuit. The wiring options which permit its use in either terminal are shown by alternate connection arrangements designated T for the transmitting and R for the receiving television terminals.

4.67 The oscillator consists of a 40-db tuned amplifier and a 40-db positive feedback loop comprised of a self-balancing bridge. As shown in Fig. 26, the adjacent arms of one side of the bridge are formed by thermistor TH and the 2-5 winding of transformer T1. The adjacent arms of the other side of the bridge are formed by resistor R19 in parallel with the 1-4 winding of transformer T1, and crystal unit Y1. When the carrier supply circuit is used in the transmitting terminal, resistor R22 builds out the resistance of the arm containing the crystal. When used in the receiving terminal, resistor R22 is replaced by saturable reactor L3 and associated components. The saturable reactor functions as a tuning element under control of the external carrier frequency control circuit. As described in 3.19, this circuit detects phase differences between the oscillator frequency and the received carrier frequency, and relates these phase differences to dc changes at the input to a balanced dc amplifier. The output of the dc amplifier is reflected as current changes in the control winding of the satura-

ble reactor, which in turn provides the means for locking the oscillator frequency in phase with the received carrier frequency.

4.68 As shown by polarity symbols in Fig. 26, the bridge is arranged so that transformer T1 provides positive feedback and thermistor TH provides negative feedback between the cathode of V2 and the grid of V1. When power is first applied to the circuit, the voltage change that occurs at the cathode of V2 is coupled through the transformer as positive feedback to the grid of V1. Very little voltage is coupled through the thermistor as negative feedback since the cold resistance of the thermistor is high. Tube V1 amplifies the voltage on its grid and supplies it to the grid of V2. The signal current through V2 develops a signal voltage across V2 cathode resistor R10, which in turn is coupled back to the grid of V1. Oscillation at the crystal frequency begins and, under these conditions, builds rapidly. Thermistor TH heats as signal current flows through it, and its resistance decreases. As the thermistor resistance decreases, the bridge approaches but never quite achieves a condition of perfect balance. Consequently, the signal voltage supplied back to the V1 grid is reduced to a very small value, which stabilizes at the point where the loss through the bridge is exactly equal to the forward gain from the grid of V1 to the cathode of V2. Any tendency toward further change is compensated by resistance changes in the thermistor, and the amplitude of oscillation remains constant. FREQ ADJ capacitor C1 provides a means for initially adjusting the oscillator frequency to that of a 4.139-mc reference frequency. The range of adjustment is at least ±25 cps.

4.69 The nearly zero signal voltage at the V1 grid is amplified and supplied through capacitor C6 to the grid of V2. Network Z1, which consists of capacitor C4 and inductor L1, forms the plate load impedance of V1 and is tuned to 4.139 mc. A voltage divider, comprised of resistors R7 and R8 connected between the plate supply and ground, supplies a 9.2-volt positive potential to the V2 grid. A potential of 11.2 volts, developed across V2 cathode resistor R10, provides a net working bias of 2 volts for the tube.

4.70 The output of the plate of V2 is coupled through an L network and dc blocking capacitor C10 to the CARR OUT jack, J2. The L network, comprised of capacitor C9 and inductor L2, matches the plate impedance of the tube to the 75-ohm line. Plate power for the tube is supplied through a relatively low-resistance divider connected between the plate supply bus and the low-impedance end of L2. The divider is comprised of parallel-connected resistors R12 and R14 in series with resistor R13. It provides, in addition to a means for supplying dc plate power to the tube, a means for extracting a portion of the output for frequency measurements or relative output power tests. The ratio of resistances in the divider is such that an approximate +10 dbm power level exists at the junction of the divider for a +30 dbm output power level measured at the CARR OUT jack. The output of the divider is supplied to CARR TST jack J1 through dc blocking capacitor C11 and an L pad comprised of resistors R20 and R21.

4.71 The L pad is designed to match a load impedance of 75 ohms connected to the CARR TST jack. The impedance looking into the L pad, i.e., at the junction of the divider, remains essentially constant with or without the 75-ohm load connected and is approximately equal to the resistance value of R21. The attenuation provided by the L pad (approximately 10 db) permits measurements at a 1-mw (0 dbm) power level relative to the +30 dbm output of the tube. In addition, the 10-db attenuation provides effective isolation between the divider and the CARR TST jack and minimizes the effects caused by a reactive load connected to the jack. Since the overall load into which the tube works remains essentially constant, the level of the signal delivered to the carrier hybrid via the CARR OUT – CARR HYB IN jacks also remains essentially constant.

4.72 The saturable reactor is wound on a ferrite core with a magnetic path common to two other windings wound on another core and which have direct current flowing through them. The magnetic fields produced by the direct current flowing in the two windings determine the degree of saturation of the reactor core. The degree of saturation affects the high-frequency core permeability, and hence, the inductance of the reactor winding.

4.73 Direct current flowing in the 4-8 (bias) winding establishes the average saturation of the reactor core and therefore establishes the

nominal inductance of the 5-6 (reactor) winding. Direct current flowing in each half of the center-tapped 1-3 (control) winding can alter the degree of saturation depending on whether the field produced around the control winding aids or opposes the field produced by the bias winding. When the current flowing in one half of the control winding is equal in magnitude but opposite in direction to the current in the other half, the magnetic fields produced by the two halves cancel and the degree of saturation of the reactor core is dependent only on the field produced by the bias winding. In actual circuit application, the currents in each half of the control winding are not equal, and the magnetic field that exists as a result of the unequal currents adds to or subtracts from that of the bias winding. The inductance of the reactor winding is therefore a function of the combined fields of the bias and control windings.

4.74 Although not shown in Fig. 26, the control winding and associated components are connected between the plates of a balanced dc amplifier in the carrier frequency control circuit. Plate power for the two sections of the dc amplifier is supplied from the 315-volt metallic rectifier connected at the center tap of the control winding. The current for one section flows through the 2-3 winding while current for the other section flows through the 2-1 winding and series resistor R28. A slight difference in the two currents exists because of the additional resistance in series with the 2-1 winding. If the oscillator frequency differs in phase from that of the received carrier frequency, one section of the dc amplifier will draw more current while the other section will draw less. As the relative polarity of the field changes, the field will either aid or oppose the field produced by the bias winding in such a manner that the inductance of the reactor winding will either increase or decrease by an amount sufficient to correct the oscillator phase.

4.75 The amount by which the reactor winding shifts the oscillator frequency is restricted to ±20 cps, since the first sideband components of the received signal are ±30 cps from the carrier. The limitation prevents possible synchronization of the locally generated carrier with one of these sideband components.

4.76 Bias current for the saturable reactor is supplied by means of a voltage divider connected between the plate supply bus and ground. The divider is comprised of fixed resistor R15, variable symmetry (SYM) control R17, and fixed resistor R18. The SYM control is adjusted at the factory to establish the point about which the oscillator frequency can be shifted. The range over which the frequency can be shifted is determined by the setting of variable RANGE control R26. This control, in series with fixed resistor R27, forms a shunt effectively connected across the control winding. It provides the means for adjusting the effective inductance of the winding, and therefore the degree of saturation of the reactor core. The setting is adjusted at the factory to obtain a frequency change of ±20 cps for a direct current change of ±2.0 ma in the control winding. Fig. 27 graphically illustrates the control characteristic for correct settings of the SYM and RANGE controls.

4.77 A QUAD TST key, located on the branching and control panel in the receiving terminal, makes possible a reversal in the connections between the control winding and the plates of the dc amplifier in the carrier frequency control circuit. Since the currents flowing in each half of the control winding are not equal (because of the resistance of R28), a reversal in connections causes the larger of the two currents (flowing in the 2-3 winding) to flow in the opposite direction through the 2-1 winding. The reversal in direction causes a polarity change in the magnetic field which shifts the oscillator phase by exactly 90° with respect to the received carrier frequency. This deliberate phase shift permits certain adjustments which are normally made during system alignment. The function of the QUAD TST key and the manner in which the alignment adjustments are performed are covered in the paragraphs describing the carrier frequency control circuit.

4.78 The crystal, its associated resistance and capacitance elements, and the thermistor (which forms one arm of the bridge) are contained in an oven that is maintained at a temperature of 70°C. Transformer T2 supplies 6.1-volt power through a thermistor network to the oven heater. The network, which is part of crystal unit Y1, is mounted externally to the oven. It regulates the oven temperature by varying the heater current inversely with the ambient temperature. Transformer T2, and also transformer

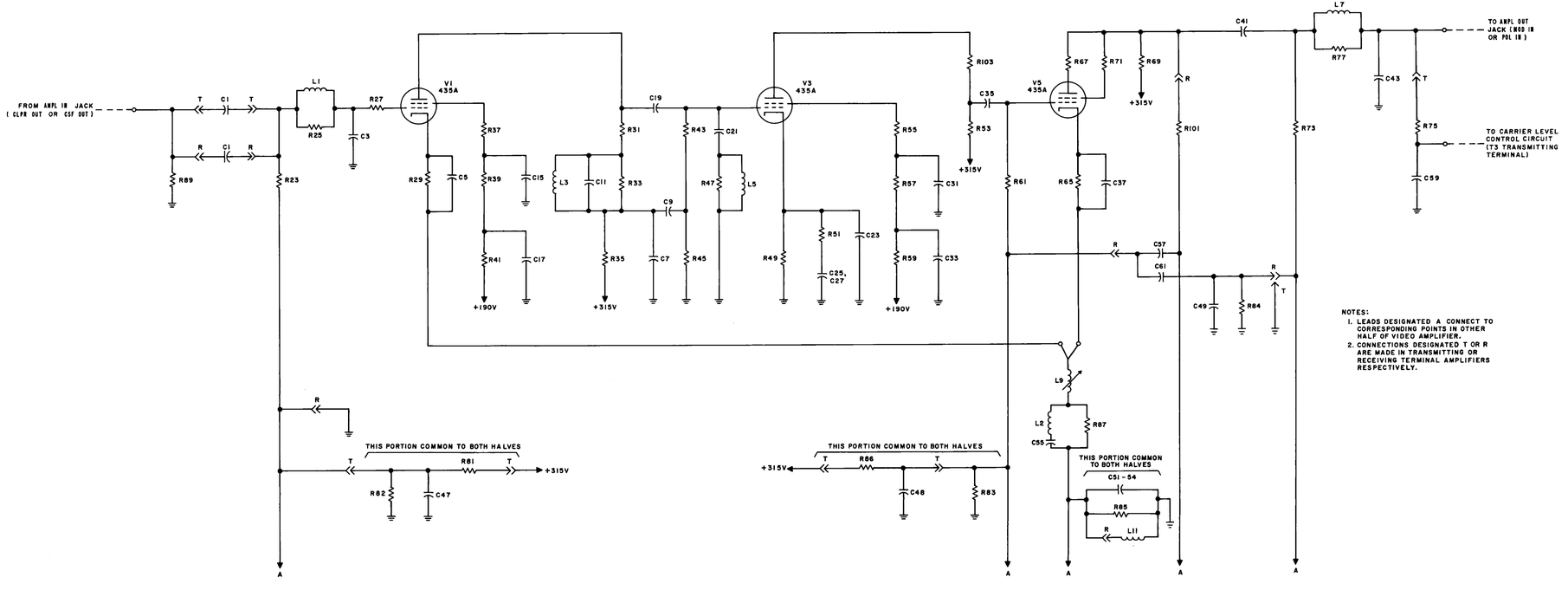


Fig. 21 — One Half of Video Amplifier, Simplified Schematic Diagram

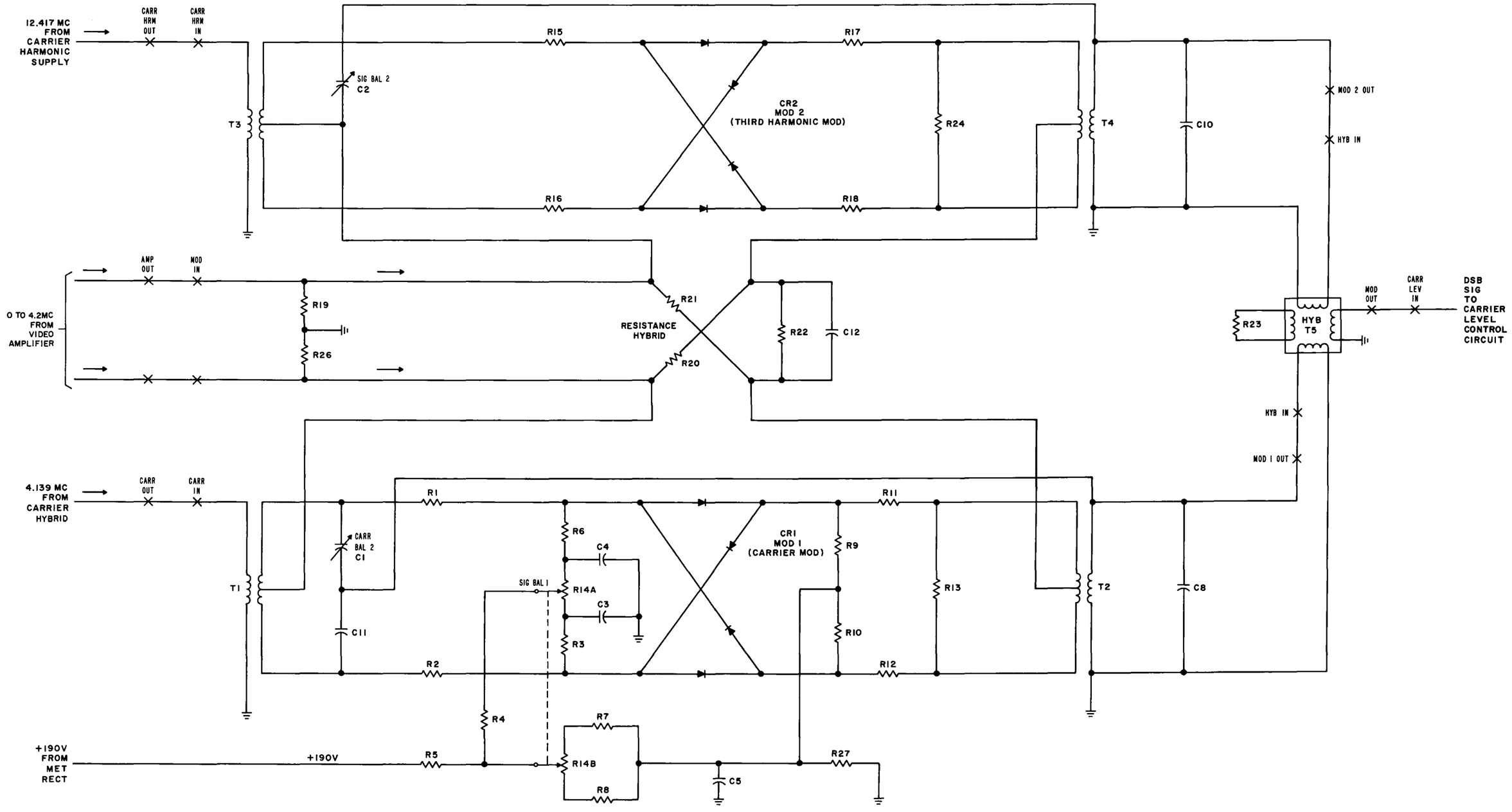


Fig. 22 — Modulator Circuit, Simplified Schematic Diagram

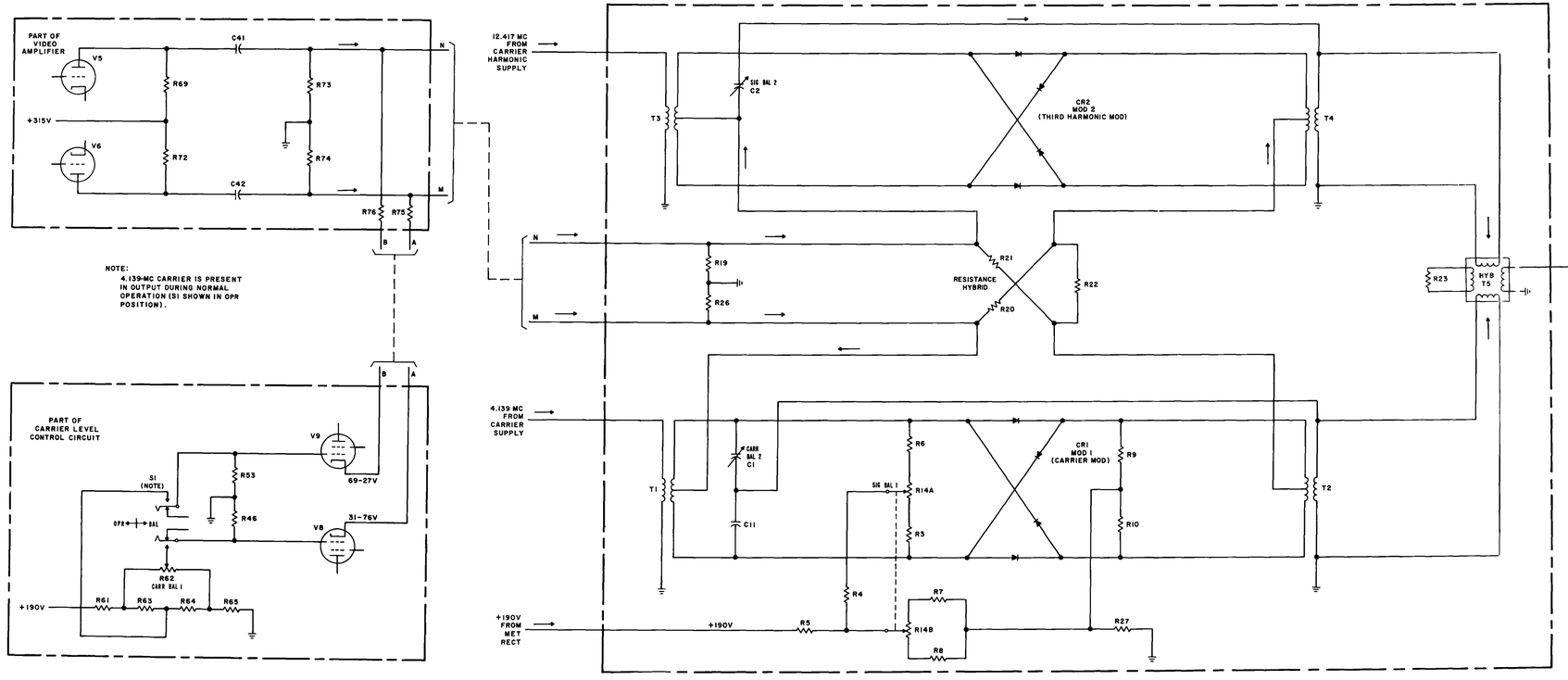


Fig. 23 — Modulator, Carrier Level Control Circuit, and Video Amplifier — Functional Schematic Diagram

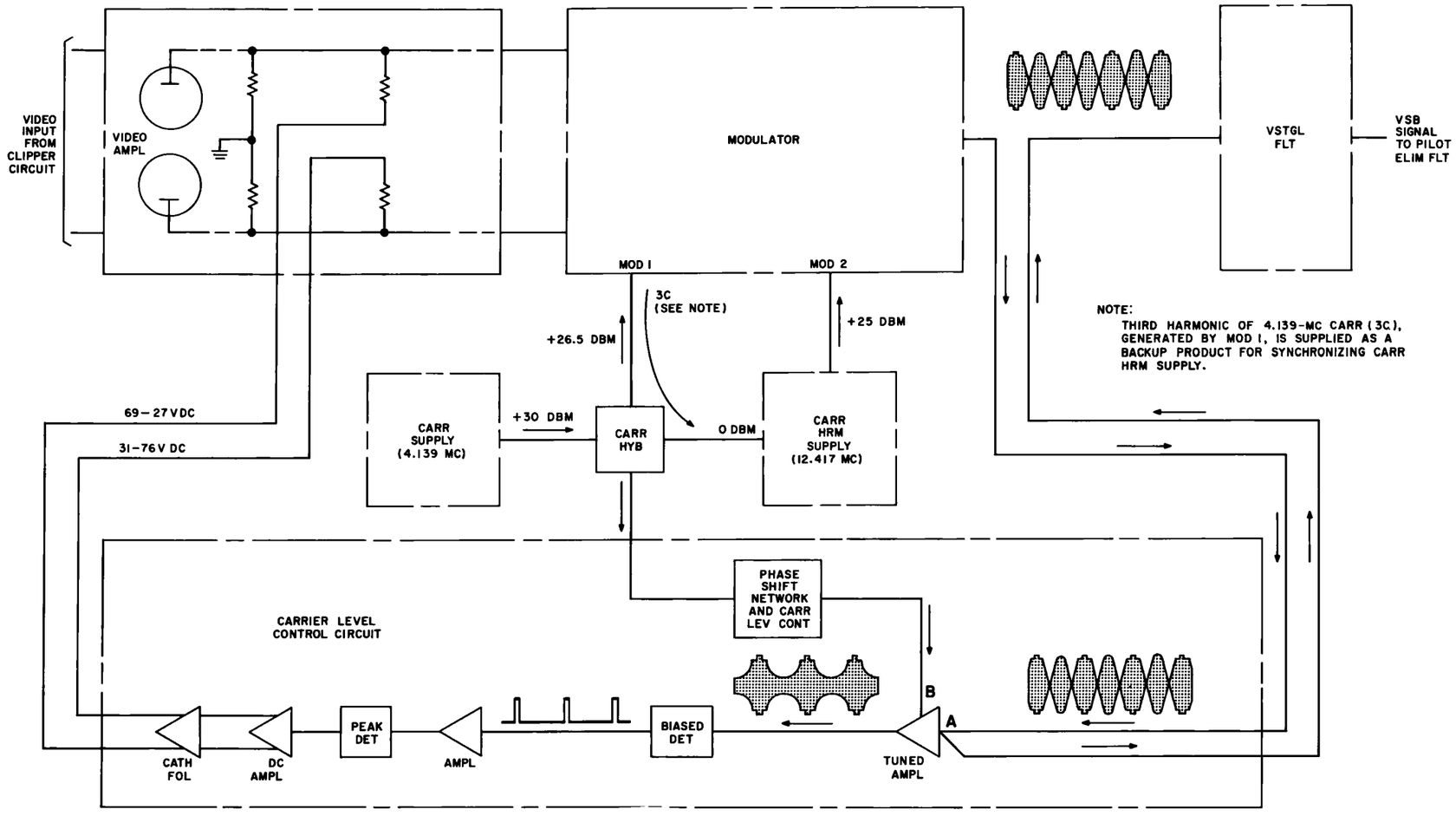


Fig. 24 — Carrier Level Control Circuit and Associated Units, Functional Block Diagram

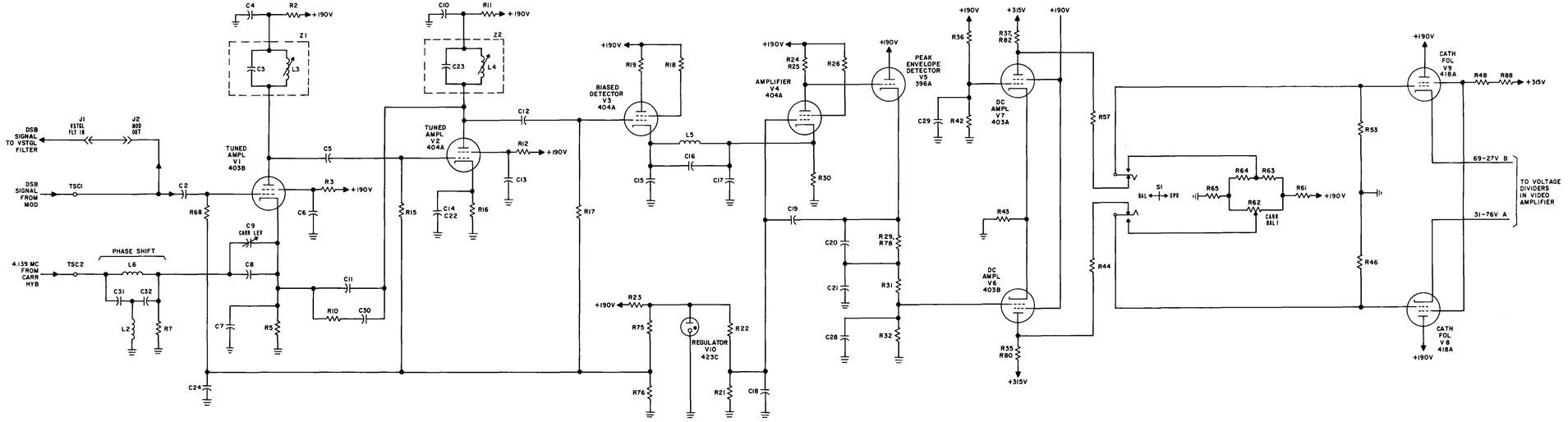
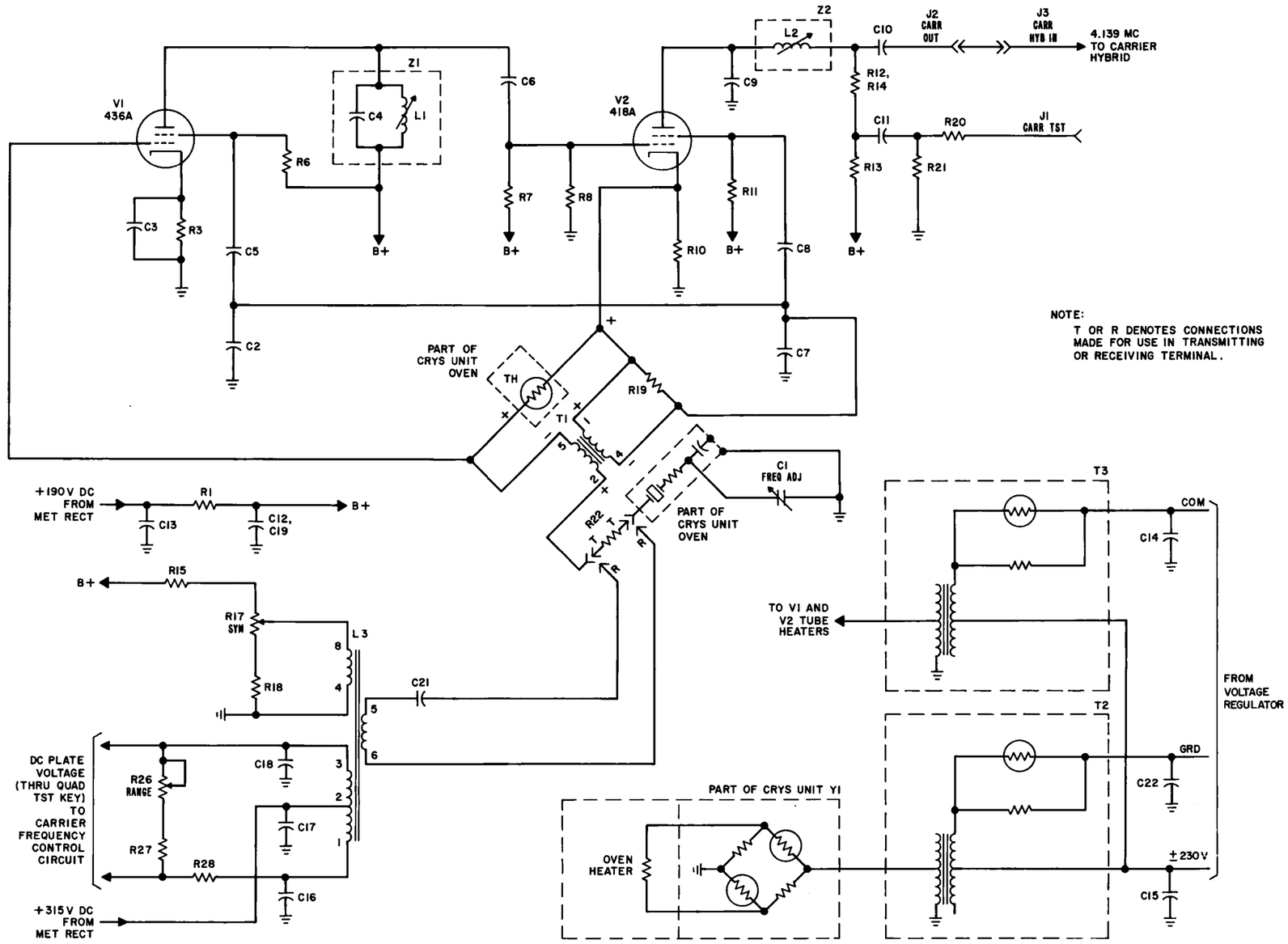


Fig. 25 — Carrier Level Control Circuit, Simplified Schematic Diagram



NOTE:
T OR R DENOTES CONNECTIONS MADE FOR USE IN TRANSMITTING OR RECEIVING TERMINAL.

Fig. 26 — Carrier Supply Circuit, Simplified Schematic Diagram

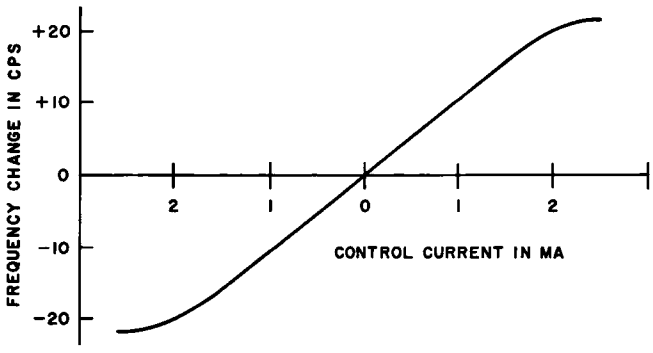


Fig. 27 — Saturable Reactor Control Characteristic

T3 (which supplies 6.1-volt heater power for tubes V1 and V2) include thermistor networks that compensate for secondary voltage variations caused by ambient temperature changes. The ac line connections to the two transformers are bypassed to ground through capacitors C14, C15, and C22. These capacitors prevent carrier energy from appearing in the ac line circuits. Transformers T2 and T3 and the oven heater temperature regulating circuitry are shown in Fig. 26.

4.79 Plate and screen power for tubes V1 and V2, and the direct current required for the bias winding of the saturable reactor, are supplied through a decoupling filter comprised of resistor R1 and capacitors C12, C13, and C19. The filter prevents energy at the oscillator frequency from being coupled back into the power supply.

4.80 Capacitors C16, C17, and C18 bypass the control winding of the saturable reactor and prevent energy at the carrier frequency from being coupled back to the dc amplifier in the carrier frequency control circuit or to the 315-volt metallic rectifier.

G. Carrier Harmonic Supply

4.81 The carrier harmonic supply circuit is used in both the T3 and R3 television terminals to supply the 12.417-mc harmonic energy required for cancellation of an interference product inherent in the normal process of modulation and demodulation.

4.82 The circuit is designed to deliver a sine-wave signal into a 75-ohm load at a level of approximately +25 dbm. It consists primarily of a bridge-stabilized oscillator and a power amplifier. The oscillator portion utilizes the third harmonic of the 4.139-mc carrier for controlling the frequency. This third harmonic energy is produced as a result of the carrier switching action within the modulator and demodulator circuits. The energy appears as a backup product in the carrier hybrid, which in turn supplies it to the carrier harmonic supply circuit for synchronization purposes. The amplitude of oscillation is controlled by means of a thermistor which forms part of the bridge.

4.83 The power amplifier portion utilizes a single-frequency output circuit which matches the plate load impedance of the tube to the 75-ohm input impedance of the modulator or demodulator. A jack designated CARR HRM TST provides a means for measuring the power output at a 0-dbm level relative to the +25 dbm output level of the circuit.

4.84 Fig. 28 is a simplified schematic diagram of the carrier harmonic supply circuit. The oscillator consists of a 40-db tuned amplifier and a 40-db positive feedback loop comprised of a self-balancing bridge. As shown in Fig. 28, the adjacent arms of one side of the bridge are formed by capacitor C5 in parallel with thermistor RT1, and the 2-5 winding of transformer T1. The adjacent arms of the other side of the bridge are formed by the 1-4 winding of transformer T1 and resistor R17.

4.85 As shown by polarity symbols in Fig. 28, the bridge is arranged so that transformer T1 provides positive feedback and thermistor RT1 provides negative feedback between the cathode of V2 and the control grid of V1. When power is first applied to the circuit, the voltage change that occurs at the cathode of V2 is coupled though the transformer as positive feedback to the grid circuit of V1. Very little voltage is coupled through the thermistor as negative feedback since the cold resistance of the thermistor is high. Tube V1 amplifies the voltage on its grid and supplies it to the grid of V2. The signal current through V2 develops a signal voltage across V2 cathode resistor R10, which in turn is coupled back to the grid of V1. Oscillation at a 12.417-mc rate begins, and under these conditions builds rapidly. Thermistor RT1 heats as signal current

flows through it and its resistance decreases. As the resistance decreases, the bridge approaches but never quite reaches a condition of perfect balance. The signal voltage supplied back to the V1 grid is therefore reduced to a very small value which becomes stabilized when the 40-db loss through the bridge is exactly equal to the 40-db forward gain from the grid of V1 to the cathode of V2. Any tendency to shift from this condition is compensated by resistance changes in the thermistor. Capacitor C5 in parallel with the thermistor bypasses a small amount of negative feedback voltage around the thermistor and prevents the circuit from becoming blocked when power is first applied. Resistor R19 and capacitor C8 constitute an impedance-matching terminating network for transformer T1. Capacitor C22 is a bypass. Variable capacitor C23 in parallel with fixed capacitor C21 provides a means for controlling the phase of the feedback loop and therefore the frequency of oscillation. The value of the combination is adjusted at the factory to establish the natural frequency of oscillation to within a few cycles of 12.417 mc. The oscillator can follow a synchronizing frequency of at least 12.417 ±0.050 mc, which is very much wider than actually required.

4.86 The 12.417-mc third harmonic energy required for synchronization is supplied at a level of about —3 dbm along with 4.139-mc energy and other odd harmonic components, through the CARR HRM IN jack J4. A single-frequency network comprised of capacitor C17 and inductor L5 discriminates against unwanted frequency components while passing the desired 12.417-mc signal through transformer T2 and a variable phase shifting network to the grid of V1. The phase shifting network is composed of resistors R22 and R27, inductor L4, fixed capacitor C18, and variable differential capacitor C24 designated CARR HRM PHASE. The output of the variable phase shifting network is supplied from the rotor of capacitor C24 to the grid of V1. The grid of V1 is returned to ground through resistors R16 and R26, the bridge circuit, and V2 cathode resistor R10. Capacitor C19 (which has very low reactance at the operating frequency), in parallel with resistor R26, permits maximum coupling between the bridge and the grid circuit of V1. Capacitor C26, in parallel with resistor R16, has a reactance which is high enough at the operating frequency to allow most of the synchronizing frequency energy to appear on the V1 grid while permitting sufficient coupling between the grid and the bridge.

4.87 A tuned circuit comprised of capacitor C3 and inductor L3 is provided in the cathode circuit of V1. Its reactance is zero at the resonant frequency, i.e., at the third harmonic of 4.139 mc, but is fairly high at the first, fifth, and higher order frequencies. The cathode impedance of tube V1 is therefore fairly high at all but the 12.417-mc operating frequency. The circuit thus provides a measure of negative feedback which results in discrimination against unwanted frequency components. Since the cathode of V1 is at ac ground at the operating frequency, no feedback occurs and operation is enhanced.

4.88 The output of V2 is coupled through an L network and dc blocking capacitor C10 to the CARR HRM OUT jack J2. The L network, comprised of capacitor C9 and inductor L2, matches the plate impedance of the tube to the 75-ohm line. Plate power for the tube is supplied through a relatively low-resistance divider connected between the plate supply bus and the low-impedance end of L2. The divider is composed of parallel connected resistors R12 and R14 in series with resistor R13. Resistor R18, shown in Fig. 27, is not considered part of the divider circuit but is provided as a filter used in conjunction with capacitor C12 to prevent carrier energy from entering the power supply. The divider, in addition to providing the means for supplying plate power to the tube, provides a means for extracting a portion of the output for test purposes. The ratio of resistance in the divider is such that a power level of approximately +8.3 dbm (one-third of the +25 dbm power output measured at the CARR HRM OUT jack) exists at the junction of the divider. The output of the divider is supplied to CARR HRM TST jack J1 through dc blocking capacitor C11 and an L pad comprised of resistors R20 and R21. The L pad is designed to match a load impedance of 75 ohms connected to the CARR HRM TST jack. The attenuation provided by the L pad (approximately 9 db) permits measurements at a 1-mw (0 dbm) power level relative to the approximate +25 dbm output of the tube. In addition, the attenuation provides effective isolation between the divider and the CARR HRM TST jack which minimizes the effects of a reactive load. The constants of the

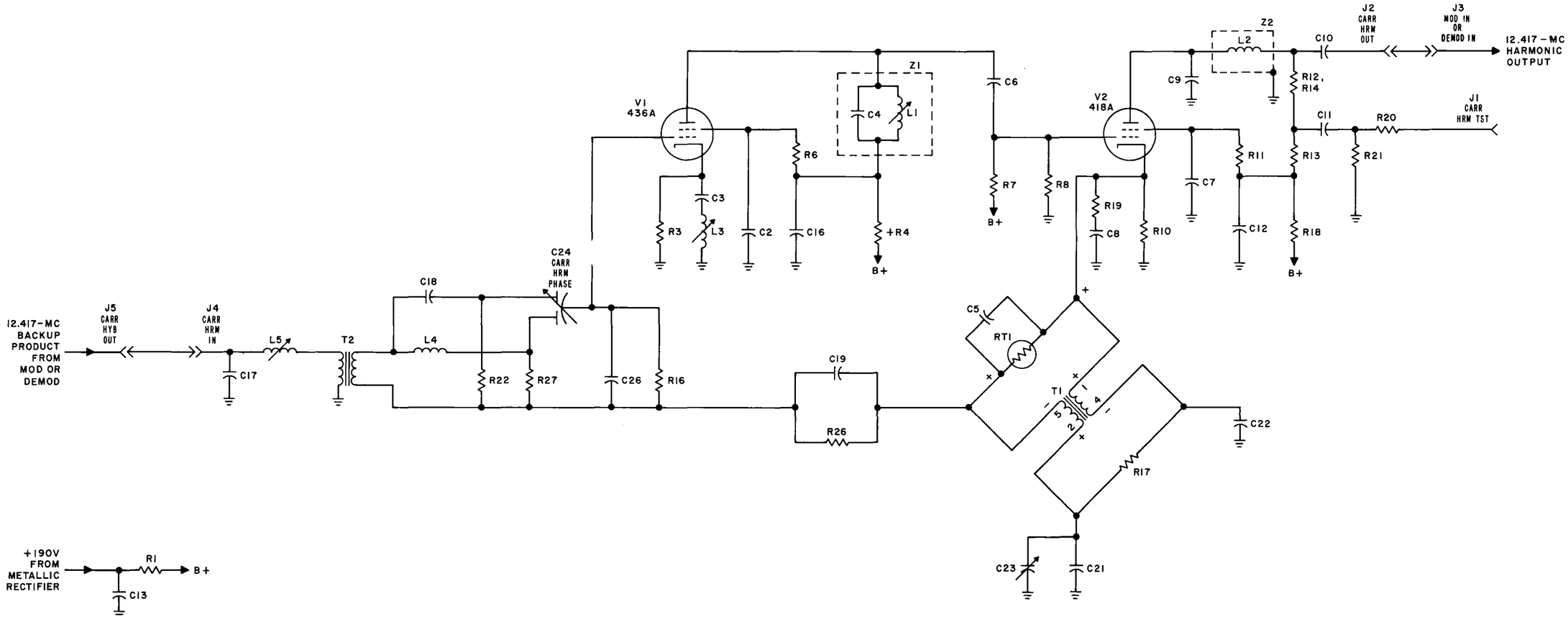


Fig. 28 — Carrier Harmonic Supply Circuit, Simplified Schematic Diagram

circuit are such that the output level at the CARR HRM OUT jack remains almost constant with or without a load connected to the CARR HRM TST jack.

4.89 A decoupling filter consisting of capacitor C13 and resistor R1 prevents carrier energy from flowing back into the power supply. Additional decoupling is provided by capacitor C16 and resistor R4 in the plate and screen circuit of tube V1. Capacitor C12 and resistor R18 provide decoupling for tube V2.

4.90 Although not shown in the figure, transformer T3 supplies ac power to the tube heaters. As in the carrier supply circuit, the 230-volt ac supply leads connected to the heater transformer primary winding are bypassed to prevent carrier energy from being coupled into the ac power line.

H. High-Frequency Amplifier

4.91 High-frequency amplifiers are used in both television terminals to compensate for losses introduced by the filters and equalizers in the carrier sections. One amplifier is required in the transmitting terminal and two in the receiving terminal, as shown in Fig. 14 and 15. The amplifiers are identical, and each provides a nominal gain of 34.0 db over the 300- to 8500-kc band with an inband gain deviation of no more than 0.2 db. The high-frequency amplifier designation distinguishes it from the video amplifier, which operates in the 60-cps to 4.2-mc band.

4.92 The high-frequency amplifier is designed for use in other portions of the L3 coaxial cable system as well as for use in the transmitting and receiving television terminals. It is therefore built to very exacting specifications, both mechanical and electrical. The amplifier is comprised of three basic parts: the input amplifier, the interamplifier network, and the output amplifier. Fig. 29 shows the amplifier configuration.

4.93 The input and output amplifiers are mounted on separate chassis designed for ready removal from the main base casting. The interamplifier network is mounted in an enclosed, shielded compartment, which also serves to shield the component amplifiers from each other.

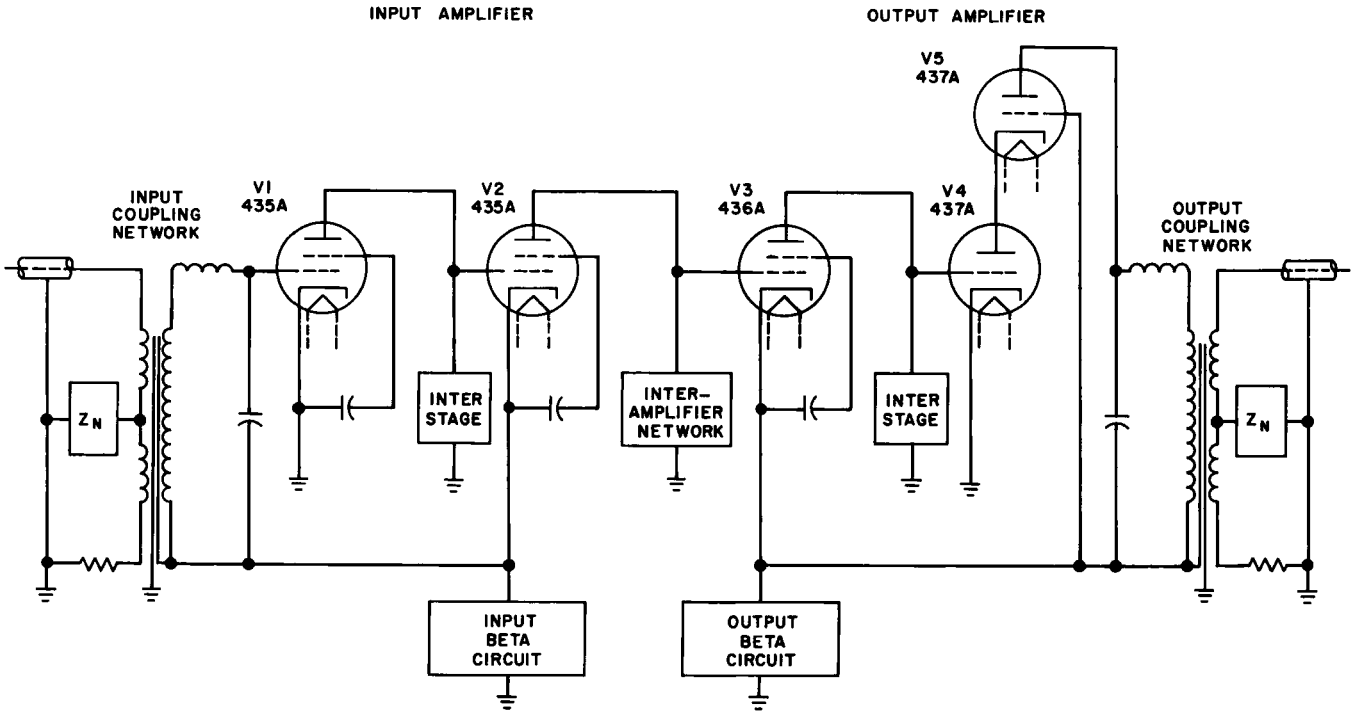


Fig. 29 — High-Frequency Amplifier, Basic Configuration

4.94 The entire amplifier assembly is housed in a sealed, die-cast container designed to protect the components from humidity damage. The housed unit is arranged for mounting, by means of self-locking slides, on a relay rack panel. Signal and power connections are made by means of flexible plug-ended cords on the connecting panel which plug into the unit after it is in place on the slides. Additional information covering the high-frequency amplifier is given in Section 359-010-110.

4.95 The connecting panel on which the amplifier is mounted contains two transformers for supplying 6.2-volt heater power for the tubes. Each transformer includes a thermistor network to compensate for secondary voltage variations caused by changes in ambient temperature. The connecting unit also contains a 423C gas regulator tube connected as a voltage divider. It provides a +100 volt potential which is used as a source of bias in the amplifier.

I. Low-Pass Video and Vestigial Sideband Filter (556A)

4.96 The 556A filter panel contains two filters, one of which is the low-pass video filter connected at the input to the transmitting terminal and the other the vestigial sideband filter connected at the output of the modulator. (See Fig. 14.)

4.97 The low-pass video filter limits the bandwidth of the video input signal to the frequencies between zero and 4.2 mc. It prevents certain unwanted modulation products from appearing in the output of the modulator and also prevents direct transmission through the modulator of energy above 4.2 mc. The filter is a balanced structure with an input impedance of 124 ohms. It includes a 6-db balanced pad which matches the filter output to the 124-ohm input impedance of the clipper circuit. Fig. 30 shows the loss-versus-frequency characteristic of the filter between zero and 4.2 mc and includes the attenuation provided by the 6-db matching pad. At frequencies between 4.8 and 20 mc, the loss is over 50 db. At frequencies between zero and 4.2 mc, the increase in attenuation with increasing frequency is compensated by a decrease in attenuation at corresponding modulated frequencies in the vestigial sideband filter.

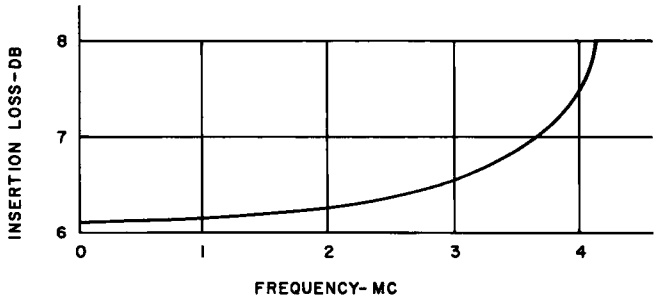


Fig. 30 — 556A Filter, Video Low-Pass Section, Loss-Versus-Frequency Characteristic (Including Loss Provided by 6-DB Matching Pad)

4.98 The vestigial filter passes the upper sideband and a portion of the lower sideband of the modulator output. At frequencies below 3.7 mc, the vestigial filter offers 60 db of discrimination in order to prevent interference with telephone channels during line transmission. Fig. 31 shows the equivalent loss-versus-frequency characteristic of the transmission band at the output of the vestigial filter. The overall characteristic is that of the vestigial filter combined with that of the low-pass video filter. The figure does not include the loss provided by the 6-db matching pad in the low-pass filter. As shown, the

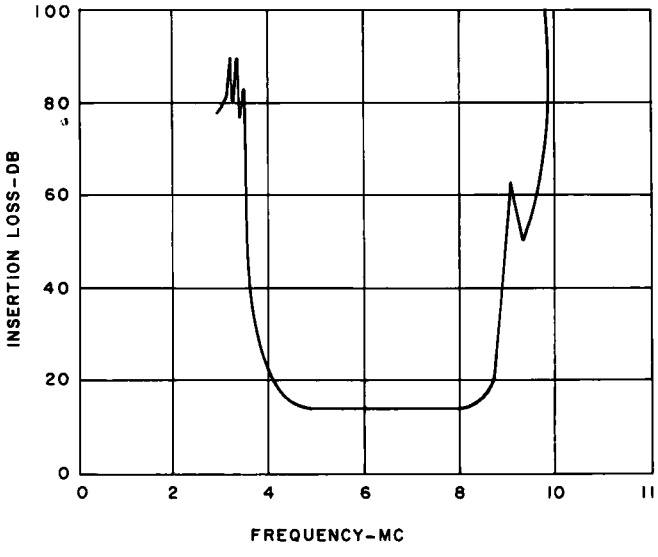


Fig. 31 — 556A Filter, Equivalent Loss-Versus-Frequency Characteristic (Excluding Loss Provided by 6-DB Matching Pad)

transmission characteristic is flat from approximately 4.6 mc to 8.3 mc but falls off rapidly on either side. Fig. 32 is an expanded presentation showing the loss-versus-frequency characteristic of the vestigial filter in the region of the carrier. The ordinate scale is given in relative amplitude with the zero transmission level point having a unit value of 1.0. As shown in the figure, the response function is symmetrical about the carrier frequency but increases and decreases linearly for corresponding frequencies above and below the carrier. The point at which the relative amplitude is zero represents the lower limit of the transmission band of frequencies. The carrier frequency is located at the half-value point with respect to zero transmission level. This particular characteristic is essential to obtaining a distortionless output in the detection process.

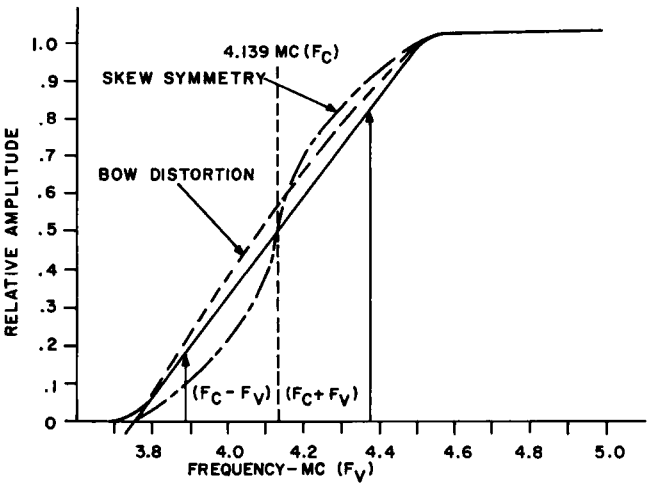


Fig. 32 — 556A Filter, Loss-Versus-Frequency Characteristic of Vestigial Sideband Filter, Expanded Presentation in Carrier Region

4.99 Fig. 32 shows two ordinates, designated ($F_C - F_V$) and ($F_C + F_V$), which are the lower and upper sidebands, respectively. The demodulator will detect energy at the sidebands ($F_C - F_V$) and ($F_C + F_V$) and the two component voltages will add in the output. If the vestigial characteristic is linear and passes through the 0.5 point at the carrier F_C, the sum of the voltages at ($F_C - F_V$) and ($F_C + F_V$) will add to a relative amplitude of 1.0 for all values of F_V. The same situation prevails if there is odd, or skew, symmetry about the carrier since the ordinate at ($F_C - F_V$) is shortened while the ordinate at ($F_C + F_V$) is lengthened, and the sum of the two ordinates will remain 1.0. Bow distortion, or even symmetry, about the carrier causes the ($F_C - F_V$) and ($F_C + F_V$) ordinates of the sidebands to be either both shortened or both lengthened as shown in Fig. 32. Hence, the sum of the ordinates will differ from 1.0, resulting in a low-frequency transmission characteristic that is not flat. This is the cause of smear distortion. The variations which result in even or odd symmetry are caused primarily by element tolerances and element deviations in the vestigial filter. These variations are corrected by means of variable equalizers electrically located in the carrier section near the output of the terminal. (See Fig. 14.)

4.100 Delay distortion, which is introduced by the filters in the 556A panel, is corrected by means of 25 delay equalizer sections included in the panel.

J. Pilot Elimination Filter (542B)

4.101 The 542B filter is a 2-section narrowband elimination filter modified per SD-50001-01 to utilize only one filter section. When the filter is used in a transmitting terminal, the unmodified section removes two narrow bands of energy from the television signal to permit insertion of the two L3 line pilot signals. When the filter is used in the receiving terminal, the unmodified section suppresses the two L3 line pilot signals to prevent interference with the demodulated signal. At L3 terminal stations, the arrangement is somewhat different; a modified 542B pilot elimination filter is located in the connecting facilities and a pad is provided in the receiving terminal.

4.102 The 542B pilot elimination filter is designed to operate between unbalanced 75-ohm impedances. Fig. 33 is a simplified schematic diagram of the modified filter. As shown by x's, the quartz crystals in one section are dis-

connected from their associated components to disable the section. Trimmer capacitors are provided in series with each of the crystals so that the filter can be adjusted for maximum loss at the two pilot frequencies. Only the two trimmers in the unmodified section need be adjusted. The nominal flat loss of the filter is 5.7 db. Thermistor-controlled ovens on the filter panel maintain close temperature control for the crystal elements in order to stabilize the resonant frequencies of the filter.

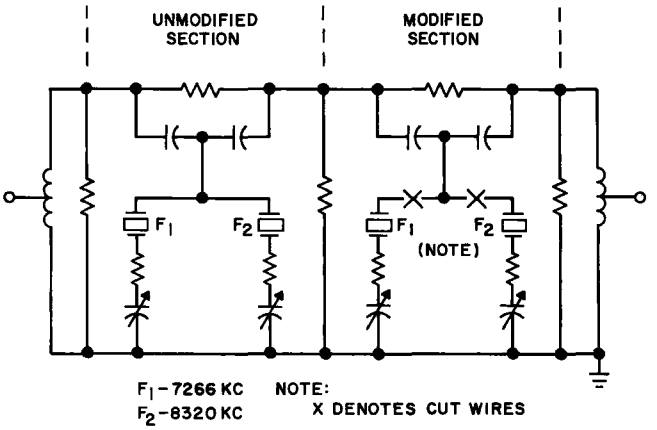


Fig. 33 — Modified 542B Filter, Simplified Schematic Diagram

K. Equalizers (328A, 226J, 226K, and 226L)

4.103 Four equalizers are provided in the transmitting terminal to compensate for residual variation in the frequency characteristic. The fixed 328A equalizer compensates for nominal deviation. Its loss is 1 db at 4.139 mc, but decreases uniformly to 0.6 db at 8 mc. The variable 226J and 226K equalizers provide compensation for bow distortion in the vestigial region. The 226L equalizer is also variable, and is provided to compensate for broadband deviations which are likely to occur in high-frequency amplifiers. Fig. 34 and 35 show the loss-versus-frequency characteristics of the four filters.

4.104 The 226J, K, and L equalizers are adjusted to obtain a minimum deviation from the ideal response function. The actual response characteristics of the transmitting terminal are determined by applying sine waves at specific frequencies and levels to the input of the terminal, then measuring the response after frequency translation. The response can be measured directly at the output of the transmitting terminal and the equalizers adjusted to obtain certain requirements. A more convenient method, when practical, employs a receiving terminal connected back-to-back with the transmitting terminal under test. In this case, the equalizers are adjusted to obtain a flat response over the entire video band of frequencies measured at the output of the receiving terminal. When the latter method is employed, it is essential that the connections between the two terminals be flat and that the receiving terminal be properly aligned prior to making the measurements.

4.105 The 226L equalizer is adjusted first to obtain a minimum deviation in the broadband response of the terminal. The desired transmission characteristic is obtained by measuring the response of the terminal at a 900-kc reference frequency, supplied at a specified level at the input to the terminal, then adjusting the 226L equalizer to obtain the same response to a 3.6-mc signal also supplied at the input to the terminal.

4.106 A reference frequency of 900 kc is employed because this frequency, when translated into the L3 television band, falls at a null point (5.039 mc) on the characteristic curves of the 226J and 226K equalizers. Thus the settings of these two equalizers, whether correct or not, do not affect the response of the terminal at 900 kc. The 3.6-mc signal is employed because this frequency, when translated, falls in the upper end of the transmission band near the color burst frequency.

4.107 The 226J equalizer is adjusted to obtain with respect to the 900-kc reference frequency, a specified response at an input frequency of 250 kc. If measurements are made using terminals connected back-to-back, the equalizer is adjusted to make the response at 250 kc equal to that obtained at 900 kc.

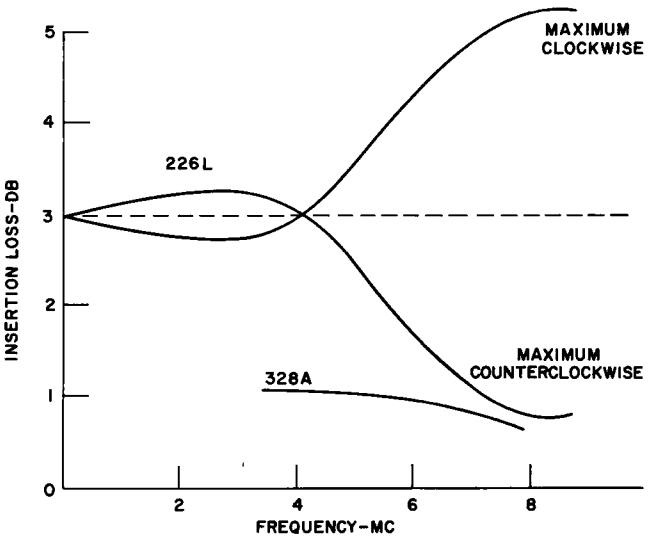


Fig. 34 — 226L and 328A Equalizers, Loss-Versus-Frequency Characteristic Curves

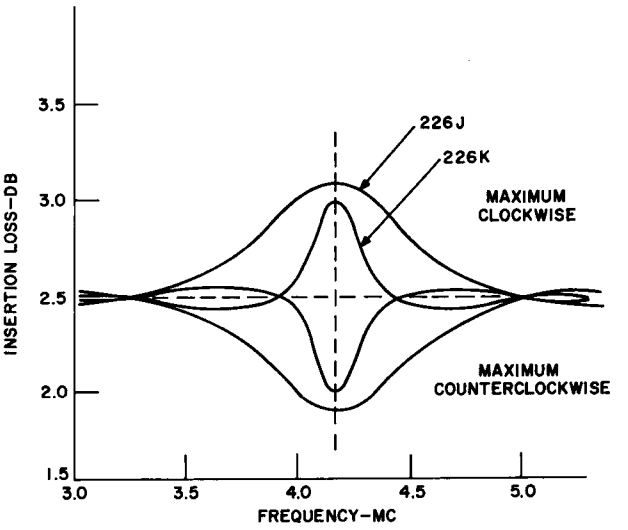


Fig. 35 — 226J and 226K Equalizers, Loss-Versus-Frequency Characteristic Curves

4.108 A 250-kc input signal is employed because this frequency, when translated, also falls at a null point (4.389 mc) on the characteristic curve of the 226K equalizer, and the particular settings of this equalizer will not affect the response of the terminal at either of the two frequencies (250 kc and 900 kc).

4.109 The 226K equalizer is adjusted to obtain a minimum deviation from a specified value at 50 kc with respect to the reference frequency. If back-to-back measurements are made rather than measurements made at the output of the transmitting terminal, the equalizer is adjusted to make the response (at the output of the receiving terminal) equal to that obtained at the reference frequency. Adjustment of the 226K equalizer reduces a residual deviation which remains after adjusting the 226J equalizer.

5. RECEIVING TERMINAL EQUIPMENT

A. General

5.01 The receiving terminal equipment, shown in Fig. 15, consists of several units and components which are either identical or similar (depending on strapping or optional connection arrangements) to some of the units used in the transmitting terminal and which have previously been described. These units, and the paragraphs in which they are described, are: the video amplifier (Part 4C), the carrier supply circuit (Part 4F), the carrier harmonic supply circuit (Part 4G), the high-frequency amplifier (Part 4H), and the pilot elimination filter (Part 4J).

5.02 The remaining units, with the exception of ac and dc power equipment, are covered in the following paragraphs. These units are: the demodulator, the carrier frequency control circuit, the polarizer, the equalizers, and the carrier suppression and low-pass filter. The descriptions covering power equipment are given in Part 6, Power Supply Arrangements.

B. Demodulator

5.03 The demodulator circuit in the receiving terminal translates the vestigial sideband signal in the 3.64- to 8.34-mc range to a video signal in the 0- to 4.2-mc range. The translation is accomplished in the same manner as in the modulator circuit in the transmitting terminal. Basically, the modulator and demodulator circuits are identical with differences existing primarily in their balancing circuits. With modification, the two units could be used interchangeably by reversing their input and output connections. Fig. 36 is a simplified schematic diagram of the demodulator circuit.

5.04 The modulator circuit in the transmitting terminal is provided with a control (CARR BAL 2) for balancing the quadrature carrier component from the output. This control, however, introduces a quadrature video signal leak which is balanced out by means of the SIG BAL 2 control. The demodulator circuit does not require a quadrature balance control, since the carrier separation filter following the demodulator provides a peak loss at 4.139 mc. Because there is no need for a quadrature carrier balance control, there is no need for a quadrature video balance control, and neither of these is provided.

5.05 The controls which are provided, however, are dc controls required for compensation of unbalances in the demodulator circuitry, and particularly in the varistor lattice. These are the SIG BAL and CARR BAL controls shown in Fig. 36.

5.06 The dc signal balancing voltage is introduced across the carrier side of varistor lattice CR1 and is adjusted, by means of SIG BAL control R14, to produce a minimum vestigial sideband signal voltage in the output of the demodulator. This control is also effective in reducing a distortion component equal to twice the carrier frequency minus the frequency components in the vestigial sideband signal. This component corresponds to the $2C - V$ term that is present in the modulator. As in the modulator, the best setting of the SIG BAL control is a compromise between the balance minima.

5.07 The dc carrier balancing voltage is introduced across the signal side of the lattice and is adjusted by means of variable CARR BAL control R15. This control is set to provide maximum suppression of the locally generated 4.139-mc carrier.

5.08 The demodulator includes another control which permits suppression of a longitudinal carrier voltage from the balanced output. This control is designated LONG CARR BAL, as shown in Fig. 36. Unless the longitudinal carrier voltage is suppressed, unbalances in the 124-ohm circuits following the demodulator can convert this voltage to a metallic voltage which would appear in the terminal output.

5.09 The third harmonic distortion term that occurs during the modulation process also occurs in the demodulation process. This term, described as $3C - V$, is suppressed in the demodulator in exactly the same manner as in the modulator. The vestigial sideband signal is supplied via hybrid T5 to Demod 2, where it is demodulated with a 12.417-mc carrier. The lower sideband output from Demod 2 is then supplied to the resistance hybrid in an out-of-phase relationship to the unwanted $3C - V$ term (where V in the demodulator represents the vestigial sideband frequency components) developed in Demod 1. Cancellation occurs in the resistance hybrid, and only the desired 0- to 4.2-mc video signal is coupled out of the hybrid.

C. Carrier Frequency Control Circuit

5.10 The carrier frequency control circuit is used at the receiving terminal to lock the locally generated carrier in phase with the incoming modulated carrier.

5.11 A portion of the received signal and a portion of the locally generated carrier are supplied to the control circuit. A dc voltage is derived from these two inputs, depending on the phase difference between them, and applied at the grids of a balanced dc amplifier. Plate power for the amplifier is supplied via the center-tapped control winding of a saturable reactor in the carrier supply circuit.

5.12 The saturable reactor is part of the series resonant quartz crystal circuit. Its reactor winding functions as a tuning element whose inductance, in series with the crystal, varies as the degree of saturation of the reactor core varies. As the phase between the two signals supplied to the carrier frequency control circuit differs, the amount of current drawn through each half of the control winding differs to change the degree of saturation of the reactor core. The carrier frequency control circuit therefore maintains the oscillator synchronous in both frequency and phase with the incoming carrier.

5.13 Synchronization of the locally generated carrier with the carrier component of the received signal is dependent on information contained in the received signal itself. Determination

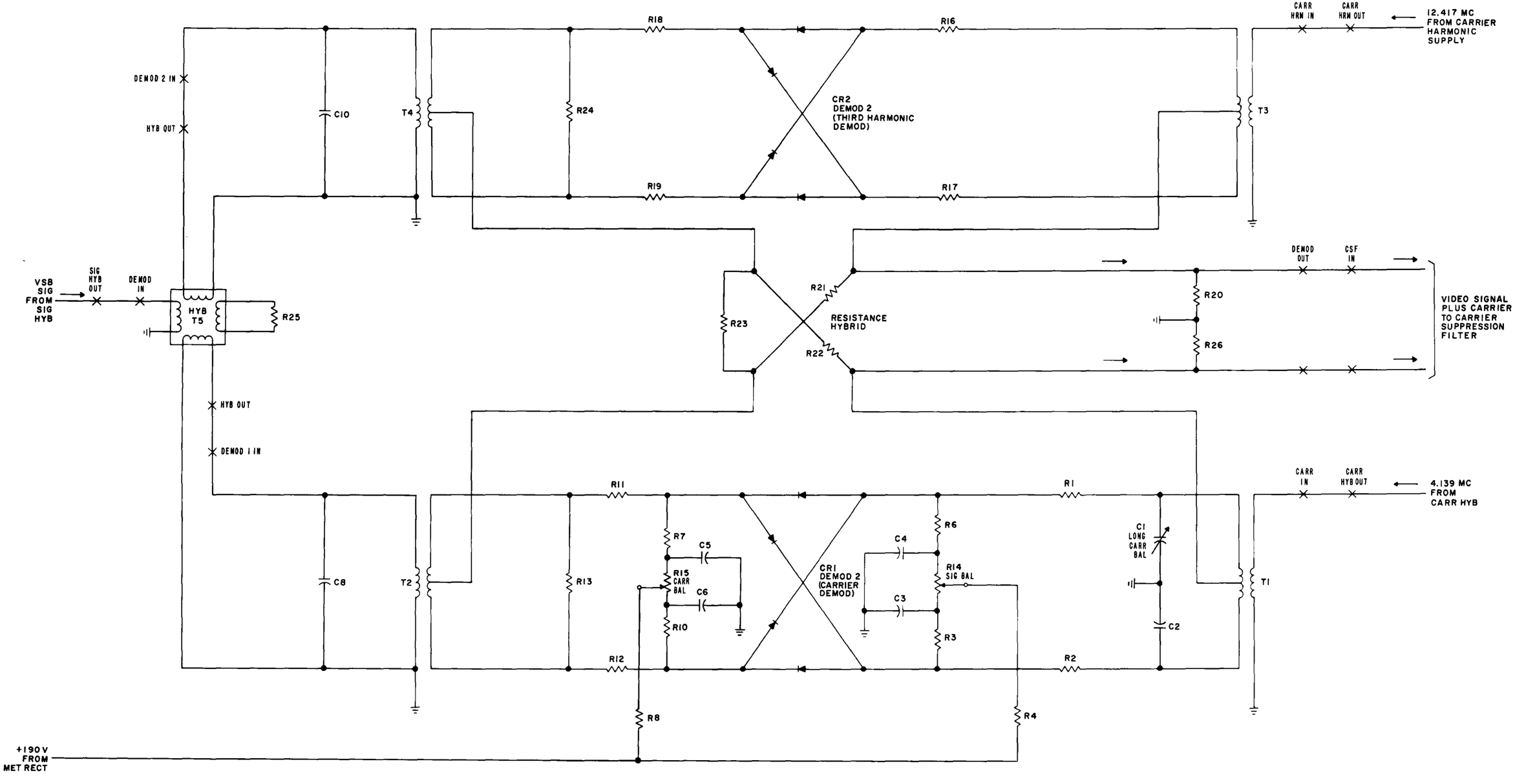


Fig. 36 — Demodulator Circuit, Simplified Schematic Diagram

of the phase angle of the carrier-frequency component averaged over a period of time (of the order of one frame scanning period), makes possible close duplication of the phase angle of the locally generated carrier. With reference to Fig. 11, the quadrature response function is zero at the carrier frequency and therefore will not affect the determination of the real carrier component phase angle (based on averaging over a sufficient period of time). Only the real component is essential to the process, and for practical purposes the quadrature component can be ignored. However, another characteristic of the vestigial sideband signal makes the average carrier polarity of the real component indeterminate. With reference to Fig. 8, the carrier executes 180° reversals in polarity for amplitudes which exceed the degree of modulation referred to as 100 percent. In video transmission, these instantaneous polarity reversals occur as the composite signal changes through its half peak-to-peak value: i.e., the average polarity determined from a predominantly white picture is opposite to that of a predominantly black picture. Unless otherwise prevented, the locally generated carrier would lock up either in phase or out of phase with the incoming carrier (depending on the instantaneous phase), and instantaneous reversals in picture polarity would occur. The ambiguity is eliminated in the carrier frequency control circuit by squaring the modulated signal, i.e., by multiplying the signal by itself on an instantaneous basis in a square law circuit. Such an operation squares the carrier amplitude, and doubles carrier frequency and phase angle, the latter of which converts the instantaneous 180° reversals into 360° changes. Since 360° changes are indeterminate in an average-phase detector, the oscillator in the carrier supply circuit will lock to the average phase of the squared signal, and instantaneous reversals in picture polarity cannot occur. The squaring operation, however, eliminates any basis for determining the original carrier polarity. As a consequence, the polarity to which the oscillator locks (and remains stably locked) can be of either polarity relative to the signal. The actual polarity to which the oscillator locks is immaterial, since a polarizer circuit following the demodulator recognizes the polarity of the video waveform independent of picture content. The polarizer functions to correct the polarity of the video signal whenever it becomes inverted.

5.14 Fig. 37 is a functional block diagram of the carrier frequency control circuit and associated units. The received vestigial sideband signal is split by the signal hybrid so that part is supplied to the demodulator and part through the OPR patching plugs and a low-pass filter to the signal branch of the carrier frequency control circuit. The signal is squared, then supplied through a tuned amplifier to one of two inputs to the phase comparison circuit. The tuned amplifier provides effective isolation between the signal squarer and the phase comparison circuit.

5.15 Because of the necessity for squaring the received modulated signal, it is also necessary to square the locally generated carrier. The locally generated carrier is split by the carrier hybrid, part of which is supplied to the demodulator and part through a variable phase shifter and splitting network (AT4) to the carrier branch of the control circuit. A phase shift network in the carrier frequency control circuit then shifts the carrier phase in preparation to the squaring, amplification, and detection process. As in the signal branch, a tuned amplifier provides effective isolation between the carrier squarer and the input to the phase comparison circuit. Although Fig. 37 shows only relative phase differences in the signal and carrier branches, there is an inherent phase shift of 23° in the carrier path at the input to the control circuit. The phase shift network in the control circuit therefore provides 22° of phase shift in order to obtain the required 45° shift ahead of the carrier squarer. The phase shift network also provides 18° (in addition to the 22°) to compensate for an 18° phase shift in the signal path (introduced by the LPF). The net phase differences, however, are as shown in the figure.

5.16 The phase comparison circuit utilizes the properties of a product modulator to obtain a measure of phase difference between two inputs. This type of circuit produces a dc component in its output for input signals differing in phase by other than 90° but produces no dc component for input signals exactly 90° apart. When no phase difference exists between the locally generated carrier and the incoming carrier, the phase difference between the two inputs to the phase comparison circuit will differ by exactly 90°, and no dc component will appear in the output. If a phase difference exists between the two

inputs to the control circuit, a phase difference of 90° plus or minus the actual phase difference will exist at the input to the phase comparison circuit. A dc component, which is proportional to the actual phase difference between the two inputs to the control circuit, will appear in the output. Since the carrier squarer doubles both frequency and phase, the required 90° relationship between the two inputs to the phase comparison circuit is obtained by providing a phase shift of 45° ahead of the carrier squarer.

5.17 The dc component, when present in the output of the phase comparison circuit, is supplied through a filter to the grids of a balanced dc amplifier. As the grid voltage changes in proportion to changes in phase between the locally generated carrier and the incoming signal, the dc plate current also changes. Since the amplifier draws its plate current through the control winding of the saturable reactor in the carrier supply circuit, any change in plate current will result in a change in oscillator frequency. The filter between the phase comparison circuit and the dc amplifier attenuates ac components which are present as a result of the sideband components in the received modulated signal. The filter prevents frequency modulation of the locally generated carrier.

5.18 Because of an inherent phase difference in the signal paths between the demodulator and the control circuit, it is essential that the same relative phase difference also exists in the carrier paths. If a 0° relationship between signal and carrier inputs to the demodulator does not exist, even though a synchronous condition is preserved between the two inputs to the control circuit, distortion of the demodulated video signal will occur. Variable phase shifter AT4, shown in Fig. 37, provides the means for equalizing the relative phase differences. Its adjustment is dependent on the properties of the demodulator to produce a ***maximum real output*** when supplied with signal and carrier voltages exactly in phase, but to produce a ***minimum real output*** when supplied with signal and carrier voltages 90° apart. In practice, the locally generated carrier is deliberately shifted by 90° (relative to the received signal), then the variable phase shifter is adjusted to produce a minimum real output from the demodulator.

5.19 The 90-degree shift in carrier frequency is obtained by means of the QUAD TST key on the branching and control panel. The QUAD TST button, when operated and held operated, reverses the connections between the dc amplifier (in the carrier frequency control circuit) and the control winding of the saturable reactor (in the carrier supply circuit). The reversal in control winding connections causes the oscillator phase to shift, but only by 90° since a 90° shift at the input to the control circuit, when squared, results in a subsequent 180° shift following the squarer. As previously described, 180° reversals in phase are indeterminate in the phase comparison circuit, and for practical purposes the control circuit recognizes a 90° difference between its two inputs as a synchronous condition. The variable phase shifter can then be adjusted for minimum video output while the QUAD TST button is pressed. A normal in-phase relationship between the carrier and signal inputs to the demodulator will result when the button is released. This operation ensures that the phase difference in the carrier paths is related to the inherent phase difference between signal paths.

5.20 The splitting network, and the jack and patching arrangement designated OPR, TST 1, and TST 2, are provided to obtain a measure of sensitivity of the carrier frequency control circuit. When the patch plugs, located on the branching and control panel, are arranged for the OPR condition, the received signal is supplied through the low-pass filter to the signal branch of the control circuit. The locally generated carrier is divided in the splitting network, part of which is supplied to the carrier branch of the control circuit and part of which is terminated. Normal operation of the terminal is provided. However, when the patch plugs are arranged for the TST 1 condition, the termination is removed from the splitting pad and the received signal is terminated instead. The locally generated carrier divides in the splitting pad, part of which is supplied in the normal manner to the carrier branch of the control circuit while part is supplied, via the TST 1 plug, through the low-pass filter to the signal branch of the control circuit. With this arrangement, both inputs to the control circuit are in phase and a zero indication on the frequency meter, shown in Fig. 37, will be

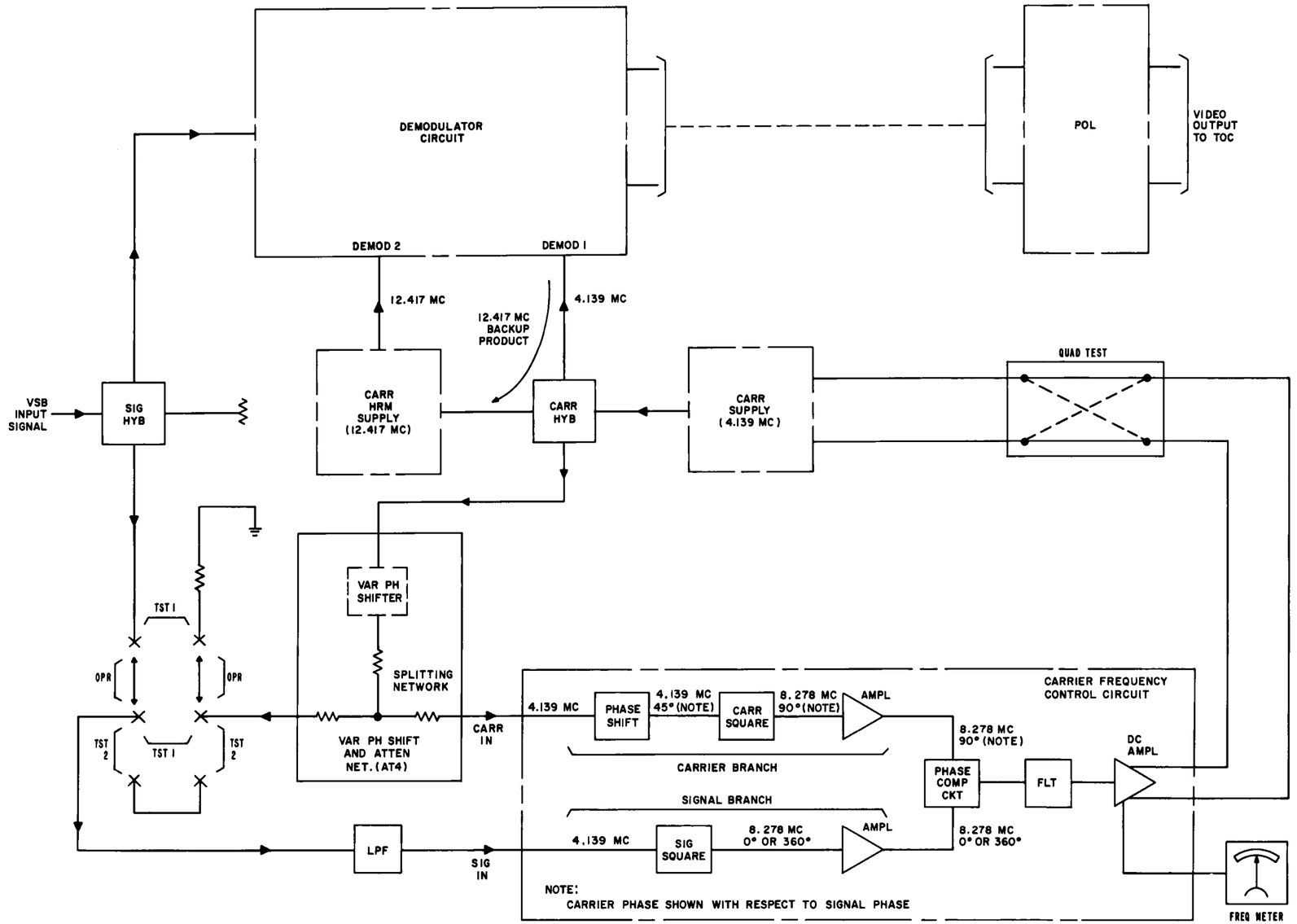


Fig. 37 — Carrier Frequency Control Circuit and Associated Units, Block Diagram

obtained. The frequency meter is located on the branching and control panel and is calibrated in cycles.

5.21 With the patch plugs arranged for the TST 2 condition, about 1.5° of phase shift is introduced into the signal branch relative to that of the carrier branch. The phase shift occurs because the electrical length of the signal path is increased by the addition of a patch plug, two jacks, and the short wire strap connecting the center contacts of the two jacks. The 1.5° phase shift at the particular levels of the two inputs is related to a change of about 20 cycles indicated on the frequency meter. The change in the indication on the frequency meter when the patch plugs are changed from the TST 1 to TST 2 condition provides a relative measurement of the overall loop feedback (or stiffness of control). At normal operating levels, a frequency deviation of 20 cycles corresponds to a much smaller phase error.

5.22 Fig. 38 is a simplified schematic diagram of the carrier frequency control circuit. The signal squarer is comprised of tubes V1 and V2 and associated components. The signal supplied from the signal hybrid is converted from unbalanced to balanced by means of transformer T1, and then supplied to the control and suppressor grids of each tube in the balanced squarer circuit. The plate current flow in each tube, which changes as the control grid signal voltage changes, is further acted upon by the signal voltage on the suppressor grid. The resulting plate current flow is therefore a function of the product of the control and suppressor grid signal voltages. Since the signal on the suppressor grid is equal in amplitude to the signal on the control grid, the output amplitude is a function of the square of the individual input signals to the tube. Further squaring action results from the nonlinearity of the grid-voltage plate-current characteristic of the tubes: i.e., each of the squarer tubes, V1 and V2, utilizes a limited portion of the tube characteristic curve which approximates a portion of a parabola. The behavior of each tube therefore follows that of a power-law device.

5.23 It is the nature of a power-law device to produce different-order components in the plate current. The first-order component of the plate current represents undistorted output of the input signal waveshape, while the second-, third-, and higher-order components of the plate current are related to the curvature of the characteristic curves of the tube at the operating point. Since the desired output is the second harmonic of the carrier frequency, the circuit is designed to enhance second-order behavior. The plate current also includes undesired components which are harmonic and sum and difference frequencies and combinations of these frequencies resulting from the squaring action. These undesired components are suppressed by a low-pass filter, following the phase comparison circuit, which prevents frequency modulation of the locally generated carrier.

5.24 The signal squarer is operated as a balanced push-push circuit (a circuit in which the input to the balanced tubes is effectively in series and the output in parallel). This type of circuit has the property of adding the even-order terms in the output while cancelling odd-order terms. Optimum cancellation of these odd-order terms occurs when they are equal in amplitude but opposite in phase. SIG BAL potentiometer R93 in the cathode circuit of V2 provides a means for adjusting the transconductance of V2 against that of V1 in order to obtain a condition of optimum balance, particularly at 4.139 mc.

5.25 Both tubes in the signal squarer are operated with considerable dc feedback to stabilize the circuit against supply voltage variations. Any change in potential appearing at the plate and screen is reflected as a proportional change in dc potential at the control grid. This feedback exaggerates that which is normally provided by self-bias, and enables the circuit to function almost independently of supply voltage variations. The grids are held at a 60-volt positive potential determined by a voltage divider comprised of resistors R1 and R2. The operating bias for V1 is determined by cathode resistors R4 and R5, and for V2 by cathode resistors R9 and R10 and SIG BAL potentiometer R93. Capacitors C2 and C4 couple the input signal to the suppressor grids while blocking the 60-volt positive potential that is present on the control grids. Bias for the V1 suppressor grid is supplied through resistor R6, connected at the junction of cathode resistors R4 and R5. Bias for the V2 suppressor grid is supplied through resistor R11, connected at the junction of cathode resistor R10 and SIG BAL potentiometer R93. The cathodes are bypassed at the carrier and higher frequencies by capacitors C3 and C5.

5.26 The plate load for V1 and V2 is comprised of network Z2 which consists of tunable inductor L1; fixed resistors R16 and R17; and fixed capacitors C6 and C7. Inductor L1 resonates with capacitor C7 and the parasitic interstage capacity at the second harmonic of the received carrier frequency (8.278 mc). Since phase instability would result in phase error of the locally generated carrier, which in turn would cause video distortion in the demodulator output, the phase shift must remain fixed. Resistor R16 stabilizes the circuit by damping the resonant portion of the network. The Q is therefore low, and hence tuning is broad.

5.27 The signal at the output of the squarer is coupled via capacitor C8 in network Z2 to the control grid of amplifier V6. Resistor R17, located in network Z2, and grid return resistor R18 form a voltage divider which supplies a 9-volt positive potential to the grid. Cathode resistors R76 and R20 establish the correct operating bias. The dc feedback thus provided helps stabilize the tube against supply voltage variations. Resistor R76 provides about 2 db of local feedback, which helps reduce the effects of a varying tube input capacitance. The effect occurs as varying grid bias varies the plate current, which in turn causes the position of the space charge surrounding the cathode to vary. This variation changes the effective grid-to-cathode capacity of the tube and would result in phase shift if feedback were not provided. Capacitor C9 bypasses resistor R20 at high frequencies.

5.28 Network Z3 forms the plate load for amplifier V6 and consists of tunable inductor L3 in parallel with capacitor C11. The network is similar to network Z2 except that damping is provided by the circuitry which follows, and no additional damping is required.

5.29 Except for reference designations of the components, the carrier squarer (V7 and V8) is identical to the signal squarer. However, a 45° phase-shift network (Z5) is included ahead of the unbalanced-to-balanced input transformer (T3). This network provides 22° of phase shift which, when added to an inherent 23° phase shift in the carrier path, results in a 45° phase shift at the input to T3. Since the squarer doubles the phase, a 90° shift in phase relative to that of the locally generated carrier will appear in the output. The output of the carrier squarer is coupled to amplifier tube V9, which functions in the same manner as V6. The output of V9 is coupled via transformer T2 to the phase comparison circuit. The transformer is tuned on the primary side by variable capacitor C42, fixed capacitor C44, and variable PHASE BAL capacitor C46. Resistor R89 forms part of the plate load on the primary side, while resistors R90 and R91 form part of the load on the secondary side. Capacitor C42 is located on the wiring side of the panel and provides a coarse phase-balance adjustment. It is set at the factory to obtain a phase balance with the PHASE BAL control C46 set to its median position. The PHASE BAL control is located on the front panel and provides a means for tuning the stage to 8.278 mc. When properly adjusted, it equalizes the phase shifts in the carrier and signal paths between the inputs of the squarers and the inputs to the phase comparison circuit.

5.30 The phase comparison circuit utilizes both sections of a dual triode tube (V4) connected as a product modulator. The squared carrier input is supplied as a balanced voltage between the two grids, and the squared signal input voltage is supplied between the common cathodes and ground. A product modulator, when properly balanced, has the property of delivering no dc output for inputs of the same frequency but differing in phase by exactly 90° (relative to each other). A dc output will be produced if one or the other of the two inputs deviates from this quadrature relationship, the dc being proportional to the magnitude of the deviation.

5.31 A balance between the plate currents in the two sections of V4 is obtained by means of MOD BAL R potentiometer R93. This control and resistors R64 and R65 form a bridge circuit connected between the plate supply and ground through resistors R63 and R66. The arrangement is such that the ratio of resistance on each side of the bridge can be varied inversely with the setting of the control. The inverse relationship of the voltage supplied to each grid permits a dynamic balance of plate current in each half of V4. The grids are operated at approximately 15 volts positive in order that dc feedback through cathode resistor R67 can be provided.

5.32 Differential capacitor C43, designated MOD BAL X, provides a means for balancing the input capacities of the two sections.

When properly adjusted, the output of the circuit will be a function of only phase differences independent of amplitude.

5.33 Network Z1 contains two matched resistors that provide the means for supplying plate voltage to the phase comparison circuit. The connection to the +315 volt plate supply bus is made at the junction of the two resistors in the network. As each half of the tube draws more or less current, depending on the relative phase difference between the two inputs to the carrier frequency control circuit, the voltage change across each resistor is reflected as a dc voltage change at the grids of balanced amplifier tube V5. Attenuation of the high-frequency ac components (which are present in the output of the phase comparison circuit) is provided by the adjacent arms of one side of a bridge. Coupling to the bridge is through capacitors C33 and C34 connected at the plates of V4. Since the reactance offered by these capacitors at high frequencies is low (about 40 ohms at 8.278 mc), the high-frequency paths to ground are through capacitor C35 and resistor R71 in one arm of the bridge and capacitor C39 in the adjacent arm. High-frequency current flowing through capacitor C35 and resistor R71 develops a voltage across the resistor which is relative to the amplitudes of the two inputs to the phase comparison circuit. HF TST jack J2, connected at the junction of the capacitor and resistor, provides a means for measuring the relative voltage while tuning networks Z2, Z3, and Z4 or while adjusting the CARR BAL and SIG BAL controls.

5.34 Resistors R72 and R77 form the adjacent arms of the other side of the bridge. The junction of the two resistors is supplied with a voltage obtained from the junction of V5 cathode resistors R30 and R70. The connection is made by means of a common return path which includes the shield can of network Z1, the shield sleeve of tube V5, and the cans of capacitors C13 through C17 (which are components of a low-frequency filter). Since the voltage at the junction of resistors R70 and R30 is almost equal to the grid voltage of V5 (and the plate voltage of V4), a low potential difference exists across the plates of capacitors C33 and C34. This same low potential difference exists between the shield can of Z1 and its two resistor elements, and also between the shield cans and the plates of capacitors C13 through C17. The effect is to minimize leakage currents which would otherwise appear as unwanted voltage changes on the grids of tube V5. The common return to ground through resistor R30 also eliminates the extraneous paths which might otherwise introduce unwanted voltages at various points between the plates of tube V4 and the grids of tube V5. By returning the shield sleeve of V5 to ground through the common path, the effects that stray electrostatic fields would have on the V5 grids are eliminated.

5.35 The low-frequency ac components which are present in the output of the phase comparison circuit are attenuated by a filter connected between the plates of the phase comparison circuit and the grids of dc amplifier tube V5. The filter is comprised of resistors R23 through R29 and capacitors C13 through C17. It has a transmission characteristic which falls off at the rate of 3 db per octave between 0.11 cps and 52 cps. The filter effectively short-circuits the grids of V5 at low frequencies. Since the ac components between the plates of V4 are of opposite polarity, the effective short circuit provides a zero-potential condition between the grids. The only voltage changes that appear on the grids of V5 are dc changes resulting from a difference in phase between the signal and carrier voltages at the input to the carrier frequency control circuit.

5.36 Tubes V5 and V3 and their associated components form a high-gain balanced dc amplifier. Plate voltage for V5 is obtained from the +315 volt supply bus connected at the junction of resistors R31 and R32. Resistors R30 and R70 are bias resistors which raise the cathode potential on V5 to a value slightly higher than the voltage (approximately +185 volts) on the control grids. The plate current changes of V5 are reflected as voltage changes across resistor combinations R33-R34 and R35-R36. The resistor combinations act as voltage dividers to reduce the dc voltage on the grids of V3, since the plates of V3 are also operated at +315 volts. The voltages on the grids of V3 are proportional to the voltages across the resistor combinations. Any changes at the grids of V5 are therefore reflected as a current change in the control winding of the saturable reactor in the carrier supply circuit. Bias for the two cathodes of V3 is produced as a

result of the combined cathode currents flowing through resistor R37 and the separate currents flowing through resistors R38 and R39. The separate currents flowing through resistors R38 and R39 develop a voltage difference between the cathodes which is supplied via build-out resistors R87 and R88 to a frequency meter on the branching and control panel. When the current flow in each half of tube V3 is equal, the voltage difference between the cathodes is zero and the indication produced on the frequency meter will be zero. This equal-current condition corresponds to a synchronous condition between the received carrier frequency and the locally generated carrier frequency, although it is possible that the two frequencies will be out of phase by 180°. This out-of-phase condition is of no significant consequence, since the polarizer circuit following the demodulator is capable of recognizing and correcting polarity inversions.

5.37 Jack J1, designated AC BAL TST, provides a means for measuring the ac output caused by a capacity imbalance at the input of tube V4. The jack is connected at the junction of inductor L5 and capacitor C40, which form a network tuned to 5 kc. The network is connected to one of the plates of dc amplifier tube V3. In practice, the capacity-balance adjustment is made, after disconnecting the signal input section, by combining in the carrier hybrid a 4.139-mc signal and a signal 5 kc away from 4.139 mc, and applying the combined signal to the carrier input section of the carrier frequency control circuit. The combined signal has the appearance of an amplitude-modulated carrier with a 5-kc envelope frequency. The 5-kc envelope is detected in the phase comparison circuit and transmitted through the dc amplifiers to the 5-kc tuned circuit. The MOD BAL X capacitor is then adjusted to produce a minimum voltage indication on a voltmeter connected to the AC BAL TST jack. A minimum voltmeter indication (approximately 0.04 volt or less) corresponds to a capacity balance at the grids of V4.

D. Polarizer

5.38 The function of the polarizer circuit is to maintain the correct polarity of the television signal at the output of the receiving terminal. Sensing circuits in the polarizer recognize the polarity of a standard television signal and cause a polarity reversing relay to operate whenever the polarity of the signal is incorrect. The polarizer does not recognize the polarity of nonstandard signals, such as sine waves and certain other kinds of test signals, but maintains the same polarity established for the previous standard signal.

5.39 The polarizer is required because the locally generated carrier supplied to the demodulator, although synchronous in frequency, can be either in phase (0°) or out of phase (180°) with respect to the received carrier frequency. The ambiguity occurs as a result of the squaring operation in the carrier frequency control circuit. (See 5.13.)

5.40 A functional block diagram of the polarizer circuit is shown in Fig. 39. Relays K1 and K3 constitute a relay oscillator that functions only when relay K2 is operated. The oscillator is bi-stable if relay K2 is released: i.e., relays K1 and K3 can be either operated or released, and the circuit will remain in that condition until relay K2 operates.

5.41 Relay K4 is a lockout relay which, when operated, shunts the winding of relay K2 and prevents its operation. Relays K2 and K4 are in the plate circuits of two modulator tubes and will operate whenever the tubes conduct through their associated relay windings.

5.42 As shown in Fig. 39, a balanced television signal is connected through the contacts of polarity reversing relay K1 to the video amplifiers of two separate sensing circuits. The modulator tube in the output of each sensing circuit either conducts or cuts off according to information derived from the video signal.

5.43 When the polarity of a standard video signal at the output of the receiving terminal is correct, modulator 2 conducts while modulator 1 is cut off. Under these conditions, relay K4 is operated while relay K2 is released. When the polarity at the output of the terminal becomes inverted, modulator 2 cuts off, releasing relay K4, while modulator 1 conducts, causing relay K2 to operate. This is the condition that causes relays K1 and K3 to oscillate. After the first half-cycle, however, the polarity is corrected. Modulator 1 then cuts off, releasing relay K2, while modulator 2 again conducts and operates relay K4.

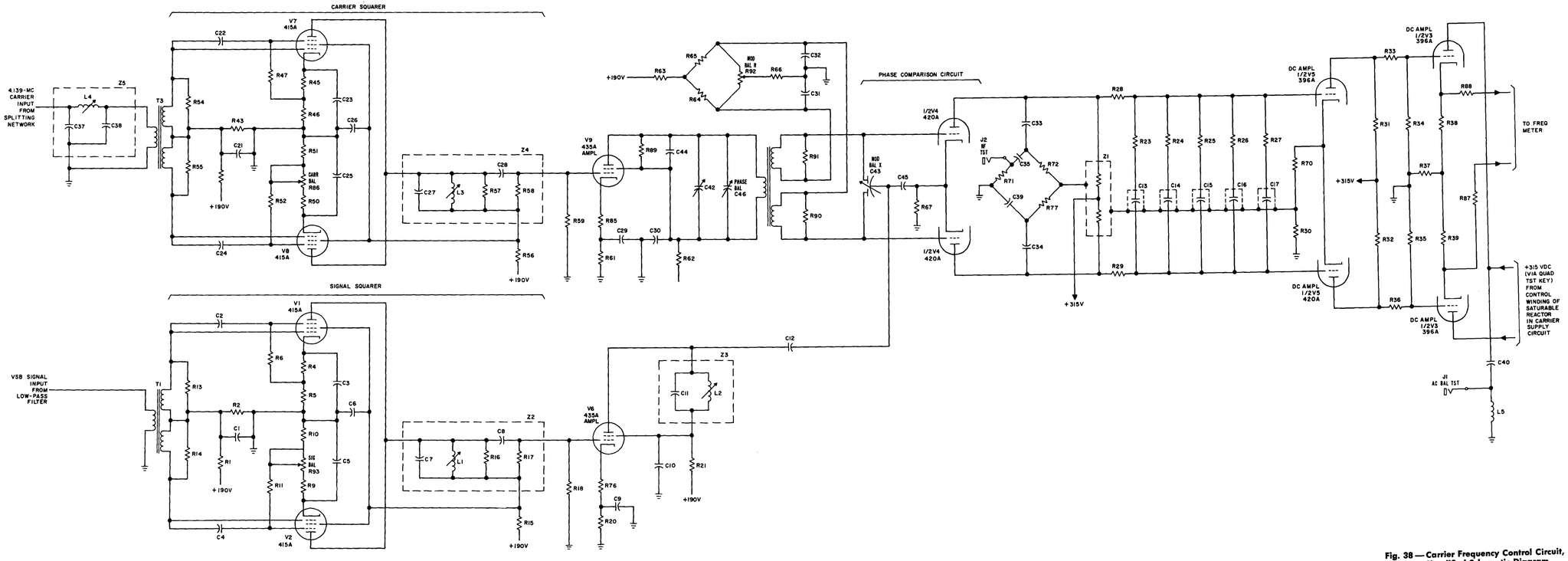


Fig. 38 — Carrier Frequency Control Circuit, Simplified Schematic Diagram

5.44 The rate at which the relay oscillator functions is determined by an RC network comprised of capacitor C19 in parallel with the winding resistance of relay K3. The delay provided by this circuit slows the rate of oscillation sufficiently to allow relay K2 to release after the polarity is corrected and before relay K1 can release (as a result of the ground at the junction of resistors R49 and R63).

5.45 During periods when no signal is received, neither modulator conducts. Relay K4 releases but its release is of no consequence since relay K2 remains released. However, when a nonstandard television signal is received (one which does not have the polarity-identifying characteristics required by the sensing circuits), the signal appears the same to both circuits, and both modulators conduct. In order to maintain the polarity previously established for a correct-polarity standard television signal, it is essential that relay K2 does not operate. To prevent operation, a capacitor (C23) in parallel with the winding of relay K2 delays its operation long enough to allow relay K4 to operate first. When relay K4 operates, its contacts shunt the winding of relay K2 and prevent its operation. Thus, the relay oscillation that would otherwise occur for nonstandard signals is prevented by locking out relay K2, and the relay oscillator remains in the condition required for a standard television signal of correct polarity.

5.46 The circuits which control the relay oscillator are shown in Fig. 40. The two similar portions of the polarizer each consist of a video amplifier, clipper, buffer, rectifier, dc inserter, ac amplifier, another dc inserter, and modulator. The information required by each of the two circuits is obtained by bridging one of the video amplifiers to one side of the video output line and the other video amplifier to the other side. The two amplifiers function on opposite extremes of the video signal, and the polarity of the signal determines which of the extremes each amplifier "sees". No transmission loss is introduced to the through circuit, and the two video amplifiers, bridged to the line in this manner, preserve line balance.

5.47 The outputs from the two video amplifiers are supplied to two clippers in such a way that the output of one clipper includes only the extremity of the picture information while the output of the other clipper includes only the extremity of the synchronizing pulse. The output of each clipper is then amplified and rectified in order to obtain separate dc voltages for operating the modulator tubes. A standard television signal containing picture information produces at the output of each rectifier a dc voltage sufficiently large to cause both modulators to conduct. The rectifiers, however, have time constants that are fast compared to the field scanning rate (60 cps) but slow compared to the line scanning rate (15,750 cps). The rectified output of one circuit, therefore, includes pulses derived from the 60-cycle vertical blanking interval of the video signal. These pulses are amplified, and then supplied to the suppressor grid of one modulator tube to prevent its conduction. The output from the other rectifier does not include these pulses, and the modulator following that rectifier conducts. Thus, for a standard signal containing picture information, the modulator in one sensing circuit will conduct while the other remains cut off.

5.48 For the case of a standard television signal containing only synchronizing pulses (a black picture), the output of each rectifier is a dc voltage, but one voltage is substantially greater than the other. The larger voltage supplied to one modulator causes it to conduct, while the smaller voltage supplied to the other modulator is insufficient to cause conduction. The circuits are arranged so that a correct-polarity television signal (with or without picture information) causes modulator 2 to conduct and modulator 1 to cut off. If the polarity changes, the sensing circuits recognize the change. Modulator 2 cuts off, modulator 1 conducts, and relay K2 operates. When relay K2 operates, it causes the polarity-reversing relay to operate to correct the polarity. Relay K2 then releases, and the sensing circuits again function as for a correct-polarity signal.

5.49 As shown in Fig. 40, the balanced signal at the video line output is supplied through coupling capacitors C10 and C11 to the grids of the balanced-to-unbalanced video amplifiers (V8 and V9). Resistor R35, which interconnects the two cathodes, provides high longitudinal suppression through cathode resistors R4 and R37. These resistors raise the cathodes to

about 70 volts above ground. The control grids are returned through resistors R40 and R41 to a voltage divider consisting of resistors R44 and R42. The divider supplies a positive potential of about 68 volts to each grid from the +190 volt supply. The difference in potential between the grids and cathodes establishes an operating bias of about 2 volts for the two video amplifiers. Plate voltage is supplied to the tubes through plate load resistors R3 and R38. Since each video amplifier supplies a separate sensing circuit, and because each circuit is identical, the description which follows is applicable to both, but is given only for the circuit associated with video amplifier tube V8.

5.50 The output of amplifier tube V8 is coupled through capacitor C1 and grid current-limiting resistor R8 to the grid of clipper tube V6. The clipper stage operates with normal plate voltage but with reduced screen voltage. With no signal at the input, the clipper operates at zero bias. With signal, grid current flows and an average grid bias is developed depending on the average positive excursions of the input signal.

5.51 A wrong-polarity signal having only synchronizing pulses (a black picture) will develop a small average bias on the clipper grid, and, consequently, a large output at the clipper plate. However, a correct-polarity signal having only synchronizing pulses will develop a larger average bias and a smaller output, about half that of a wrong-polarity signal. Fig. 41 illustrates the waveforms at various points in the polarizer circuit for a sync-only television signal of both polarities at the output of the receiving terminal. The waveforms are at the line scanning rate.

5.52 For the case of a composite television signal of either polarity, a small average bias will be developed at the clipper grid, resulting in a large output at the clipper plate. Additional information, however, is derived from this type of signal, which enables the circuit to recognize polarity and prevent false operation. Fig. 42 illustrates the waveforms for both polarities of a composite television signal at various points in the polarizer circuit. The waveform for a correct-polarity composite signal at the plate of clipper tube V6 will be roughly triangular in shape. This is because the output is high during the time that picture information is received, but low during the vertical blanking interval. A composite signal of the wrong polarity at the output of the receiving terminal will develop a high output during the time picture information is received and also during the vertical blanking interval. Thus, the waveform for a wrong-polarity composite signal does not have the triangular envelope. The waveforms shown in Fig. 42 are at the field scanning rate.

5.53 The output of clipper tube V6 is supplied through one section of capacitor C6 (designated C6A in Fig. 40) to the grids of buffer amplifier tube V3A. The primary purpose of this tube is to provide a signal turnover and also a low output impedance. Although tube V3A is shown as a single triode in Fig. 40, the tube is actually a double triode with two sections effectively connected in parallel. Each grid, however, is provided with a series resistor (not shown in the figure) to prevent high-frequency singing. Plate voltage is supplied through resistor R10 and negative feedback resistor R19, which lowers the output impedance of the stage. Bias is developed across cathode resistor R20, and the two grids are returned to ground through resistor R17.

5.54 The output from the buffer is supplied through the other section of capacitor C6 (designated C6B in Fig. 40) to electron tube V12. This tube is a double triode with both sections connected as diodes. One half functions as a dc inserter which conducts during negative excursions of the signal and cuts off during positive excursions. The positive dc bias, developed on the inserter cathode, remains fairly steady because of the long (0.25 second) time constant of capacitor C6B and resistor R16. The voltage at the cathode of the dc inserter therefore consists of a wave which can vary only in a positive direction starting from the positive dc bias. This wave also appears at the plate of the second half of electron tube V12, which functions as a peak rectifier. It develops a positive voltage across capacitor C5 which corresponds very nearly to the peak-to-peak value of the wave at the input to the rectifier. The time constant of capacitor C5 and resistor R15 is 680 microseconds, long compared to the horizontal blanking interval but short compared to the vertical blanking interval. As a result, the output will be an almost steady dc voltage for all types of signals except a composite television signal of correct polarity. For this type of signal,

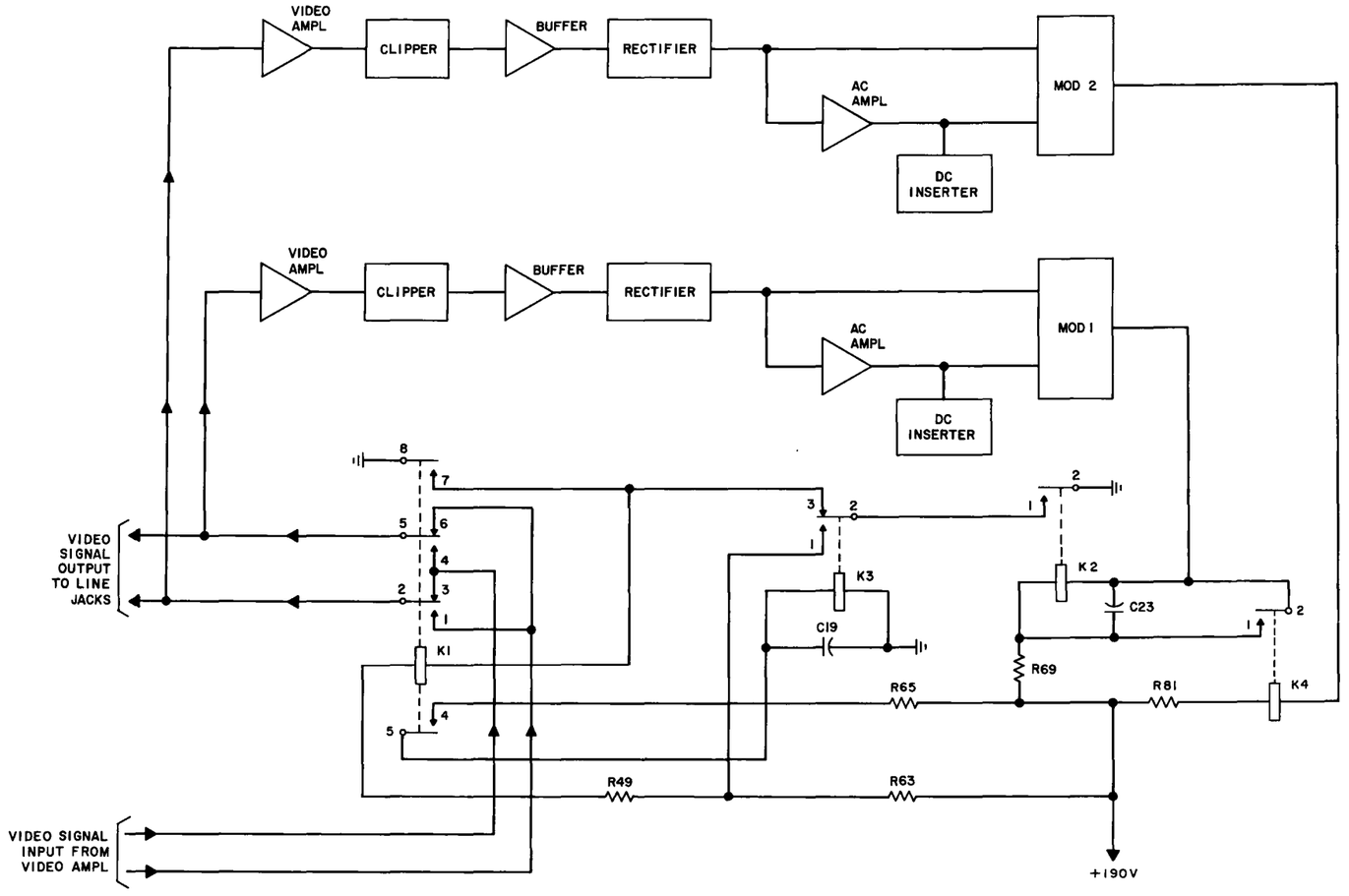


Fig. 39 — Polarizer Circuit, Functional Block Diagram

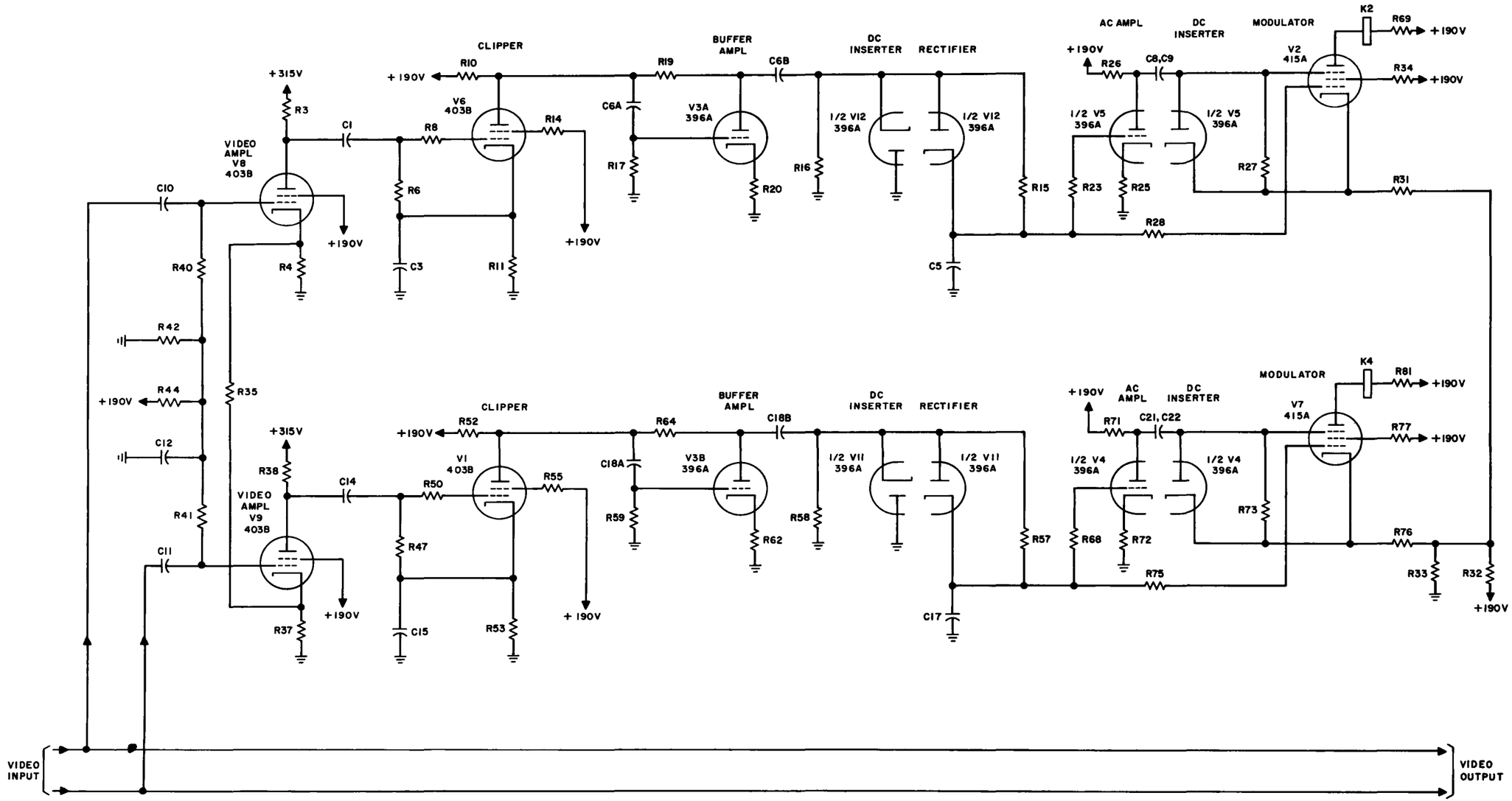


Fig. 40 — Polarizer Circuit, Simplified Schematic Diagram

the rectifier output voltage will decay during the vertical blanking interval, and possibly during part of the picture time. The result is an output with a low-frequency ac component. The rectifier output is connected through grid leak resistor R28 to the control grid of modulator tube V2 and through grid leak resistor R23 to the control grid of ac amplifier tube V5.

5.55 Modulator tube V2 operates with a cathode potential of approximately 12 volts obtained from a voltage divider connected between the +190 volt plate supply bus and ground. The divider is comprised of resistors R32 and R33. Since the suppressor grid of the tube is returned through resistor R27 to the cathode, it also has a positive potential of 12 volts. Under no-signal conditions, however, the +12 volt cathode voltage holds the tube at cutoff.

5.56 As previously described, the rectifier will develop a small, steady, dc output voltage for a sync-only signal of correct polarity. This voltage is insufficient to overcome the cathode bias on modulator tube V2. A sync-only signal of the wrong polarity, however, will develop a large rectifier output, more than enough to cause tube V2 to conduct. This is the desired operation.

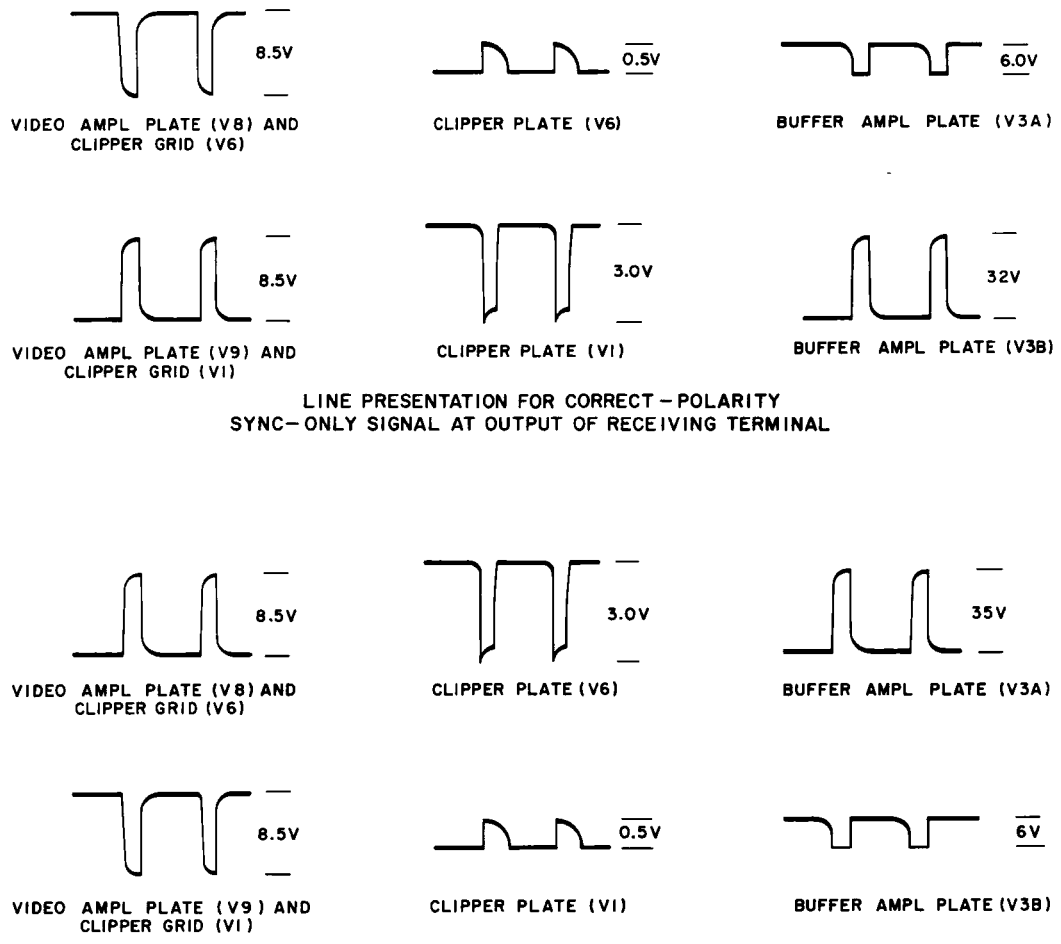


Fig. 41 — Waveforms at Various Points in Polarizer Circuit for Both Polarities of a Sync-Only Signal

5.57 The circuitry which makes possible polarity recognition of composite television signals consists of double triode tube V5 and associated components. One half of V5 functions as an ac amplifier which derives its input from the cathode of the peak rectifier. The control grid of the ac amplifier is returned to ground through resistors R23, R15, and R16. (See Fig. 40.) Plate voltage for the amplifier is supplied through load resistor R26, and cathode bias is developed across resistor R25. Parallel-connected capacitors C8 and C9 couple the output of the amplifier to the suppressor grid of V2. For the case of a sync-only signal of either polarity, or a wrong-polarity composite video signal, no output will be developed on the far side of capacitor combination C8 and C9 because the rectifier output will not have an ac component. For these signals, the voltage on the suppressor grid of tube V2 will be approximately +12 volts, the same as the voltage on the cathode. Since the voltage at the control grid of V2 is high for a wrong-polarity sync-only signal or a wrong-polarity composite signal, it overcomes the 12-volt cathode bias and V2 conducts. Under no-signal conditions, or for a correct-polarity sync-only signal, the rectifier output is low and V2 remains cut off.

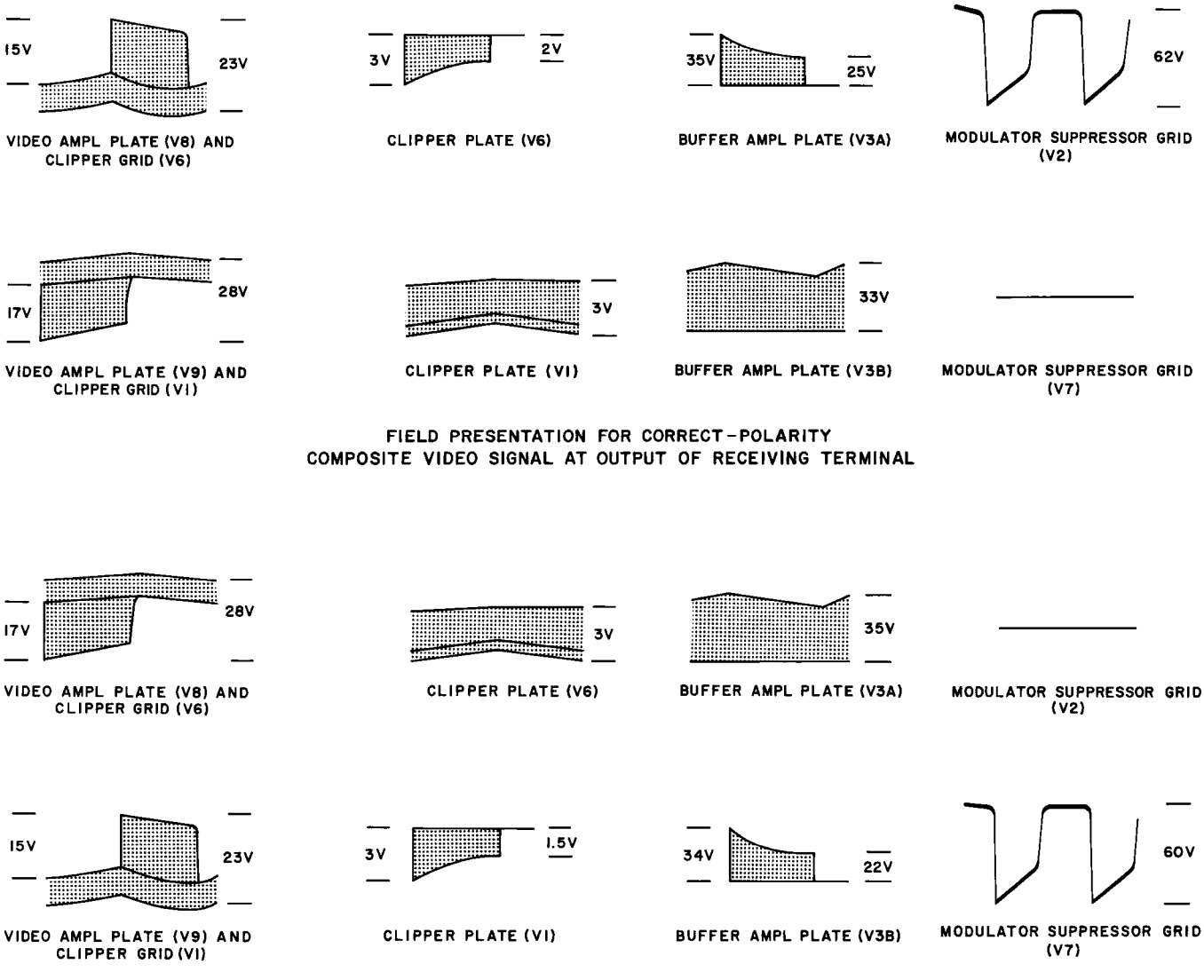


Fig. 42 — Waveforms at Various Points in Polarizer Circuit for Both Polarities of a Composite Video Signal

5.58 For a correct-polarity composite signal, the ac component across capacitor C5, which is supplied to the ac amplifier grid, will appear on the far side of capacitor combination C8 and C9 as a wave having narrow, positive-going pulses. The diode-connected half of tube V5 functions as a dc inserter to position the peaks of these positive pulses at a dc value equal to the normal bias on the suppressor grid of V2. As the diode conducts on positive peaks, the average voltage on the suppressor grid goes sufficiently negative to prevent conduction regardless of the large positive voltage supplied to the control grid. Modulator V2 is thus cut off for a composite television signal of correct polarity.

E. Equalizers (328A and 226L)

5.59 Two equalizers are provided in the receiving terminal. The fixed 328A equalizer compensates for nominal deviation, while the variable 226L equalizer compensates for broadband deviations. Both equalizers are described in Part 4K, and the loss-versus-frequency characteristics are illustrated in Fig. 34.

F. Carrier Suppression and Low-Pass Filter Panel (542A)

5.60 The 542A panel provides the mounting for the carrier suppression filter, which rejects 4.139-mc carrier leak, and the low-pass filter, which rejects an unwanted upper sideband by suppression frequencies about 5.0 mc. The circuit is shown in Fig. 43.

5.61 The carrier suppression filter is a 2-section, narrowband elimination filter designed to operate between balanced impedances of 124 ohms. Thermistor-controlled ovens on the filter panel maintain a close temperature control for the crystal elements in order to stabilize the resonant frequencies of the filter. The nominal loss of the filter is 7 db. The rejection band of the filter is within 400 cycles, centered at 4.139 mc, with a peak loss exceeding 35 db. The carrier suppression filter can be tuned for maximum loss at 4.139 mc by means of two adjustable capacitors located on the front of the panel above the crystal ovens.

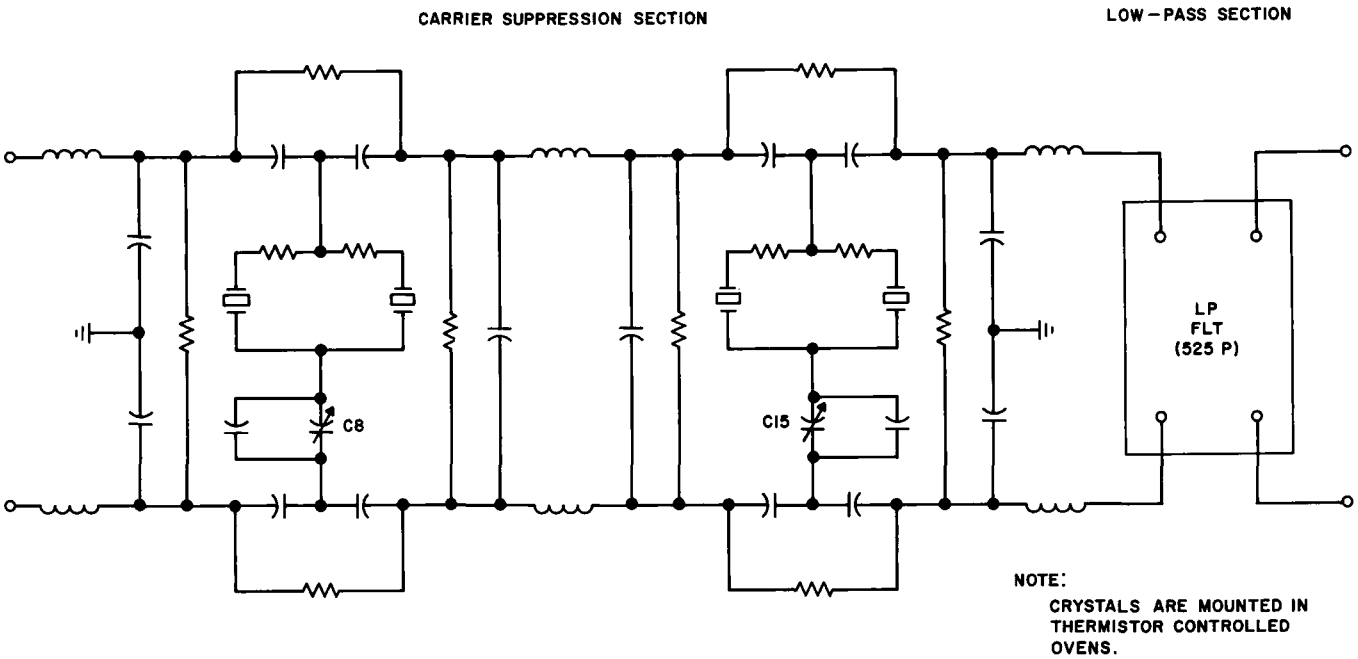


Fig. 43 — 542A Filter, Simplified Schematic Diagram

5.62 The low-pass filter, coded 525P, operates between 124-ohm impedances and is designed to pass frequencies up to 5 mc with 40 db of suppression from 7.6 to 11 mc.

6. POWER SUPPLY ARRANGEMENTS

A. General

6.01 The transmitting and receiving terminals are designed to operate from 115 or 230 volts ac, single-phase, 56 to 60 cps. Power can be supplied from a commerical source of either voltage or from the 505D power plant which supplies 230 volts ac to the L3 carrier equipment. A 24-volt battery is required for supplying power to the alarm lamps and for energizing one of the relays (filament activity relay K3) in the fuse and alarm panel.

6.02 The power supply equipment, which is mounted at the top of each terminal bay, consists of the line voltage regulator, the fuse and alarm panel, and the +190 volt and +315 volt metallic rectifiers. The combination of the magnetic ac regulator and metallic rectifiers in each bay provides adequate suppression of hum and line voltage variations.

6.03 Fig. 44 and 45 are functional block diagrams showing the ac power distribution in the terminals. As shown, the line voltage regulator in each terminal supplies stabilized 230-volt ac power to the 190-volt rectifier, the 315-volt rectifier, and the heater transformers of the vacuum tubes and crystal ovens in the bay. An autotransformer (T2) permits precise control of the 230-volt power supplied to the heater transformers. The autotransformer is connected between the 230- and 115-volt taps at the output of the regulator instead of between the 230-volt tap and ground. This arrangement permits the use of a 115-volt autotransformer to adjust the voltage between the limits of 115 and 230 volts. The total number of degrees of mechanical rotation provided by the ADJ VOLTS knob is therefore twice as great as would be provided if a 230-volt autotransformer were used, and the incremental change in voltage is smoother.

6.04 Accurate ac voltage measurements of the regulator output are obtained by means of a resistance divider and AC TST jack J3 located on the equalizer panel. The divider is comprised of parallel-connected resistors R18, R19, and R20 in series with resistor R21. The AC TST jack is connected at their junction. (See Fig. 44 and 45.) The resistor combination is designed to deliver a power level of 0 dbm into a 75-ohm load when the 60-cycle regulator output is 230 volts. A 73A power meter is normally used to measure the output at the jack.

6.05 The ac ground connection for the vacuum tube heater transformers appears on the back contacts of filament activity relay K3. (See Fig. 44 and 45.) The relay operates when the FIL ACT key is operated from NOR to TST, and shifts the ground connection of the vacuum tube heater transformers to a 15-volt tap on the regulator. The voltage applied to the tube heater transformer primaries is effectively reduced to 215 volts, which in turn reduces the cathode emission of the tubes. This test makes it possible to determine whether or not the cathode emission of the tubes is below certain minimum acceptable values while the tube heaters are operating at reduced voltage. The grounds for the crystal oven heater transformer primaries are not affected by operation of the filament activity relay.

B. Line Voltage Regulator

6.06 The regulator circuit delivers 115- and 230-volt ac power at a rated output of 750 volt-amperes. The regulator does not contain circuit breakers or fuses in its input but depends instead on the protection provided by fusing in the 115- or 230-volt ac main lines. The regulator will hold the 230-volt rms output voltage to ±1 percent and the peak output voltage to ±2 percent. The voltage output can be adjusted over a range of 5 to 10 volts by adjusting the air-gap screws associated with an inductor (L1) in the regulator.

C. Metallic Rectifiers

6.07 The metallic rectifiers supply the dc voltage requirements of the T3 and R3 terminals. The 315-volt rectifier is rated at an output of 0.37 amperes, while the 190-volt rectifier is rated at an output of 0.55 amperes.

6.08 Optional input connections are provided in the 315-volt rectifier for operating from a sine-wave input such as is obtained from commercial supply or 505D power plant, or from a complex-wave input such as is obtained from a magnetic-type voltage regulator. The output voltage is changed by means of an adjustment, designated ADJ VOLTS, which changes transformer taps.

6.09 A circuit breaker at the input provides overload protection and also the means for turning off the rectifier. Four distribution fuses of the indicating type are provided on the front panel of each rectifier. Direct current for the various panels in the bay is supplied through these distribution fuses. Alarm features are provided in each rectifier for connection to an alarm system.

D. Fuse and Alarm Panel

6.10 This panel mounts the alarm relay equipment and fuse holders for the 230-volt ac distribution fuses. The panel also contains filament activity relay K3 which, when operated, changes taps on the line voltage regulator output and effectively reduces the voltage supplied to the tube heater transformer primaries.

6.11 The alarm circuit, shown in Fig. 44 and 45, consists of a transformer, a rectifier circuit, and two relays (K1 and K2). Whenever any fuse in the ac distribution circuit opens, or whenever a circuit breaker on either of the two rectifiers opens, a contact is made so that 230 volts ac is supplied to the alarm circuit power transformer (T1). The transformer output is rectified by varistor CR1 (connected as a full-wave, bridge-type rectifier), and then supplied to relay K2. One set of contacts on relay K2 is connected to alarm lamp I1, which lights whenever the relay operates. Other contacts on the relay extend the alarm to external audible and visible alarm circuits. An AC ALM TST switch (S2) provides a means for testing the ac alarm circuit.

6.12 Whenever any of the four dc distributing fuses on the front of each rectifier panel opens, a contact is made within the fuse holder which supplies dc to relay K1. Whenever relay K1 operates, one set of contacts lights alarm lamp I1 while other contacts extend the alarm to the external alarm circuits.

E. Power Requirements

6.13 The ac power required for operation is 545 watts at 85 percent power factor for the transmitting terminal and 570 watts at 85 percent power factor for the receiving terminal. The dc power requirements are given in Tables A and B. The circuits associated with each of the four fuses in each rectifier are given, as well as the type of fuse required in each fuse holder.

TABLE A

T3 TRANSMITTING TERMINAL				
RECTIFIER	FUSE DESIG	CIRCUITS SUPPLIED	DRAIN (AMPS)	FUSE TYPE
190-VOLT	F1	HF AMPL 1 AND 2	0.120	70E
	F2	CARR SUP AND CARR HRM SUP	0.250	70G
	F3	CARR LEV CONT CIRCUIT AND MOD	0.135	70E
	F4	VIDEO AMPL	0.012	70K
315-VOLT	F1	HF AMPL 1 AND 2	0.080	70E
	F2	CARR LEV CONT CIRCUIT	0.045	70E
	F3	CLIPPER	0.070	70K
	F4	VIDEO AMPL	0.170	70K

TABLE B

R3 RECEIVING TERMINAL				
RECTIFIER	FUSE DESIG	CIRCUITS SUPPLIED	DRAIN (AMPS)	FUSE TYPE
190-VOLT	F1	HF AMPL 2	0.060	70E
	F2	CARR SUP AND CARR HRM SUP	0.250	70G
	F3	POL, DEMOD, AND CARR FREQ CONT CIRCUIT	0.150	70F
	F4	VIDEO AMPL AND HF AMPL 1	0.072	70K
315-VOLT	F1	HF AMPL 2	0.040	70E
	F2	POL	0.030	70E
	F3	CARR SUP, HF AMPL 1 AND CARR FREQ CONT CIRCUIT	0.050	70E
	F4	VIDEO AMPL	0.170	70K

7. EQUIPMENT ARRANGEMENTS

7.01 The T3 and R3 television terminal equipment is mounted on 11-foot 6-inch duct-type bays with vacuum tubes and operating controls on the apparatus side. The terminals are illustrated in Fig. 46 and 47.

7.02 Most of the transmission units have jack appearances on their equipment panels for their input and output circuits. Coaxial cables, which provide interconnection of these units, also have jack appearances on the equipment panels, and patch plugs are used to complete the interconnections. This method of interconnecting transmission units permits the use of shorter coaxial cables than would otherwise be required if run to a common jack field. This method also allows the electrical characteristics of the cables to be included in the design. Removal of the patch plugs associated with these interconnected panels facilitates testing by providing electrical access to various points in the transmission paths.

7.03 A 35-pin connector block is provided on each panel so that tube tests can be conducted using the J44104R vacuum tube test set and a connecting cord. The grid and cathode points of each panel are connected through isolating resistors to the various pins on each connector block. In general, the tube designations of the various panels are made to correspond with the designations of the different tube test positions of the vacuum tube test set. An exception occurs in the carrier frequency control circuit where no provision is made for testing tubes V4 and V5. In certain cases, tube designations are omitted, as in the polarizer which contains no tube designated V10. In other cases, tubes are numbered higher than the highest-numbered designation on the test set, such as tubes V11 and V12 in the polarizer. These tubes cannot be tested by use of the J44104R test set but must be removed from their sockets and tested in a KS-type or commercial vacuum tube test set.

8. J44104R VACUUM TUBE TEST SET

8.01 The J44104R vacuum tube test set is designed to detect vacuum tubes whose thermionic emission is nearing the lower useful life limit. This test is made by measuring the percentage of grid bias change introduced by plate current variations that occur when the heater voltage is lowered from 6.1 volts to 5.7 volts. The test set can also be used as a voltmeter to measure dc rectifier voltages in the transmitting and receiving television terminal bays. The function desired is selected by operation of the 11-position TUBE TEST switch. (See Fig. 48.)

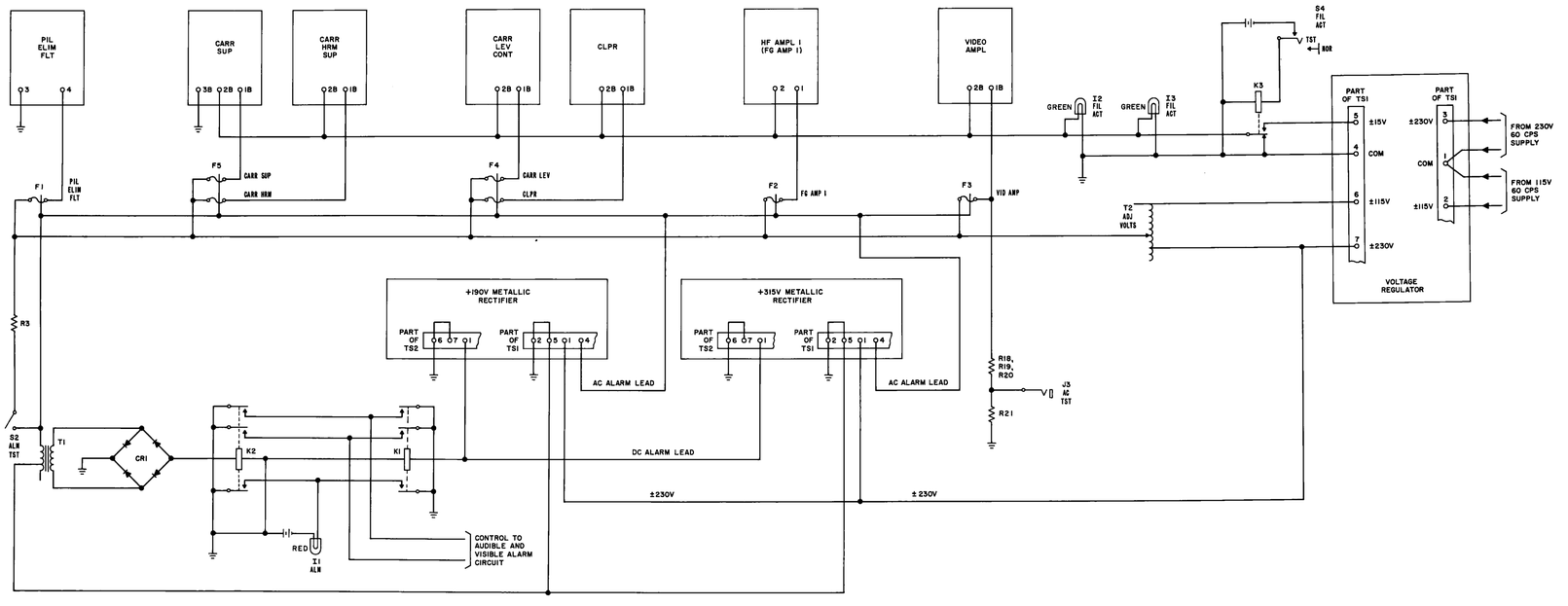


Fig. 44 — T3 Transmitting Terminal, AC Distribution, Functional Block Diagram

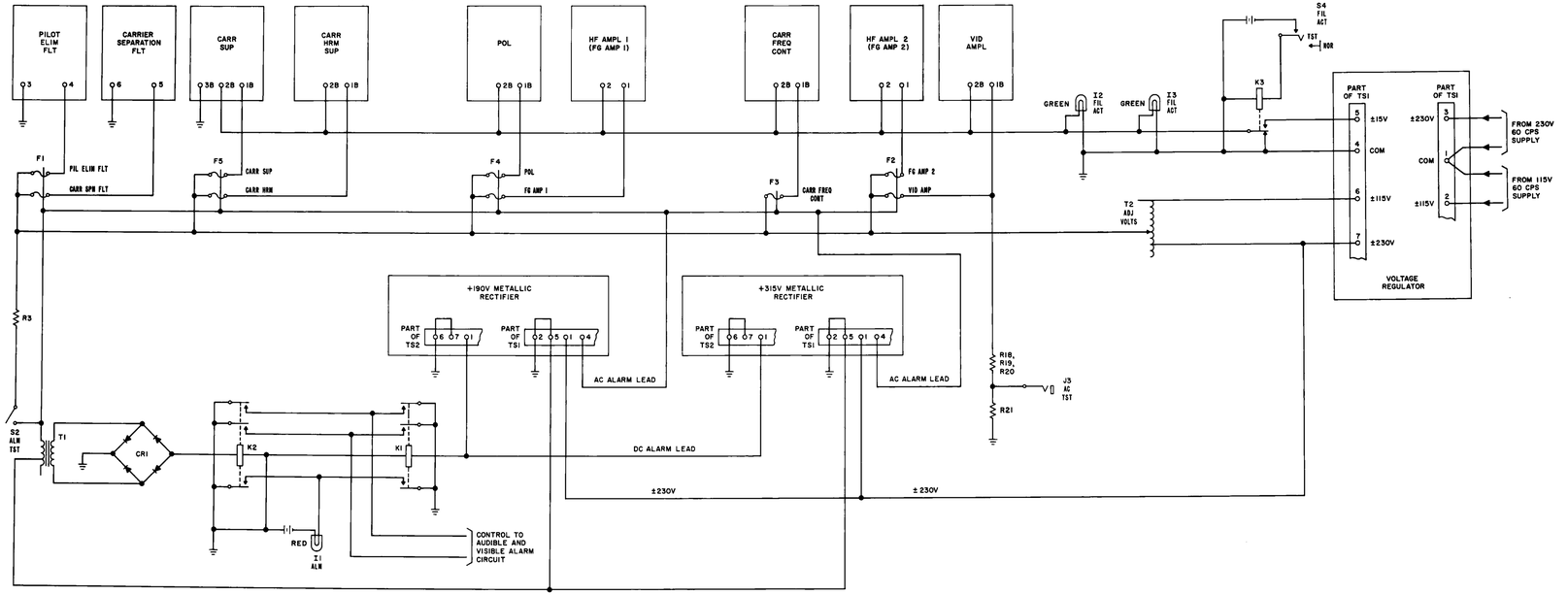


Fig. 45 — R3 Receiving Terminal, AC Distribution, Functional Block Diagram

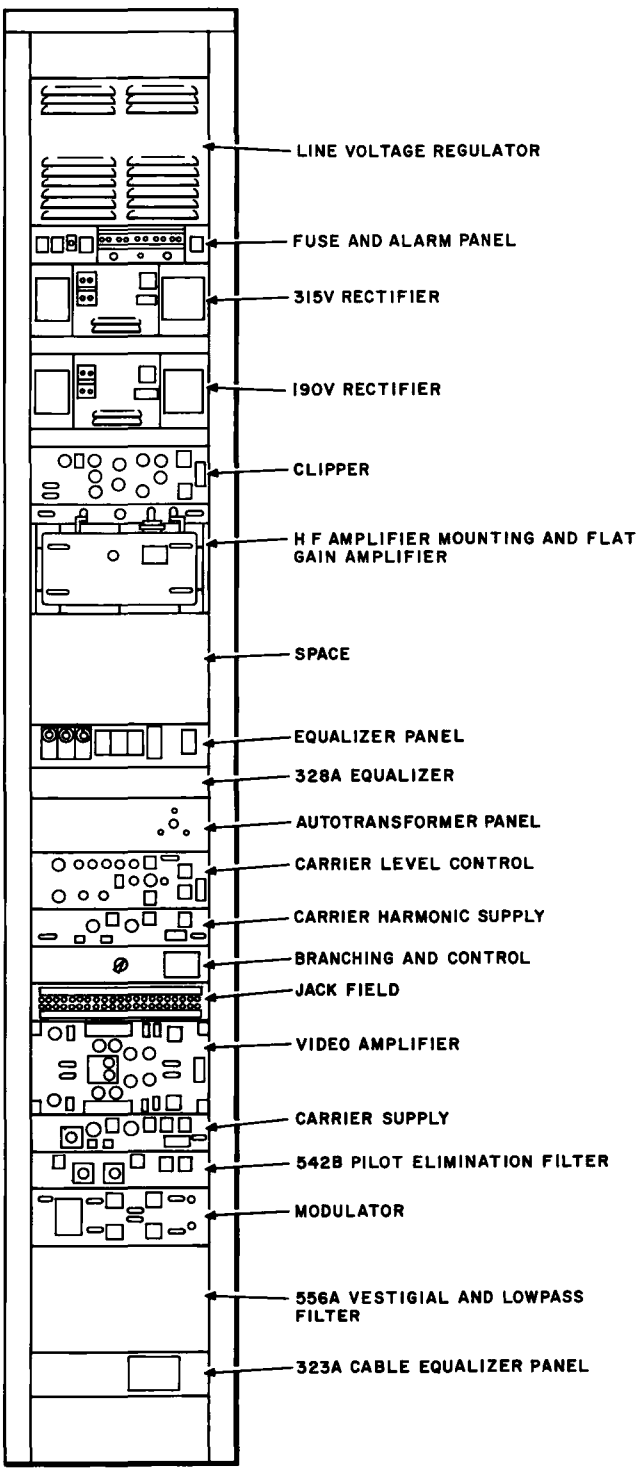


Fig. 46 — T3 Transmitting Terminal, Front View

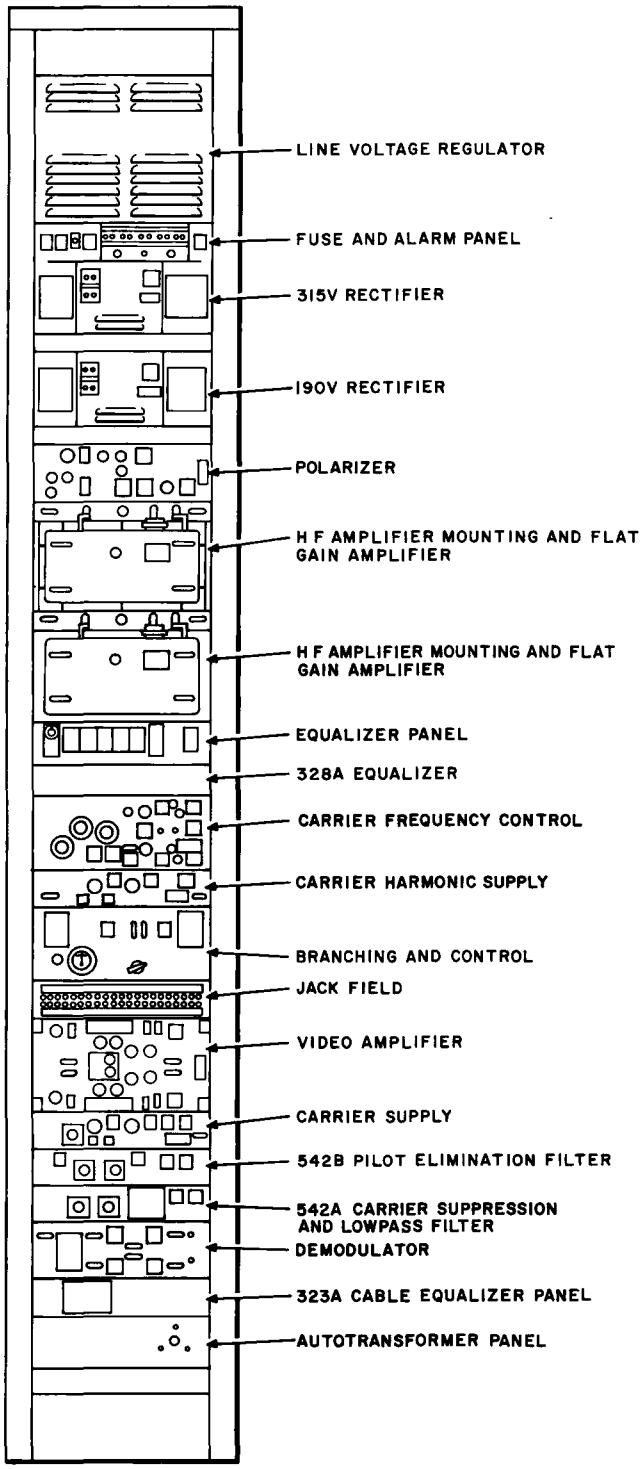


Fig. 47 — R3 Receiving Terminal, Front View

8.02 All vacuum tubes in the terminals having designations which correspond to designations on the vacuum tube test set can be tested, with the exception of tubes V4 and V5 in the carrier frequency control circuit. These tubes, as well as tubes V11 and V12 in the polarizer, must be tested in a KS-type or commercial vacuum tube test set. No provision is made in the J44104R vacuum tube test set for checking gas regulator tube V10 in the carrier level control circuit.

8.03 Testing with the tubes in their socket positions is made possible by a 35-pin connector block on the face of each panel. A connecting cord provided with the vacuum tube test set permits connection to each block. Provision is made in the test set for testing tubes that normally operate at cutoff or with low values of plate current. Various contacts of the TUBE TEST switch connect circuit components within the tube test set into the circuit which cause the tube under test to draw peak operating current while isolating it from interaction effects of other tubes.

8.04 Filament activity tests on high-frequency amplifiers require the use of an adapter which is supplied with the vacuum tube test set. This adapter connects between the cord and the high-frequency amplifier.

8.05 In practice, the test cord of the test set is connected to the block of the panel under test. If the carrier level control circuit is being tested, the carrier level control key must be set to the OPR position. Ten thumb-operated potentiometers (one for each of ten positions of the TUBE TEST switch) are then adjusted to produce zero indications on the PERCENT scale of the 0- to 20-microampere meter while the TUBE TEST switch is rotated through the ten tube-test positions. After each potentiometer is adjusted, the FIL ACT key on the jack field of the terminal is operated from NOR to TST. This operation energizes relay K3, which in turn reduces the voltage supplied to the tube heater transformer primary windings from 230 volts to 215 volts. The reduction in voltage results in a change from 6.1 volts to 5.7 volts at the tube heaters. After the tube heaters have stabilized at the lower temperature, the TUBE TEST switch is again rotated through its various positions. The percentage change indicated on the meter for each position of the switch is noted. Any tube which fails to meet its minimum requirement should be replaced.

8.06 The J44104R vacuum tube test set is a self-contained portable unit weighing approximately 5 pounds. Its overall dimensions are 8 by 10 by 6.5 inches. A removable cover stores the Jones plug adapters and the cable to connect the test set to the panel being tested. The test set circuit is shown in Fig. 48.

9. LIST OF DRAWINGS (NOT ATTACHED)

9.01 The following SD drawings are related to this section.

SD-42024-01	T3 Television Terminal, Application Schematic
SD-42025-01	R3 Television Terminal, Application Schematic
SD-42026-01	Video Amplifier Circuit
SD-42027-01	Modulator Circuit
SD-42028-01	Demodulator Circuit
SD-42029-01	Carrier Supply Circuit
SD-42030-01	Carrier Level Control Circuit
SD-42031-01	Carrier Frequency Control Circuit
SD-42032-02	Polarizer Circuit
SD-42033-01	High-Frequency Amplifier Mounting and Heater Supply
SD-42034-01	Video Clipper Circuit
SD-42038-01	Carrier Harmonic Supply Circuit
SD-42042-01	Vacuum Tube Test Set (J44104R)

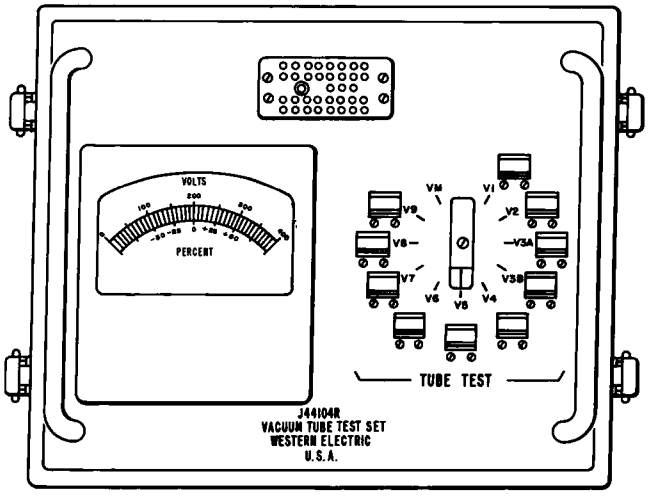


Fig. 48 — J44104R Vacuum Tube Test Set, Cover Removed