SYSTEM CENTURY®
DIGITAL CENTRAL OFFICE

LOCAL LINE SWITCH
DESCRIPTION AND OPERATION

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1. INTRODUCTION

1.01 This section provides functional descriptions of the circuits that make up the local line switch (LLS) of a SYSTEM CENTURY DCO System. An overall description of the entire DCO System is provided in the section titled *General Description*, referenced in paragraph 2.02.

2. RELATED INFORMATION

2.01 General.

A Sales and Instructional Literature Index of latest available publications can be obtained from your Stromberg-Carlson sales representative or from Publications Services, Stromberg-Carlson Corporation, 400 Rinehart Road, Lake Mary, Florida 32746.

2.02 Related Sections.

The following sections are recommended for use with this document. To determine the actual section numbers, refer to the *DCO Index of Related Sections* provided with your set of Stromberg-Carlson Practices (SCPs).

23-YYY-02	General Description
23-YYY-51	Equipment Location

3. GENERAL

3.01 The LLS (fig. 1) is a solid-state, pulse-code-modulated (PCM) line-switching frame. It has the capability of connecting up to 1,080 lines to, from two to eight, 30-timeslot port group highways in the DCO common equipment, by way of a time-switching stage. This variable port group highway capability allows up to 6.2 average busy season busy hour (ABSBH) hundred call seconds (CCS) per line without depopulation. The line group highway switch provides full availability from any line to any port group highway timeslot.

3.02 The line switch controller monitors all activities of the line groups, assigns lines to port group highway timeslots, controls the maintenance and administration functions for the LLS frame, and transfers information between the LLS and the DCO common equipment.

3.03 The line switch controller also controls the line test controller and the maintenance and diagnostic controller.

a. The line test controller does line routining and party testing and makes measurements for the automatic line insulation test (ALIT). All test results are reported to the line switch controller.

b. The maintenance and diagnostic controller is the gathering point for alarms and status changes in the LLS frame and reports directly to the line switch controller. In addition, the maintenance and diagnostic controller serves as an interface for telephone-company provided alarm and control signals.

3.04 Each LLS frame (fig. 2) containing up to 1,080 lines, is 87 inches (221 cm) high, 54 inches (137 cm) wide, and 22 inches (56 cm) deep. The two top cells in the frame contain redundant control circuits for the frame. The 12 line group cells each contain 90 lines and associated circuits that make up the line group.

4. SYNCHRONOUS DATA LINK CONTROL LOOPS

4.01 The LLS contains several circuits (communications buffer controllers, line switch controllers, line group controllers, line test controllers, and maintenance and diagnostic controllers) that are controlled by microprocessors. Because proper operation of the LLS depends on accurate and timely communication between these processors, all inter-processor communication is done with synchronous data link control (SDLC) loops. The following subparagraphs provide a general description of SDLC loops.

4.02 An SDLC loop contains one master station and one or more slave stations. The master is responsible for controlling all communications on the loop and for all maintenance and diagnostics of the loop. Slave stations acknowledge receipt of all commands from the master station; the master station responds to all information messages received from a slave. All transmissions are originated by the master station and sent around the loop in the same direction. All transmissions are in sequenced, numbered messages. Each station maintains a send and receive message count for each station with which it communicates. Message counts are sent with each message and the count is verified by the receiving station. Out-of-sequence messages are rejected.

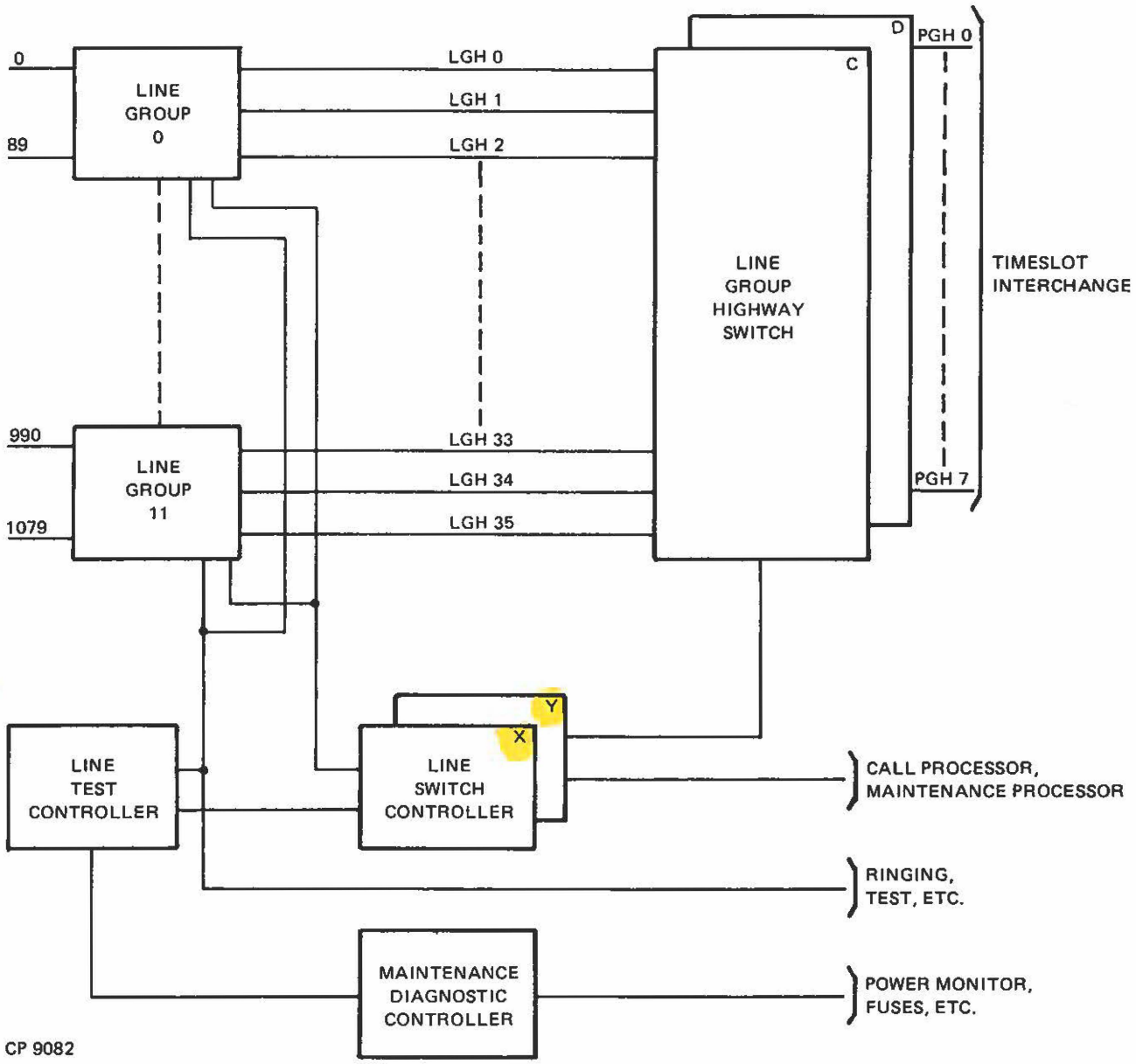

Figure 1. Local Line Switch, Basic Block Diagram

4.03 Commands sent by the master station can be addressed to any or all of the slave stations. When a slave receives a message addressed to another station it passes the message on down the one-way loop. All transmissions are made in a frame format. This enables the receiving station to determine where the transmission starts and stops, whether the message is intended for that station, what actions are to be done with the transmission, specific information for that station, and whether the frame was received without error.

4.04 An SDLC loop is designed so that when a slave station is removed bypass relays in the next station on the loop close to maintain the loop. The relays also close if +5 volts or –48 volts are lost, if a bypass signal is received, or if a faulty circuit is detected.

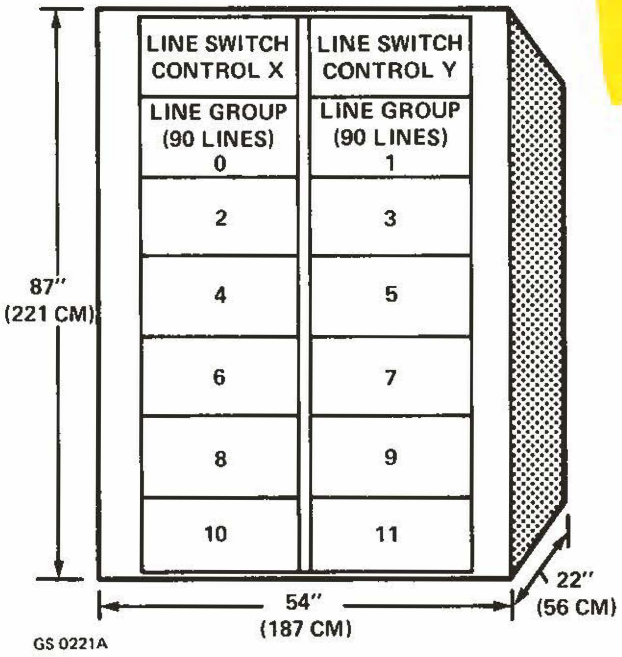

Figure 2. Local Line Switch Frame

5. LINE GROUP

5.01 General.

a. One line group (fig. 3) is housed in each line group cell and consists of 90 lines, line group multiplexer (mux/demux), line group access, and line group controller circuits. The line group mux/demux contains three identical circuits, each serving 30 lines and one line group highway. Each line circuit contains a CODEC that encodes the analog input into PCM signals. Each group of 30 lines is multiplexed in groups of 4, onto 8 wires to the line group mux/demux.

b. The line group is microprocessor controlled by the line group controller, which monitors the lines and the mux/demux and reports to the line switch controller.

c. The line group access, under control of the line group controller, allows the line routiner to access the tip and ring (in and out) for automatic line insulation testing (ALIT) and routine line testing.

5.02 Line Circuits.

a. Three types of line circuits are available. Each line circuit is arranged for two-to-four wire mode of transmission with two wires to the subscriber and four wires to the switching system. Each line has a switchable (software controlled) balance network for use with either loaded loops or unloaded loops.

b. A series of relays establishes the normal data path into each line circuit, as shown in figures 4 through 6. The test access, reverse, and ringing relays are standard on each line circuit; the others vary according to the functions required. In addition to providing a path for normal call data through the line circuit, the relays provide the following features:

1. The test access relays allow testing of the tip, ring, sleeve, and meter pulse leads through the system or out towards the subscriber.

2. The reverse relay reverses the tip and ring leads to provide reverse-battery answer supervision and to apply ringing to the tip lead for divided ringing applications.

3. The ringing relay connects the multifrequency ringing bus to the ring lead (or tip lead if reverse relay is operated).

4. The calling battery logic monitors the tip and ring loop status and repeats dial pulses to the sense bit logic and line group control as the loop is closed and opened.

5. The ground relay grounds the tip lead for ground-start operation and grounds the sleeve lead for sleeve-lead-control operation.

6. The open loop relay operates when a ground is received on the sleeve lead. This opens the tip and ring paths and sends a sense bit to the line group controller.

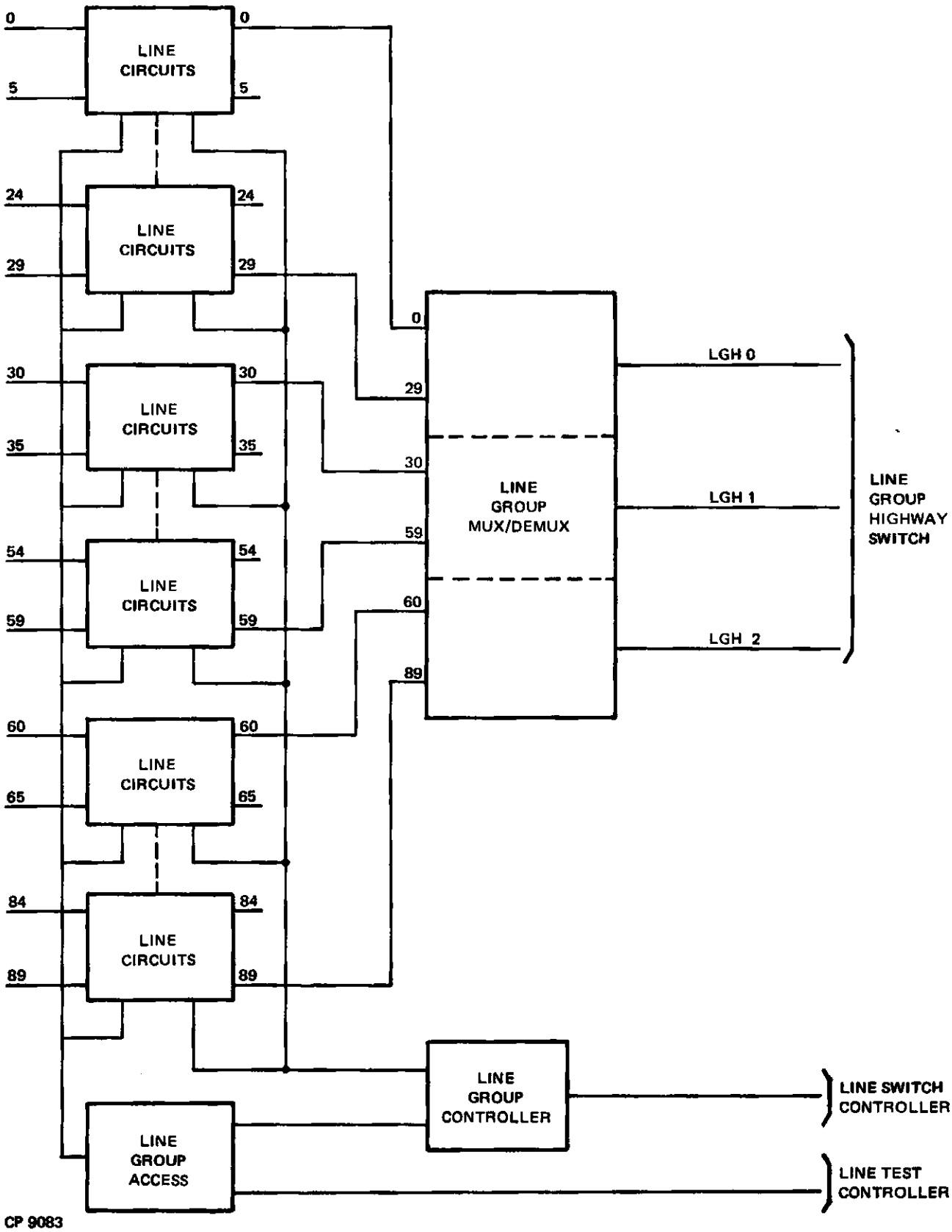

Figure 3. Line Group, Block Diagram

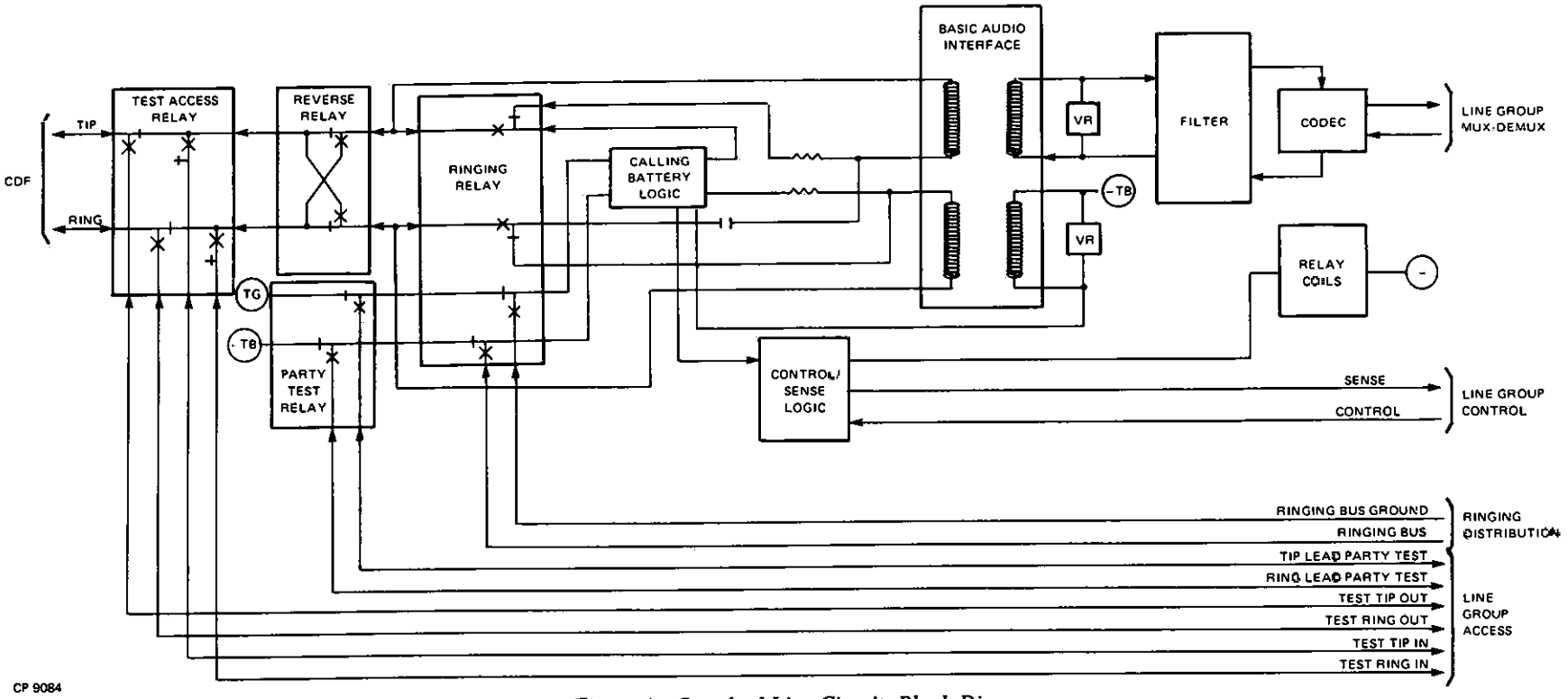

Figure 4. Standard Line Circuit, Block Diagram

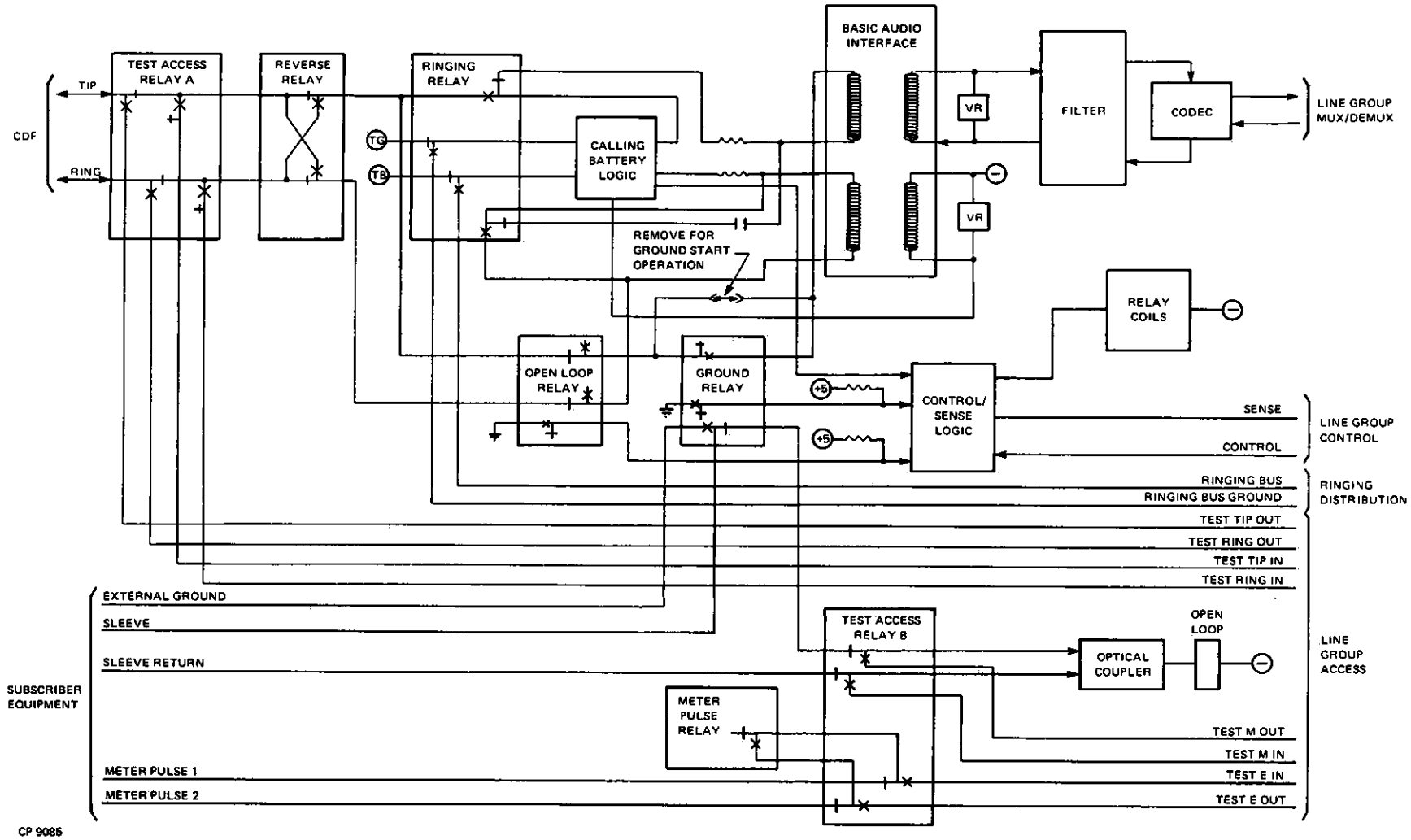

Figure 5. Sleeve Lead Line Circuit, Block Diagram

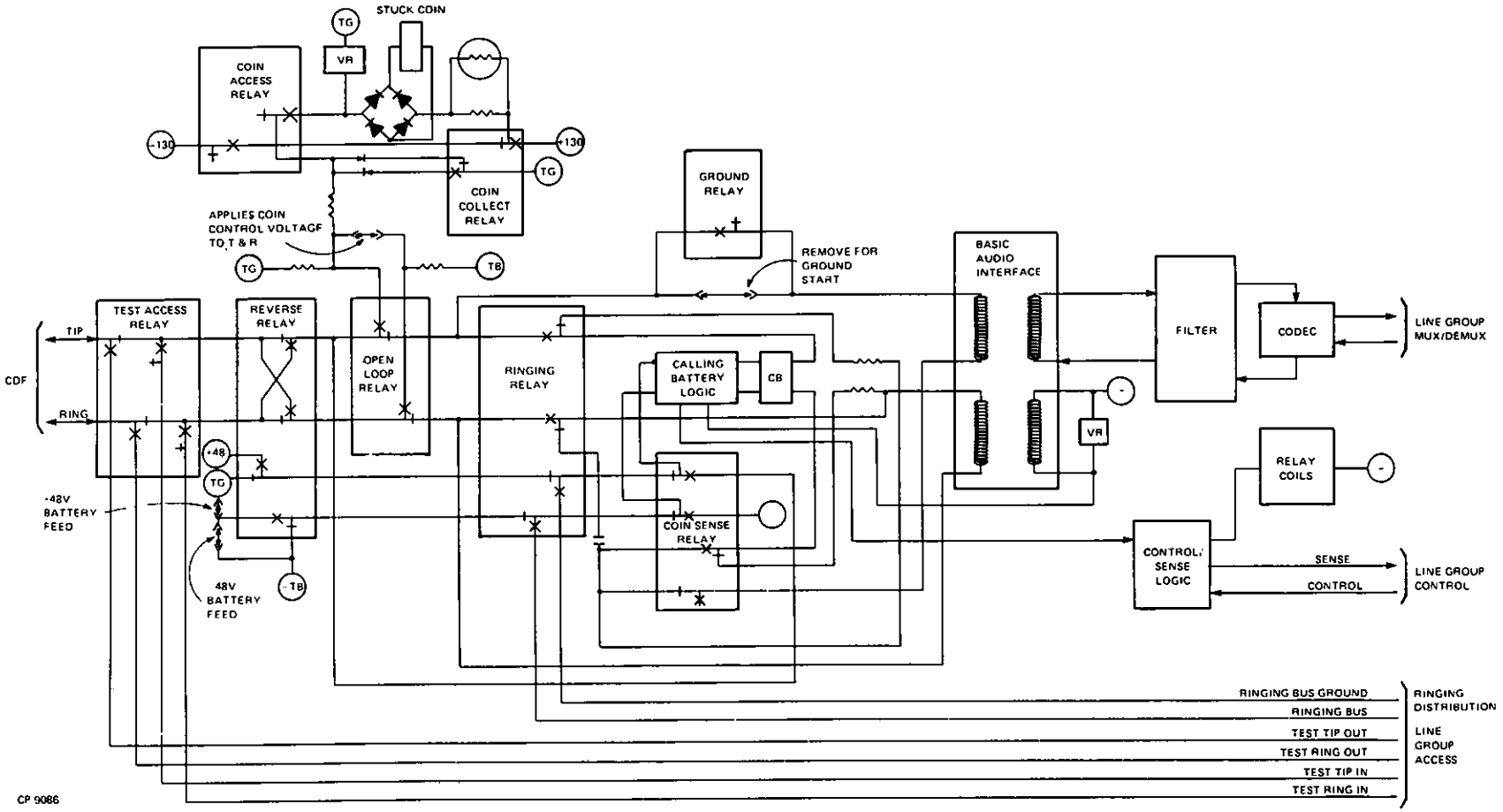

Figure 6. Paystation Line Circuit, Block Diagram

c. Two basic line circuit PWBAs, each containing six line circuits, are available. Figure 4 shows one line circuit. Assembly 817541-026 provides 4-party, bridged-ringing service; assembly 817541-036 provides 8-party, divided-ringing service.

d. The sleeve lead line PWBA (817543-026), containing three line circuits, can interface with a variety of subscriber or peripheral equipment. One or more of the following can be provided by the circuit shown in figure 5:

1. Sleeve lead control and sensing.
2. Meter pulse control for message metering.
3. Loop range extender control.
4. External test access control.
5. Reverse-battery supervision.
6. Sleeve lead ground start supervision.
7. Interface with the following:
   a) Hotel/motel systems.
   b) Private branch exchanges.
   c) Improved mobile telephone service (IMTS).
   d) Customer-supplied volunteer fire reporting systems.
   e) Specialized line adapters.

e. The prepay paystation line PWBA (817545-526 or 817545-536) contains three line circuits. In addition to the normal functions of a single-party line circuit, this circuit (fig. 6) provides for coin collection, coin return, coin-deposit sensing, and stuck-coin sensing. The circuit is designed for single-slot or multislot prepay paystations, coin-first or dial-tone-first signaling, and either inband tones (817545-526) or the multiwink method (817545-536) for operator control of coins. Coin collection or return at the paystation is done by applying +110 volts or −110 volts, respectively, to the paystation line by means of coin collect and coin access relays. The stuck coin relay is used to determine if a coin is stuck in the coin mechanism.

5.03 Virtual Spare Line Circuit.

One line circuit in each LLS frame is designated as a spare. This circuit is automatically put into service if routine testing or diagnostic testing determines that a regular line circuit is inoperative, that the spare can restore full service to the subscriber, and that the spare is not currently assigned. The spare line remains in service until manually reassigned or unassigned. The spare line can be manually assigned at any time.

5.04 Line Group Multiplexer/Demultiplexer.

a. The line group mux/demux PWBA (fig. 7) in each line group cell contains three identical circuits. Each circuit accepts voice and supervisory data from 30 lines (multiplexed on 8 wires) and multiplexes the data onto one line group highway. Any line in a 30-line group can be assigned to any timeslot on the line group highway. The line group mux/demux converts parallel 8-bit words into a frame of serial words. Thirty six line group highways from 12 line group mux/demux PWBAs, serving 1080 lines, are connected to line group highway switch I.

b. The multipexed transmit voice data received from the line circuit CODECs at a 256-Kbs rate is further multiplexed (8:1) and stored in a voice RAM. The write addresses for the voice RAM are provided by the line group controller.

c. The voice RAM is read sequentially in the port group highway format. The transmit and receive data is synchronous at the line circuit CODEC and the line group highway (no offset between transmit and receive data). The transmit and receive voice RAMs function as a dual-port RAM (while transmit data is being written, receive data is being read, and vice versa).

d. Receive operation is similar to transmit operation.

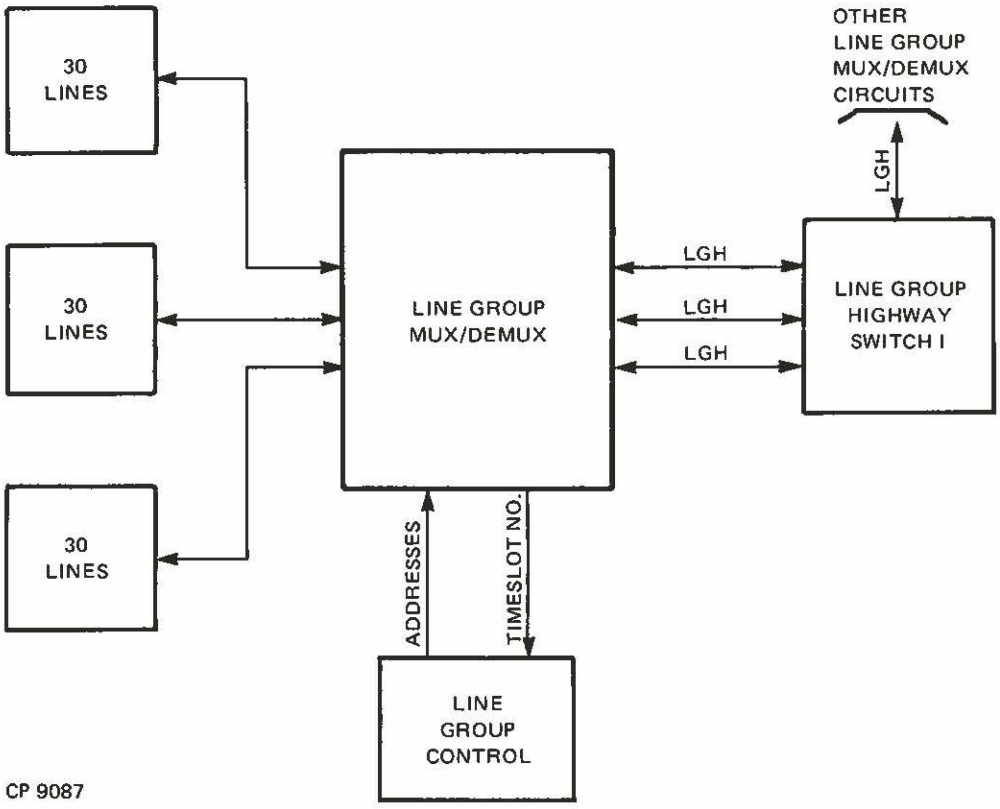

Figure 7. Line Group Mux/Demux, Orientation Diagram

5.05 Line Group Controller.

The line group controller (fig. 8) is the control interface for the 90 lines in a line group. Through communications with the following circuits, the line group controller performs the functions described.

a. Line Switch Controller.

Through an SDLC loop (par. 4), the line switch controller controls the line group controller and sends and receives port supervisory information to and from the line group.

b. Line Group Access.

Relays in the line group access circuit that control access to the lines are controlled by the line group controller microprocessor. The line group controller is directed by the line switch controller (by way of the SDLC loop) to operate specific relays in the line group access circuit which provide test paths as required.

c. Line Group Mux/Demux.

The microprocessor data bus of the line group controller is extended to read and write registers that control time slot assignments in the line group mux/demux. In addition, equipment number and read/write timing signals are provided to the line group mux/demux for stripping control bits from, and inserting sense bits onto the line group highway.

d. Line Circuits.

Up to 90 line circuits are scanned every millisecond for sense supervisory information. These bits are loaded, by the line group controller, into serial shift registers on the line circuits and shifted into the line group controller memory for later access. Every four milliseconds, control information written into line group control memory by line switch controller command,is serially shifted to the line circuits and latched. Sense and control

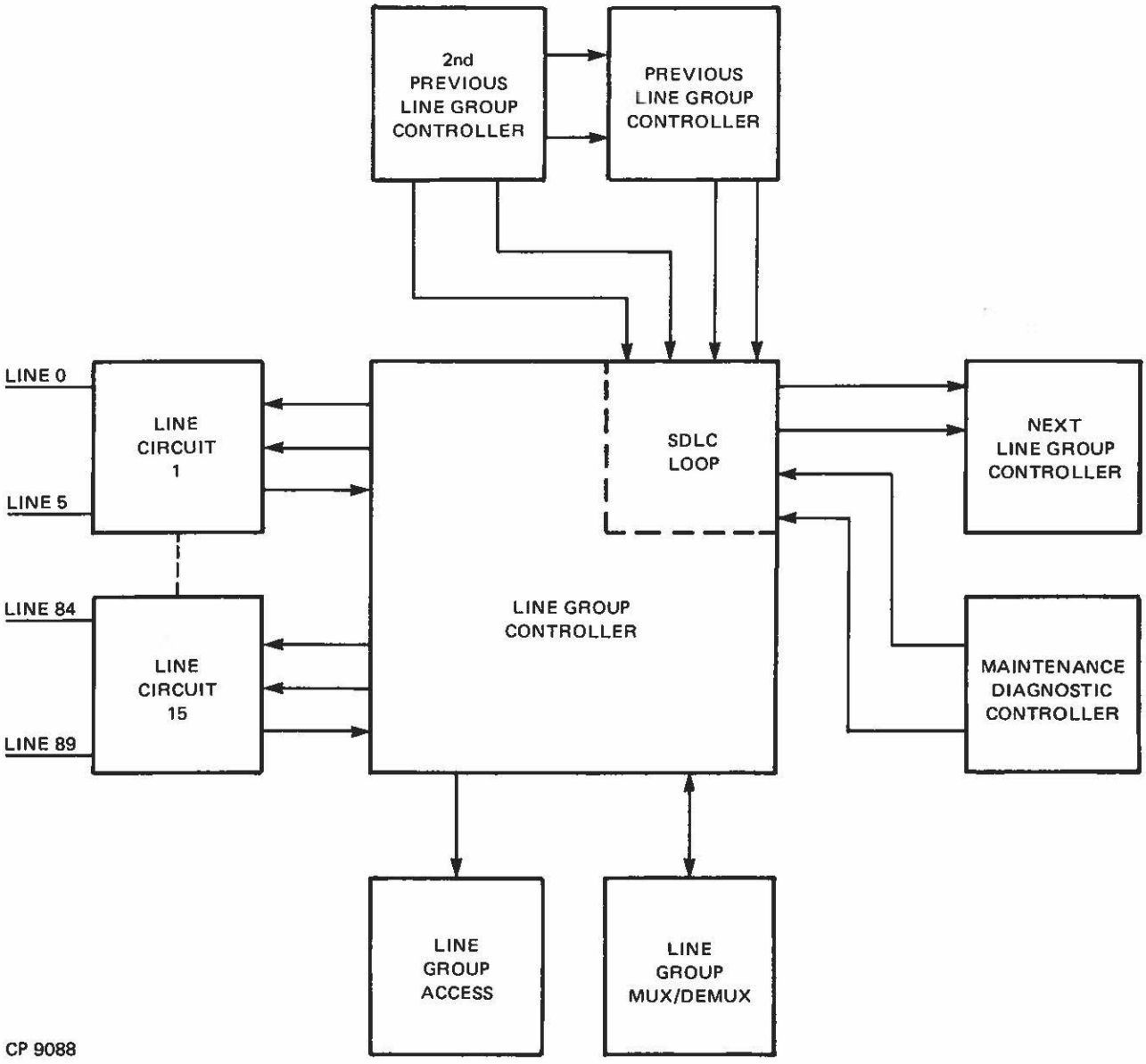

Figure 8. Line Group Controller, Orientation Diagram

information for each port is always available in line group controller memory and can be accessed at any time, except during direct memory access scan cycles.

5.06 Line Group Access.

a. The line group access circuit contains 14 relays that switch various buses between line circuits and the test access selectors, line test circuit, and virtual spare line circuit. All relays are under direct control of the line group controller.

b. Each line group is divided into three 30-line subgroups. Nine of the fourteen relays are used to establish paths between the subgroups, test access selectors and the line test circuit. Two relays switch in the virtual spare line circuit, when required. One relay is provided to connect sleeve leads from sleeve lead lines to the line test circuit. A party test relay connects a multiparty line to the party test bus. Figure 9 is an orientation diagram for the line group access circuit.

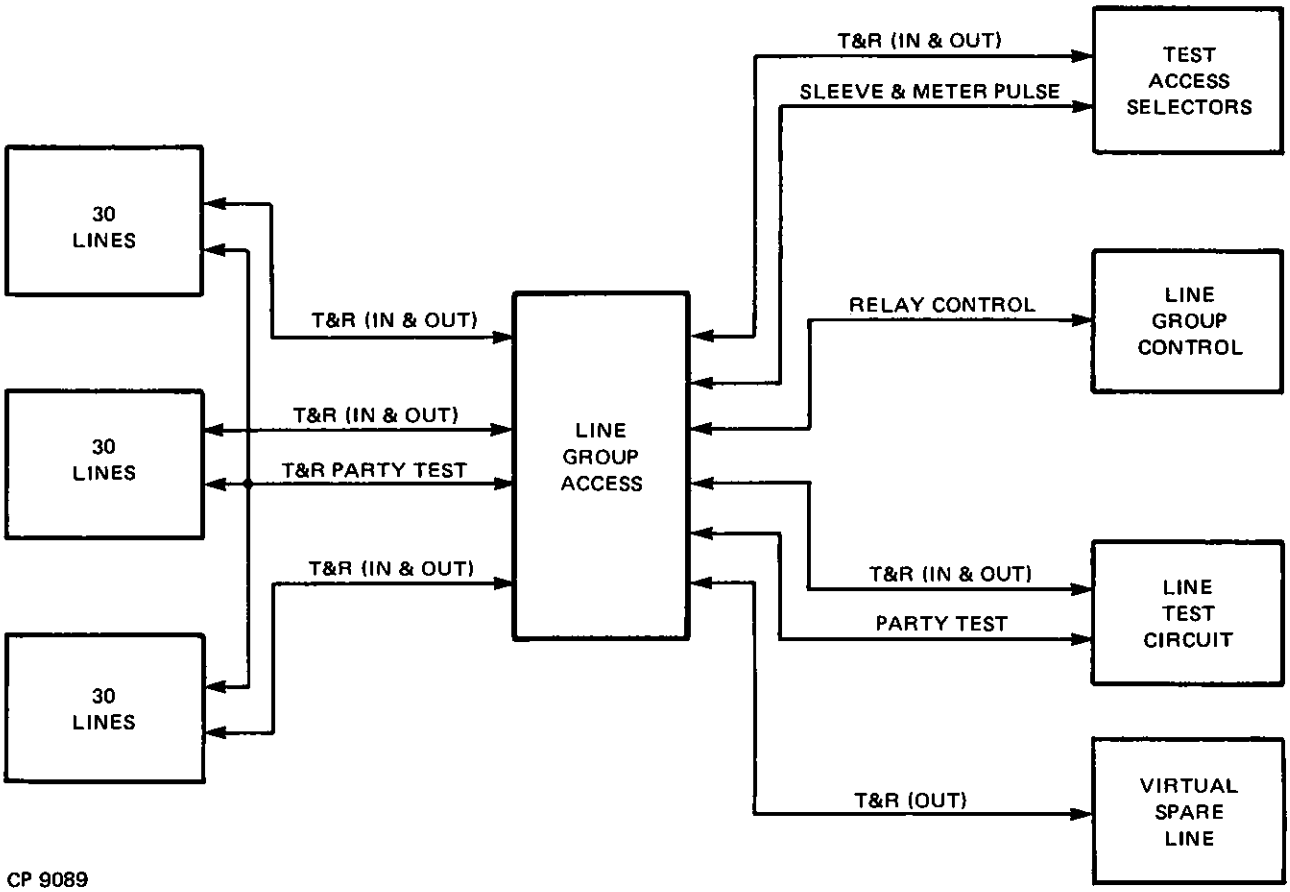

Figure 9. Line Group Access Circuit, Orientation Diagram

6. CONTROL CIRCUITS

6.01 General.

The control circuits for an entire LLS frame, except the line group controllers (par. 5.05), are mounted in the two top cells of the frame (fig. 2). Each of these X and Y line switch controller cells contains a line switch controller circuit, line group highway switch I, line group highway switch II, and frame tone generator. The X cell contains the maintenance and diagnostic controller and the Y cell contains the line test controller and the automatic line insulation test (ALIT) circuit. The major control circuits are shown in figure 10.

6.02 Control Elements.

The DCO system uses a distributive processing system of control. The 11 units of microprocessor control are as follows:

a. Line Switch Controller.

By way of a high speed digital control loop, the on-line circuit handles all functions necessary to service and control 1,080 lines.

b. Maintenance and Diagnostic Controller.

1. Controls first- and second-level diagnostics in the LLS frame.

2. Provides watchdog timing control.

3. Controls 24-hour X/Y switchover and diagnostics.

c. Line Test Controller.

1. Provides continuous LLS line origination testing.

2. Routines all LLS lines every 24 hours.

3. Contains analog transmission test circuits.

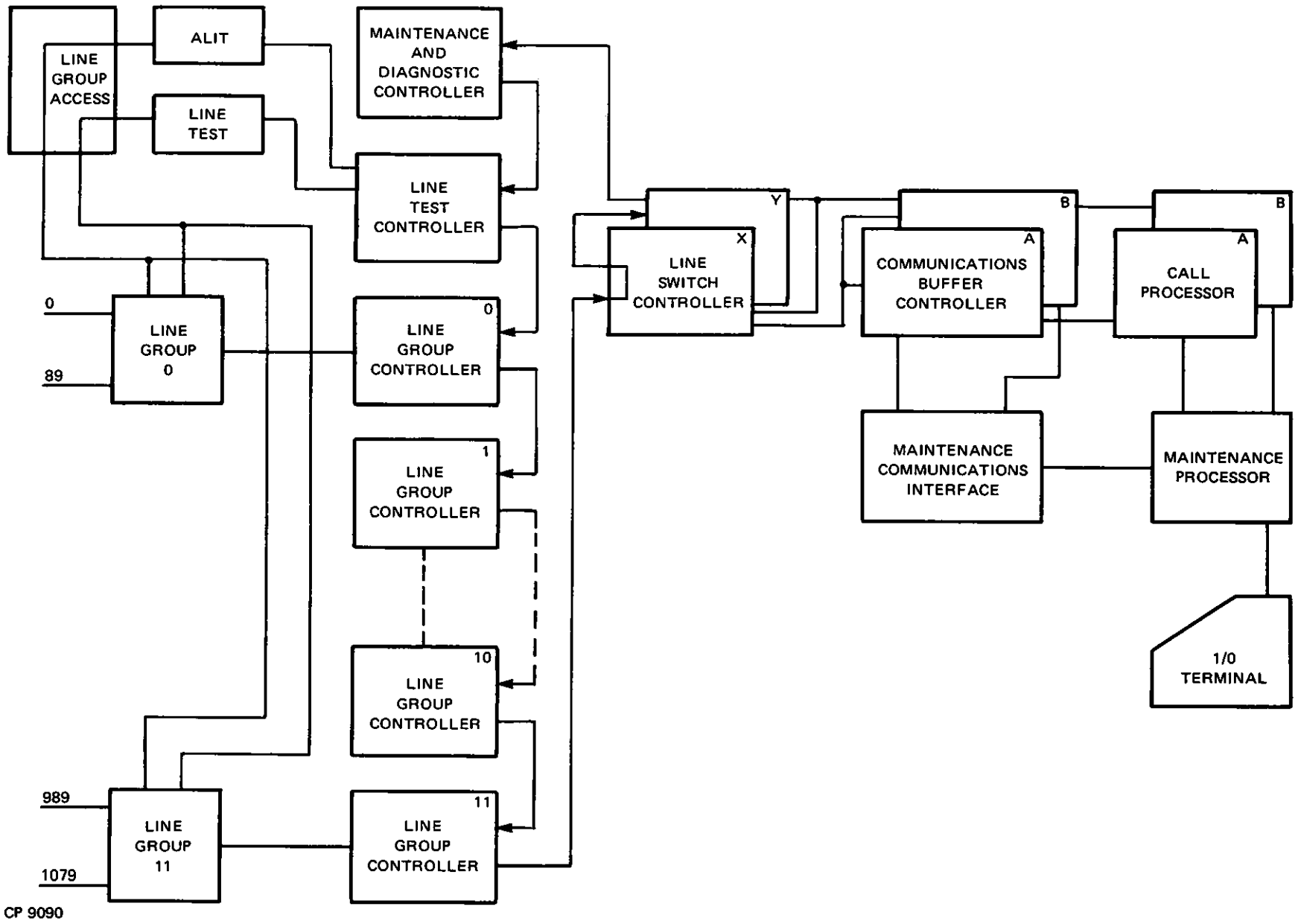

Figure 10. Control Circuits

d. Automatic Line Insulation Test (Optional).

1. Contains ALIT hardware and software controls.

2. Tests outside plant.

e. Communications Buffer Controller.

1. An auxiliary call processor that handles up to eight LLSs by way of a high speed data link.

2. Serves as interface between call processor and line switch controller.

3. Serves as interface between maintenance communications interface and line switch controller.

f. Maintenance Communications Interface.

This circuit is the interface for all LLS maintenance, administration, and test functions between the line switch controller and maintenance processor.

g. Line Group Access.

1. Provides metallic test bus access to line circuits (3 in and 3 out buses per line group).

2. Connects lines to auxiliary test equipment.

3. Puts virtual spare line in service as required.

h. Line Group Controller.

Provides all control functions (off-hook detection, ringing, status, relay control, etc.) for 90 lines.

i. Line Test.

1. Provides test control functions to IN bus for the line test controller.

2. Simulates loop or ground start, ANI, sleeve lead, and dial pulse closures to line under test.

3. Used by line test controller to initiate the continuous origination test for each line.

j. Maintenance Processor.

1. Provides all maintenance and administration.

2. Controls man/machine interface for up to four input/output terminals.

3. Provides two levels of system diagnostics.

k. Call Processor.

1. Performs call processing route selection and control for all connections.

2. The redundant processors operate in a bit-by-bit synchronized mode. Both processors receive digits, translate, and set up call paths.

6.03 Line Switch Controller.

The line switch controller (fig. 11) is the LLS interface to the call processors and maintenance processor. Communications between the line switch controller and the processors is by way of redundant communications buffer controllers on an SDLC loop (par. 4). The line switch controller is also part of another SDLC loop (peripheral control) that serves the LLS frame.

a. Communications Buffer Controller SDLC Loop.

In this SDLC loop (fig. 12), the on-line communications buffer controller is the master station and the line switch controllers in up to eight LLS frames are the slaves. If a line switch controller is removed or the maintenance communications interface circuit forces a bypass, relays close to maintain the loop without that line switch controller. The identity of the bypassed circuit is sent to the maintenance processor.

b. Peripheral Control SDLC Loop.

In this SDLC loop (fig. 13), the on-line line switch controller is the master station; the slaves are the off-line line switch controller, line group

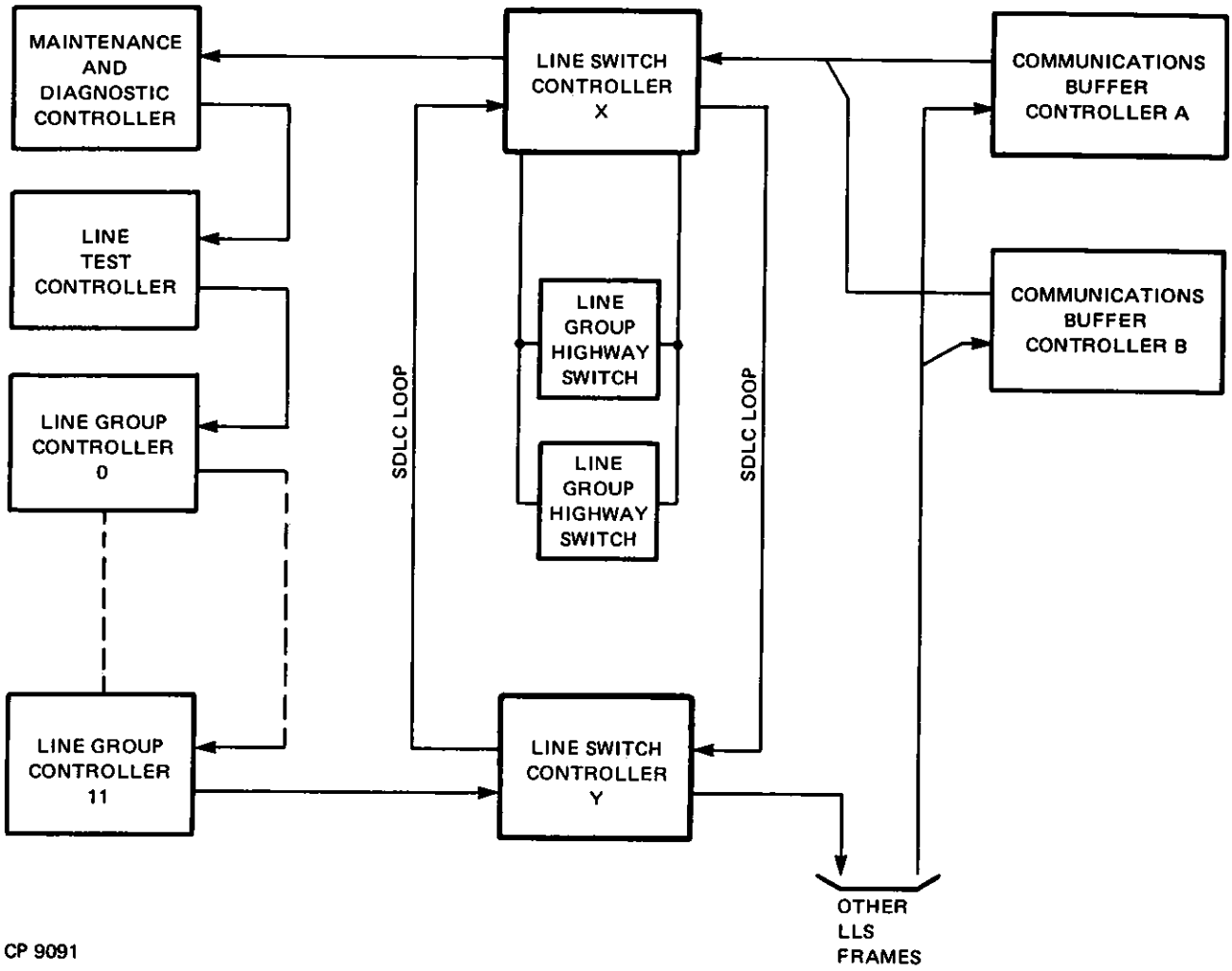

Figure 11. Line Switch Controller, Orientation Diagram

controller, line test controller, and maintenance and diagnostic controller. As with all SDLC loops, a missing or faulty slave station is bypassed to maintain loop integrity. *Two consecutive slaves, however, cannot be removed from the loop at the same time.*

c. Line Switch Controller Functions.

The functions of the line switch controller are as follows:

1. Receives ringing relay control data from the ring serializer, by way of the line group highway switch. The line switch controller extends the signals to the line group controller over the SDLC loop. The ring data can also be provided to the line switch controller by a local ringing generator.

2. Designates which redundant line group highway switch is to be enabled onto the line switch controller data bus during a read cycle. The on-line line switch controller writes to both line group highway switches.

3. Supplies the basic clock for the line switch controller microprocessor and supplies clock signals to the interrupt vector generator in the line switch controller and to the two associated SDLC loops.

4. A watchdog circuit sends an alarm to the maintenance and diagnostic controller if the line switch controller software fails to report periodically.

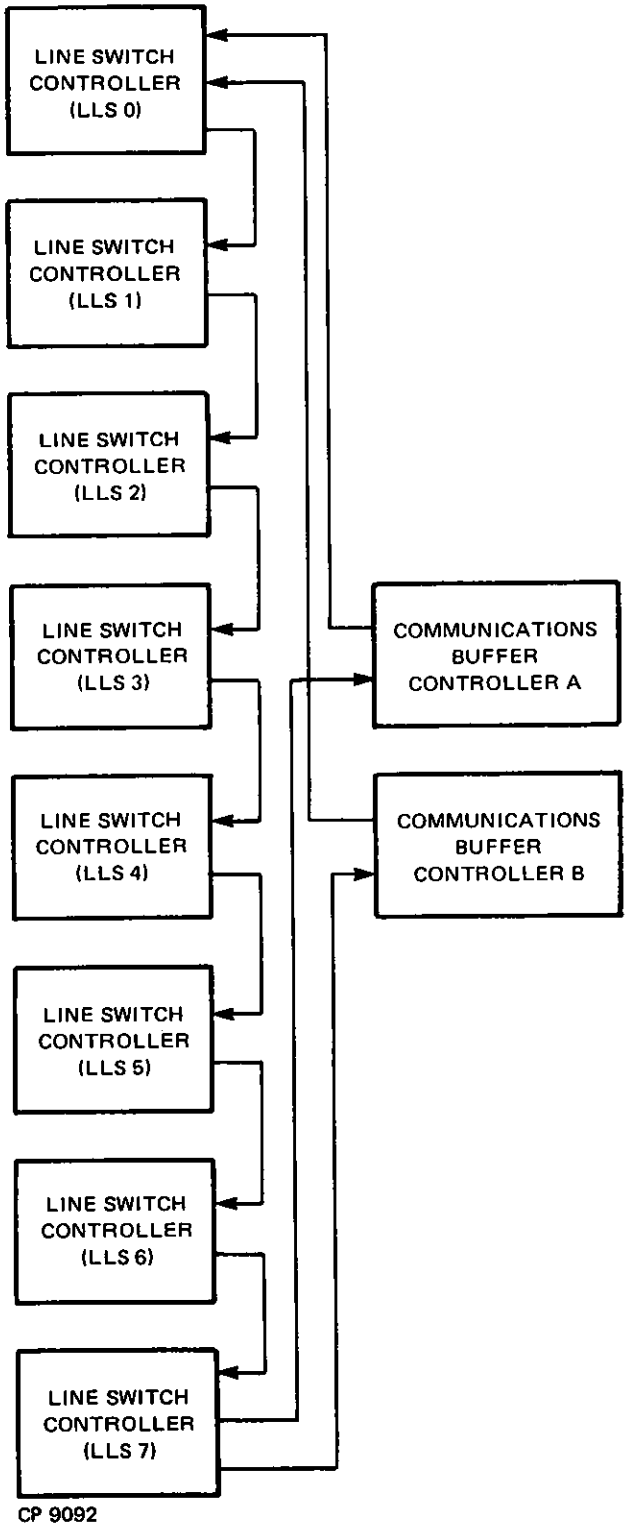

Figure 12. Communications Buffer Controller/Line Switch Controller SDLC Loop

6.04 Line Group Highway Switch I.

a. Each redundant (C and D) line group highway switch I multiplexes data from the 36 line group highways onto 8 port group highways and demultiplexes data in the opposite direction. Line group highway data can be gated to any port group highway and port group highway data can be gated to any line group highway. See figure 14.

b. The line group highway number and path information are stored in RAMs in line group highway switch I. The information is gated into the RAM by control signals from line group highway switch II. The line group highway number is written into a specific timeslot (0-29) in the RAM, where the line group highway/timeslot association is maintained.

c. Data from the line group mux/demux is presented to the 36-to-8 selectors. The line group highway number (0-35) is also sent to the 36-to-8 selectors. The stored line group highway number is then used to select the gates required to pass data to the port group highways, by way of line group highway switch II.

d. Data from the port group highways is received by way of line group highway switch II and applied to the 8-to-36 selectors. The line group highway number stored in the RAM (par. b) is applied to the 8-to-36 selectors so that the port group highway data can be gated to the proper line group highway. The data is then sent to the line group mux/demux.

6.05 Line Group Highway Switch II.

a. Line Switch Controller Communications.

1. The line switch controller provides port group highway, timeslot, and line group highway numbers to line group highway switch II (fig. 15) each time a path is to be set up or broken. The line switch controller also tells line group highway switch II when to provide a voice pattern test on an established path. Upon test completion, an

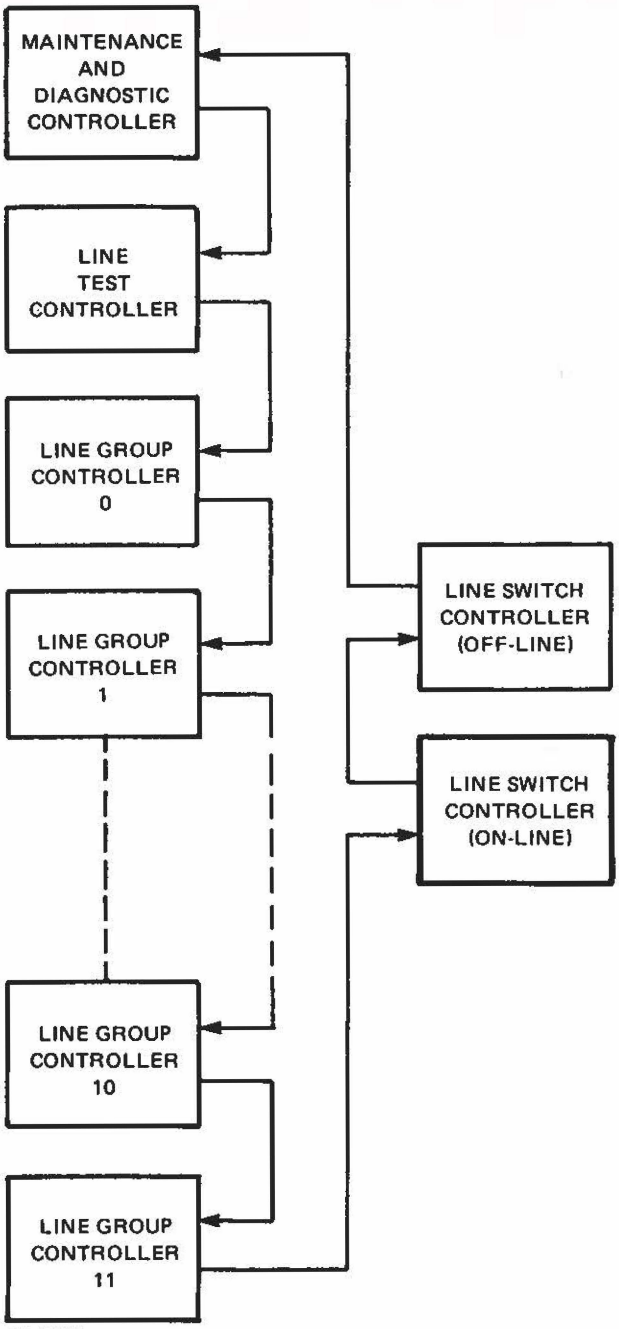

Figure 13. Peripheral Control SDLC Loop

interrupt is sent to the line switch controller which reads the test results.

2. Tones from the frame tone generator can be applied to any line group highway by way of line group highway switch I. Control data from the line switch controller determines the tone, timeslot, and line group highway.

3. A data mismatch between the C and D line group highway I switches causes line group highway switch II to send an interrupt to the line switch controller. For diagnostic purposes, the line switch controller can force C/D mismatches and also A/B port group highway mismatches.

b. A/B Mismatch Reporting.

Any data mismatch between the A and B port group highways is reported to the timeslot interchange diagnostics circuit.

c. A/B and C/D Select.

The A/B control lead from the timeslot interchanges diagnostics circuit is monitored to determine which set of port group highway timing and control signals to use. The C/D control lead is monitored to determine which line group highway switch pair (I and II) is to be on-line.

d. Alternating Supervisory Bits.

During timeslot 31, supervisory bits from the receive port group highways are looped back to the transmit port group highways to check for transmission errors.

6.06 Frame Tone Generator.

The frame tone generator (fig. 16) has the following functions in conjunction with line group highway switches I and II:

a. Runs voice pattern tests when instructed by the line switch controller. A voice pattern tone generator on the frame tone generator PWBA sends a digital pattern to line group highway switch II, where the bits are inserted into the receive port group highway. The bits are steered to the assigned line group highway and then the line group mux/demux loops the bits back to line group highway switch I, where they are stripped off at the port group highway transmitters. The frame tone generator compares the bits sent with those received and reports the results to the line switch controller, by way of line group highway switch II.

b. Runs self tests on the voice pattern test circuitry, under control of the line switch controller.

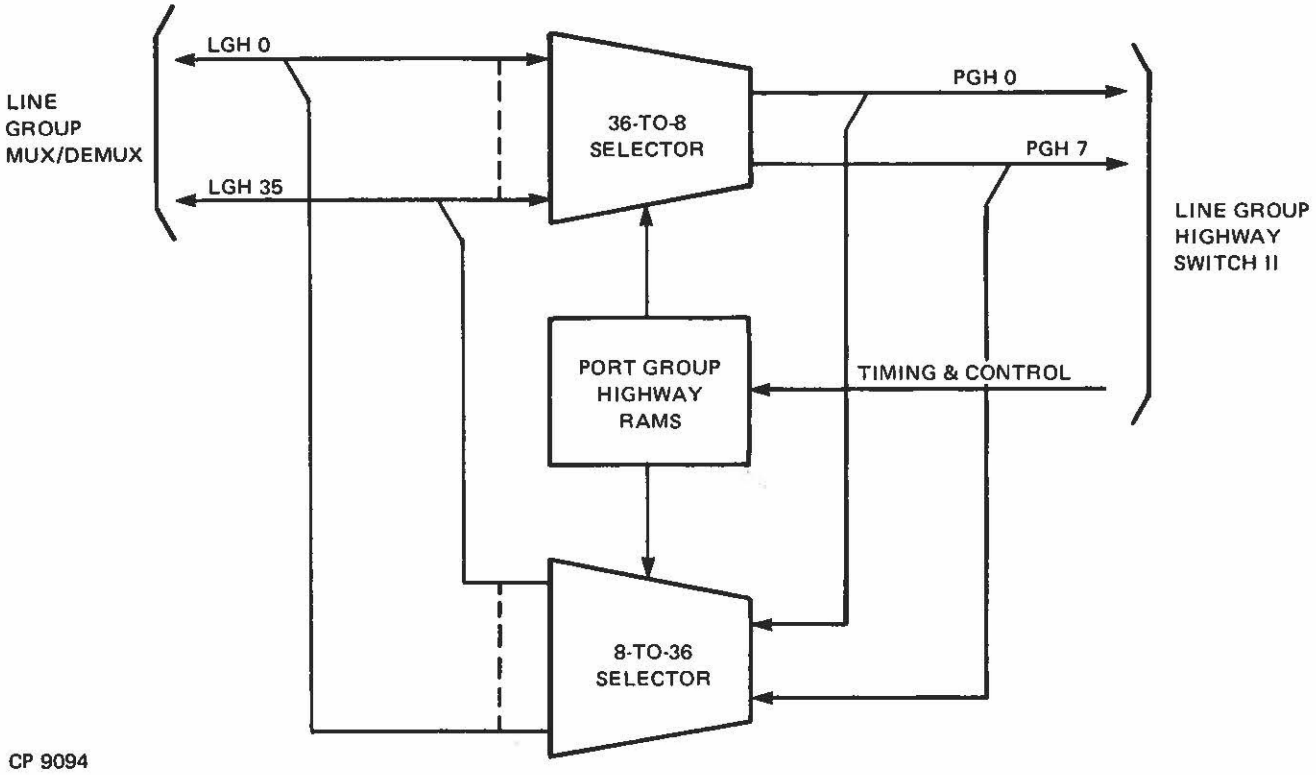

Figure 14. Line Group Highway Switch I, Block Diagram

c. Supplies digital receiver-off-hook tone information to line group highway switch II for distribution to the line group highways. Digital information is stored on the frame tone generator PWBA before being sent to line group highway switch II. Timing from the port group highway is used to provide the proper sequencing of digital data to the line group highways.

d. Timing signals (2 MHz and 4 ms) are normally received by line group highway switch II from the port group highways. If these signals fail, emergency timing is provided by the on-line line switch controller. The selection and distribution of these signals is done by the frame tone generator.

6.07 Maintenance and Diagnostic Controller.

a. The non-redundant maintenance and diagnostic controller (fig. 17) is the gathering point for alarms and status changes in the LLS. If a fault is detected in a redundant circuit, the maintenance and diagnostic controller causes the faulty circuit to be taken off-line and sends an alarm to the line switch controller, which passes it on to the maintenance processor. The maintenance and diagnostic controller is mounted in and powered by the line switch controller X cell. If an X side power failure occurs, however, the maintenance and diagnostic controller receives power from the Y side.

b. The inputs to the maintenance and diagnostic controller include:

1. Power alarms.
2. Parity error from line switch controllers.
3. Watchdog timeouts.
4. Peripheral control SDLC loop.
5. Manual on-line select.
6. Customer alarm signals.

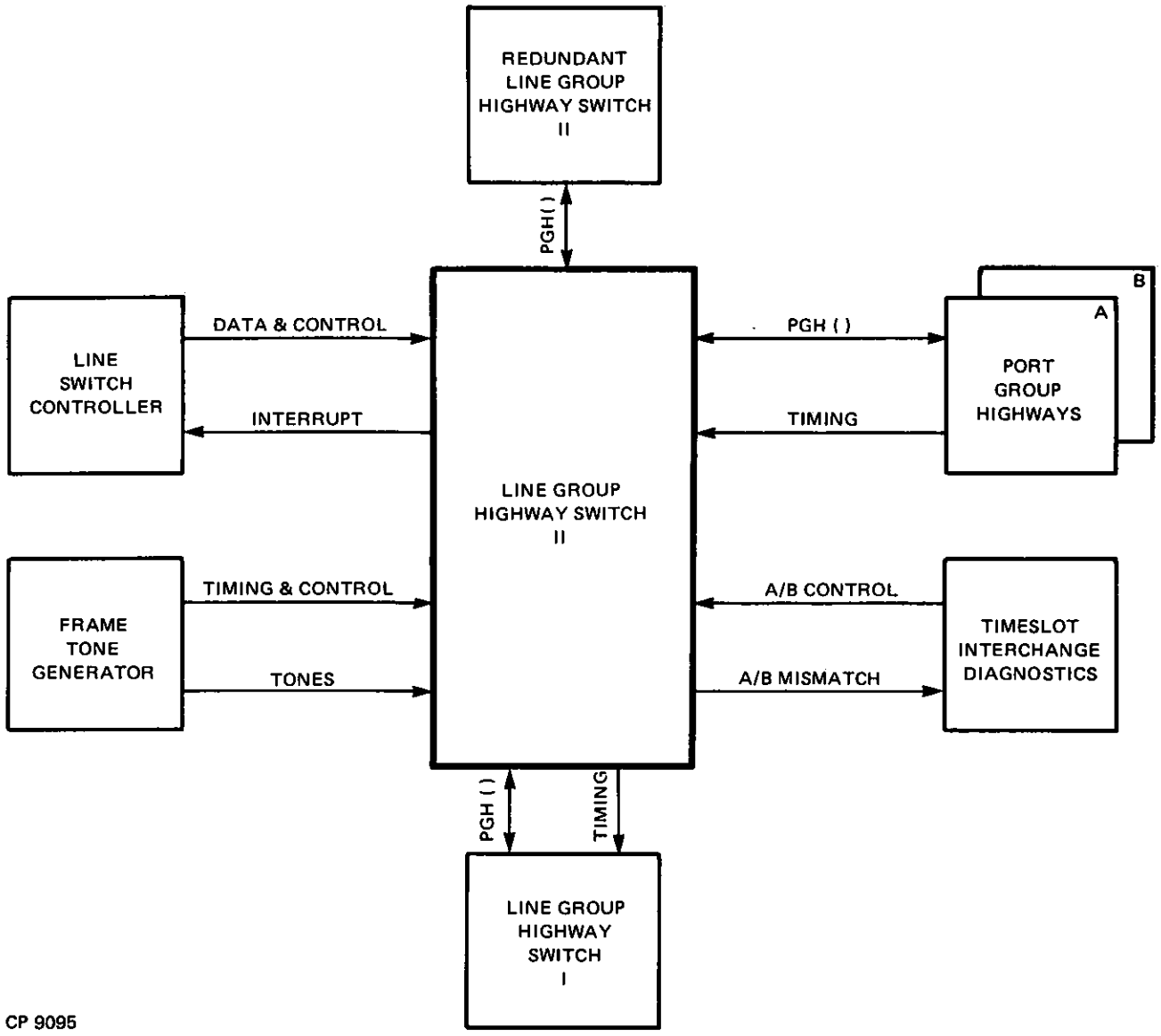

Figure 15. Line Group Highway Switch II, Orientation Diagram

c. Using the above inputs, the maintenance and diagnostic controller microprocessor provides the following outputs:

1. Peripheral control SDLC loop bypass.
2. Line group controller bypass relay signals.
3. Line group controller reset.
4. Line test controller bypass signals.
5. On-line select signals for line switch controllers and line group highway switches.
6. Control signals for customer-provided equipment.

d. The maintenance and diagnostic controller is a slave unit in the peripheral control SDLC loop. Before removing the maintenance and diagnostic controller PWBA, the redundant line switch controller and line group highway switches I and II must be locked to prevent switchover.

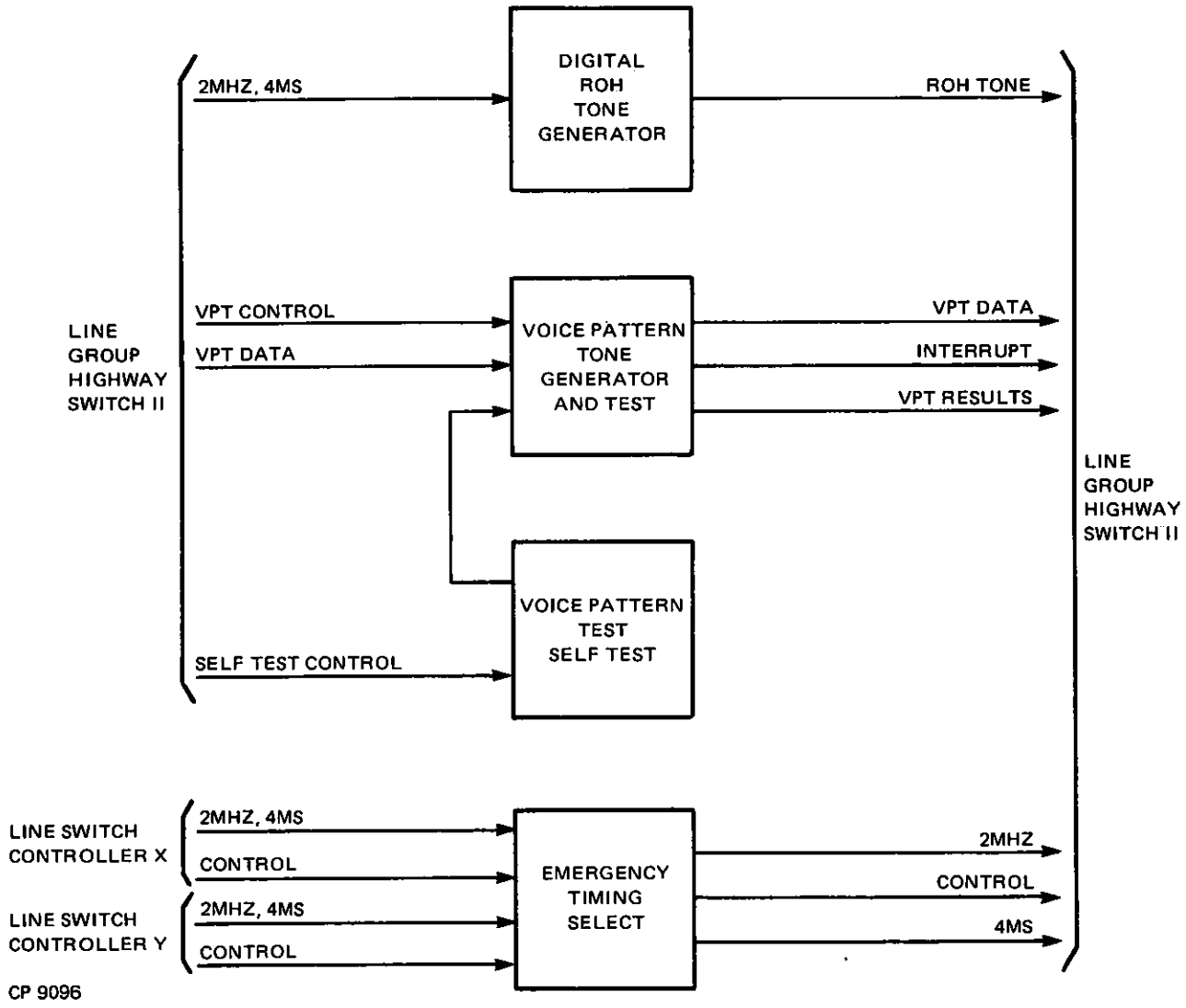

Figure 16. Frame Tone Generator, Block Diagram

6.08 Line Test Controller.

a. The line test controller (fig. 18) consists of two PWBAs in the Y line switch controller cell. The circuit is used for LLS line routining, making automatic line insulation test (ALIT) measurements, and party identification. The line test controller, under control of the line switch controller and maintenance processor, automatically generates test calls over LLS lines by simulating the actions of subscribers. Proper system responses and communications paths are checked at various stages of each call.

b. An origination test is scheduled every 10 seconds by the maintenance processor. The line switch controller causes a test access path to be set up between the selected line and the line test controller and then commands the line test controller to do the origination test. The line test controller establishes an off-hook condition for the line, resulting in a transmission path being set up and dial tone being returned to the off-hook line. The line test controller detects dial tone, dials the digit 1, and detects dial-tone removal when the digit is received by the system. The line test controller then puts the line on-hook and disconnect is reported by the call processor.

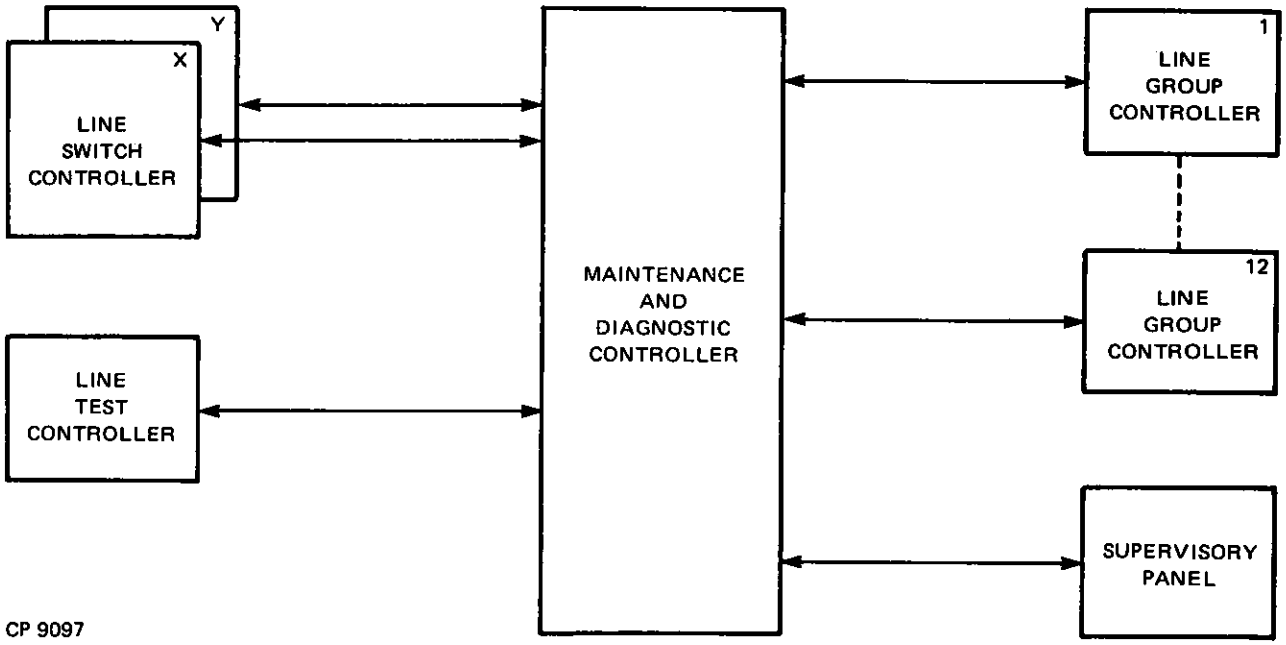

Figure 17. Maintenance and Diagnostic Controller, Orientation Diagram

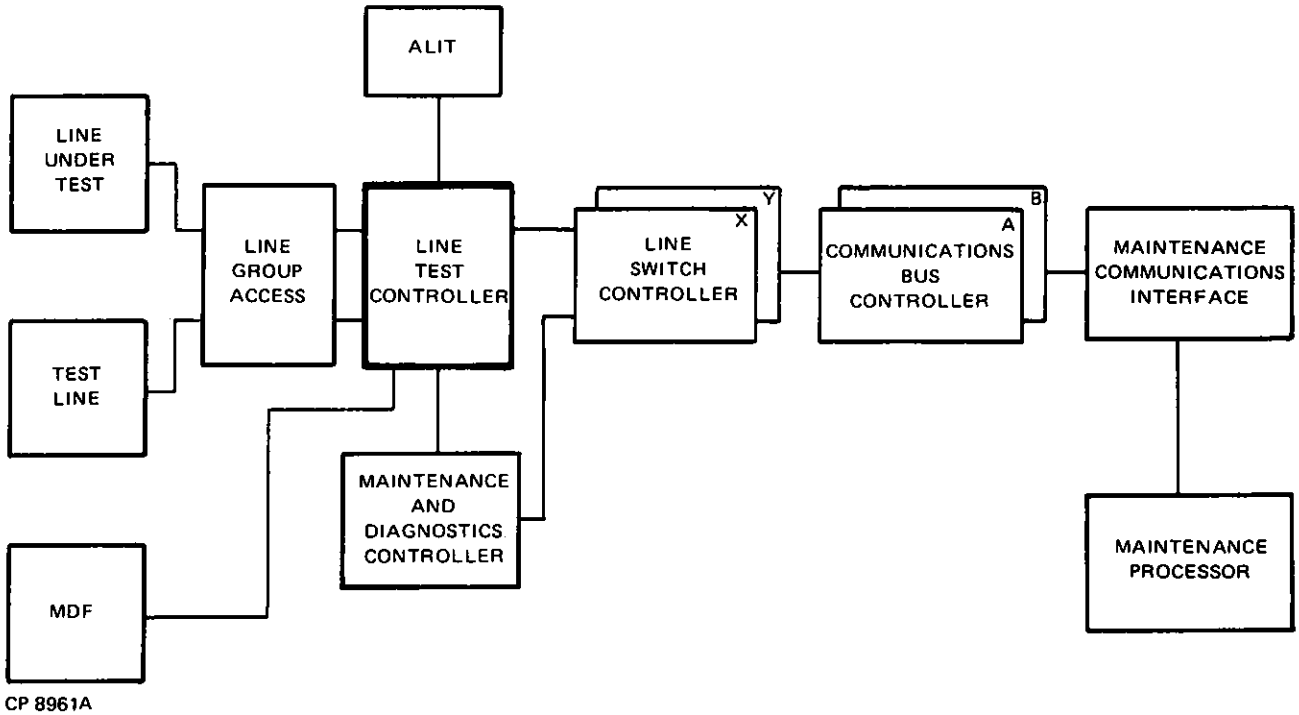

Figure 18. Line Test Controller, Orientation Diagram

c. Line routining provides a thorough test of all LLS line circuits once a day. In addition, the voice path, supervisory paths, and most of the control functions are tested. If ALIT is provided, a test of the subscriber line is done at the same time as the line circuit is being tested. Line routining is usually done at night during low traffic periods.

1. Before testing is started, the line test controller does a self check. The line switch controller then selects a line for testing and checks that it is equipped and idle. If busy, the line is put on a test-later list; if idle, a metallic path is set up between the line and the line routiner in the line test controller.

2. After some initial checks, the line test controller goes off-hook and dials a 3-digit code to establish a voice path from the line under test, through the system, and back to a dedicated LLS line that has a direct-wired access to the line test controller. The line test controller makes a noise test on the path, tests voice transmission by generating and detecting a tone in each direction, and releases the voice path.

3. Line circuit relay functions (ringing, tip and ring reversal, etc.) are now checked by generating supervisory control bits in the line test controller and monitoring the results. The test access path is released and the next line to be tested is selected.

6.09 Automatic Line Insulation Test.

a. The optional ALIT PWBA is mounted in the Y line switch controller cell. The circuit contains all hardware required for ALIT operation except for the actual measurement recording device, which is an 8-bit analog-to-digital converter in the line test controller. The ALIT circuit is completely controlled by the line test controller. The ALIT PWBA contains a 60-Hz rejection filter, a constant current source for measuring resistance, a voltage ramp generator for measuring capacitance, and relays for connecting these measuring devices to the tip and ring leads and to the line test controller in the proper sequence. During ALIT operation, the LLS line circuit is split into an inward and outward section. While the line test controller checks the line circuit inward, the ALIT circuitry checks the outside plant.

b. The purpose of ALIT is to find outside plant problems before they affect a subscriber's ability to make and receive calls. Tests made on the outside plant include insulation (leakage), capacitance, foreign voltage (ac and dc), and noise. The noise measurement determines the differential voltage across tip and ring.

c. If ALIT is done concurrently with line routining, the ALIT unit provides a set of line measurement values to the line switch controller by way of the line test controller. The line switch controller compares the measurements with a set of established threshold values, if any measured value exceeds the threshold the tests are repeated. If the second test shows the same discrepancy the maintenance processor is notified.

7. INTERFACE TO COMMON EQUIPMENT

7.01 General.

The line switch controllers transfer control data to and from the common equipment call processors and maintenance processor by way of the communications buffer controller and maintenance communications interface. These PWBAs are located in the maintenance and administration frame. The exact location is provided in the section titled *Equipment Location*, referenced in paragraph 2.02.

7.02 Communications Buffer Controller.

a. The communications buffer controller (fig. 19) is a message switch for control data between the line switch controller and the call processors or maintenance processor. Each redundant communications buffer controller pair serves up to eight LLS frames; up to four communications buffer controller pairs can interface each pair of redundant call processors.

b. The communications buffer controllers are connected to the redundant call processor data buses and the maintenance communications

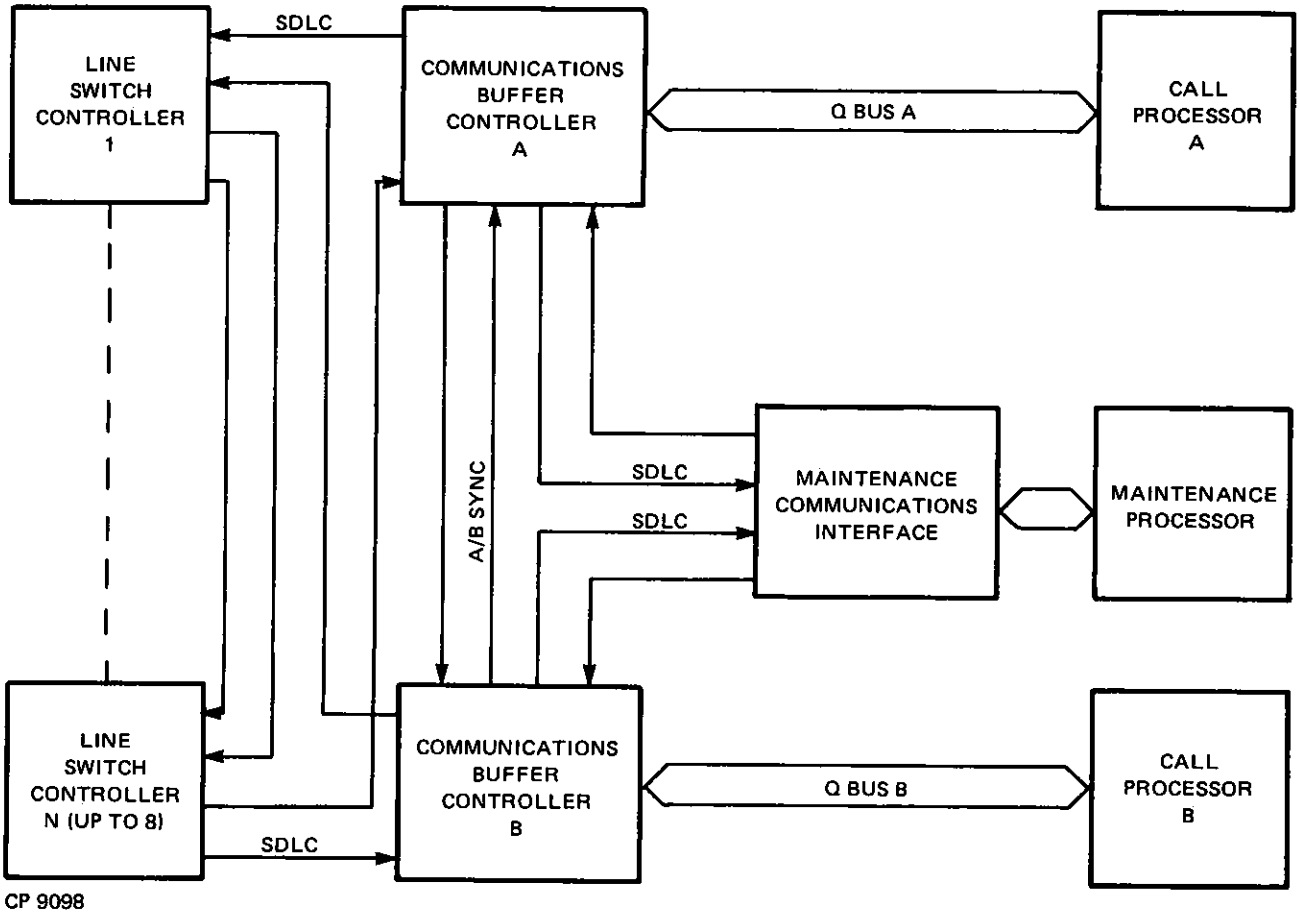

Figure 19. Communications Buffer Controller, Orientation Diagram

interface. The communications buffer controllers are synchronized and the two outputs are compared before a message is sent to the call processors. Messages from the call processors to the communications buffer controller are held in a RAM and applied to the communications buffer controllers only when the redundant units are synchronized.

c. On messages from the communications buffer controllers to the line switch controllers, the outputs of both communications buffer controllers are sent to both line switch controller cells. Either the A or B communications buffer controller signal is selected and applied to the line switch controllers.

d. As previously stated, the on-line communications buffer controller is the master on an SDLC loop and the line switch controllers in up to eight LLS frames are the slaves. Each pair of communications buffer controllers are also slaves on another SDLC loop on which the maintenance communications interface is the master. See figure 19.

7.03 Maintenance Communications Interface.

a. Each communications buffer controller pair interfaces to the maintenance processor through a dedicated maintenance communications interface (MCI). Up to four MCI circuits can interface the maintenance processor.

b. The MCI has independent connections to the A and B communications buffer controllers to permit synchronous communications with both or exclusive communications with either communications buffer controller. Service requests from the communications buffer controller are converted to the proper format and passed on to the maintenance processor as interrupts.

c. Commands from the maintenance processor are analyzed and converted by the MCI and then sent to the LLS by way of the communications buffer controller. Microprocessors in the communications buffer controller are also reset by the maintenance processor by way of the MCI.

8. TECHNICAL CHARACTERISTICS

8.01 Traffic Capacity.

Based on erlang B tables at a grade of service of .003, the capacities in table 1 are provided by the LLS.

8.02 Loop Resistance Ranges.

The minimum dc insulation resistance and ringer load are defined by various loop resistance ranges that include telephone instruments, as listed in table 2. The dc insulation resistance refers to the minimum resistance between line conductors or between either or both conductors and ground without any line attachments. The ringer load assumes high-impedance ringers. It provides adequate audibility of all signals at maximum loop resistance without premature ring trip at minimum loop resistance.

8.03 Service Selection.

The flexibility of the LLS permits service additions in accordance with PWBA selection. Table 3 shows the various line PWBA types that can be used.

Table 1. Traffic Capacity

NO. OF CHANNELS	*AVAILABLE CCS*	*NO. OF LINES*	*CCS/LINE: ORIGINATING/TERMINATING*
60	1,692	1,080	1.6
240	6,768	1,080	6.3

Table 2. Subscriber Line Loop Resistance Ranges

LOOP RESISTANCE (ohms)	*DC VOLTAGE (volts)*	*MINIMUM INSULATION RESISTANCE (ohms)*	*RINGER LOAD*
0 to 1,500	44 to 54	15,000	17 ringers or one three-line common audible
0 to 1,900	51.6 to 54	25,000	10 ringers or one three-line common audible
1,900 to 4,500	51.6 to 54 with loop range extenders.	100,000	Six ringers or one three-line common audible

Table 3. Line PWBA Type and Service Provided

LINE PWBA TYPE	*NO. LINES/PWBA*	*SERVICE PROVIDED*
817541-026	6	Bridged Ringing, ANI
817541-046	6	Bridged/Divided Ringing, ANI, Reverse Battery
817543-026	3	Ground or Loop Start, Sleeve Lead (two-way)
817545-526, 536	3	Prepay Coin

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