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SYSTEM CENTURY R
DIGITAL CENTRAL OFFICE

COMMON CONTROL
DESCRIPTION AND OPERATION

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

1. INTRODUCTION

1.01 This section provides functional descriptions of the circuits that make up the common control of a SYSTEM CENTURY Digital Central Office (DCO) equipped with a local line switch (LLS).

2. RELATED INFORMATION

2.01 General.

A Sales and Instructional Literature Index of latest available publications can be obtained from your Stromberg-Carlson sales representative or from Publications Services, Stromberg-Carlson Corporation, P. O. Box 1698, Sanford, Florida 32771.

3. FUNCTIONS OF COMMON CONTROL

3.01 General.

The common control is composed of two circuit groups: the telephony preprocessor and the controller circuits. One common control serves 8 timeslot interchanges (TSIs) that, in turn, serve up to 8 port group highways (240 channels) from LLS or trunk frames. Port group highways can be distributed as desired to LLS or trunk frames. Each LLS has from 2 to 8 port group highways spread across up to 8 TSIs. Redundant common controls are provided to enhance system reliability and ensure service continuity. Figure 1 shows the functional relationship of the common control to other circuits in the SYSTEM CENTURY DCO.

3.02 Telephony Preprocessor.

a. Trunks.

The telephony preprocessor does all real-time dependent functions for the trunks associated with it. It communicates with the call-processing system (CPS) by way of the controller circuits with status information, port control store memory access, and queue information, and with the trunk by means of supervisory sense and control bits developed in the telephony preprocessor. The telephony preprocessor also con-

tains a dedicated storage area (port control store) for each trunk. This storage area is used to store all current information required to service a trunk. This information includes type of port, call state (off-hook, ringing, etc.), dialed digita, etc.

b. Lines.

The main functions done for lines are receipt of dialed digits and sending of supervisory information. All other functions are handled by the line switch controller. Another difference for LLS is that each port control store serves one port group highway timeslot and is assigned a common port type for all LLS/port group highway timeslots.

3.03 Controller Circuits.

a. The timeslot interchange controller, port store controller, and crosswrite circuits provide the interface required for the call processors to communicate with the port control store and the TSI. They enable the CPS to read out of, write into, and search the TSI stores. The TSI number and CPS commands are decoded by the controller and the required control signals are then sent to the TSI to do the appropriate functions, such as writing and reading of call data and searching for receive equipment numbers.

b. For LLS, redundant communications bus controller (CBC) circuits provide an interface between the call processors and the LLS line switch controller (LSC). Each CBC pair also interfaces with the maintenance processor through a maintenance communications interface (MCI).

4. COMMON CONTROL CIRCUITS

4.01 General.

Figure 2 is a block diagram of the common control, showing how

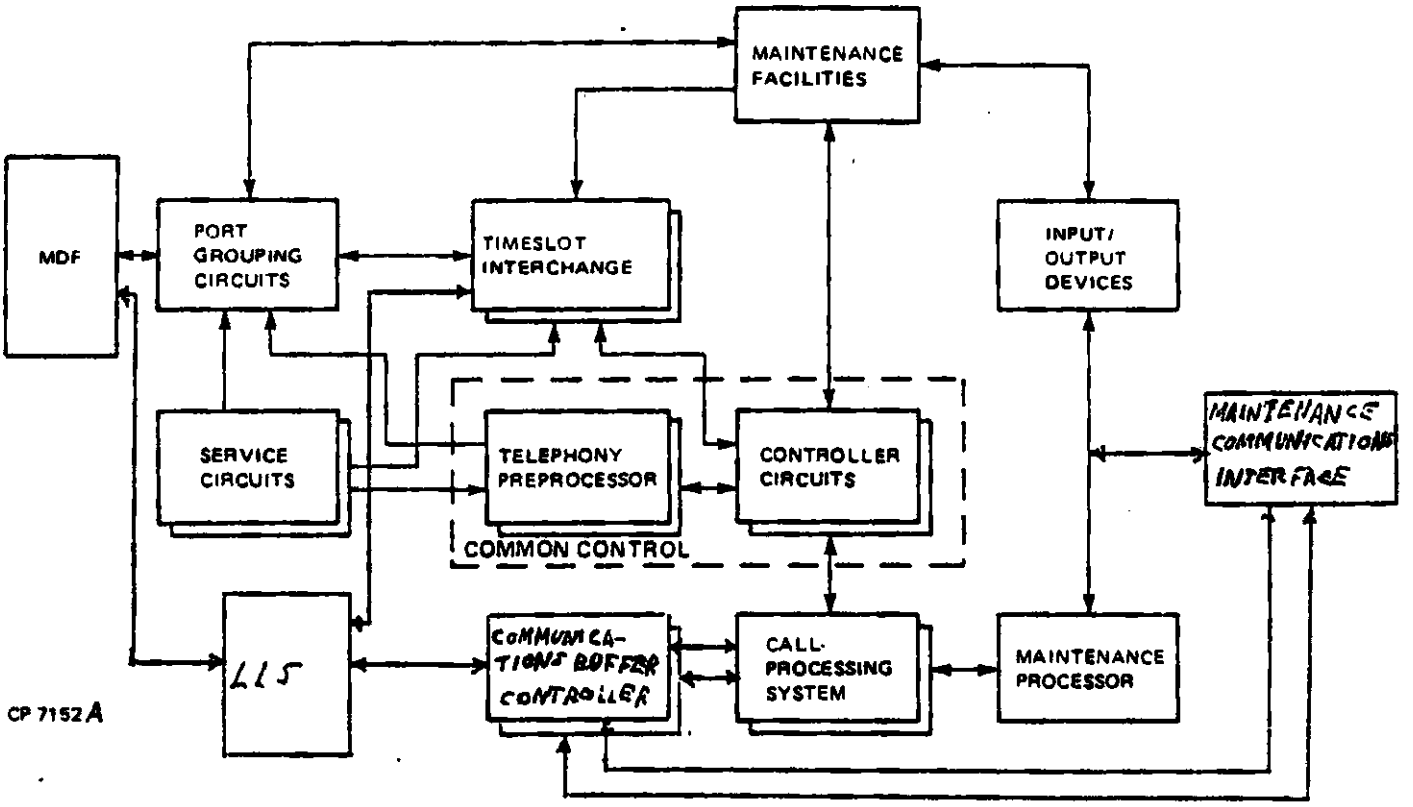


Figure 1. Common Control, Orientation Diagram

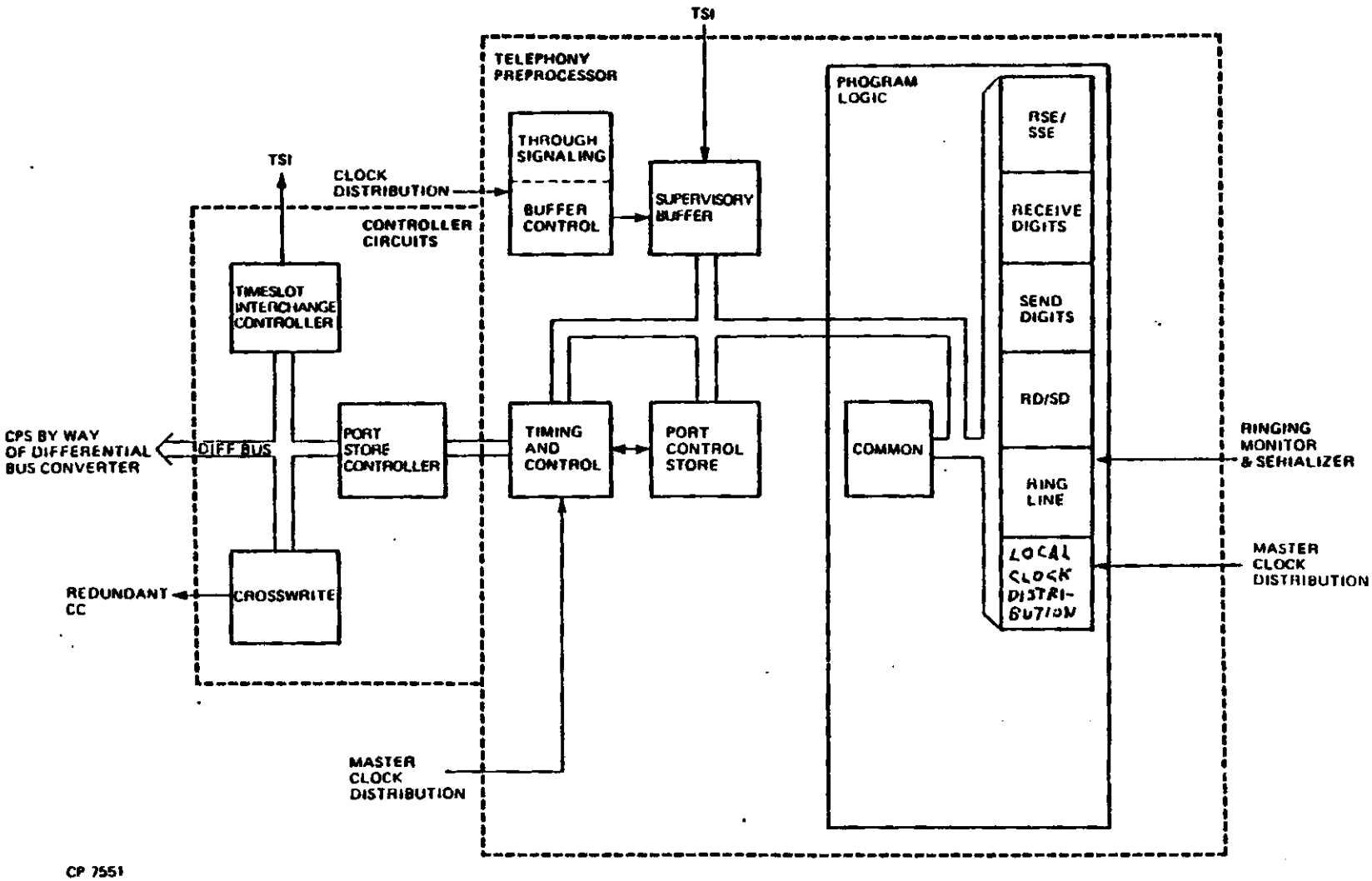


Figure 2. Common Control, Block Diagram

the circuits interconnect with each other and with associated circuits in the DCO system. A brief description of each common-control circuit is provided in the following paragraphs.

4.02 Timeslot Interchange Controller.

The timeslot interchange (TSI) controller is the interface between the CPS and the TSI. One TSI controller printed wiring board assembly (PWBA) is required for each common control. The TSI controller works in conjunction with the port store controller and the crosswrite circuit to provide CPS access to the telephony preprocessor. The TSI controller is made up of the following circuit elements:

a. Differential Receivers.

The differential receivers convert control signals from the differential bus (differential extension of CPS bus) to logic levels for use by ther TSI controller, port store controller, and crosswrite logic circuits. The differential bus provides high noise immunity. These control signals are used to do the following:

1. Identify when CPS is addressing the input/output memory locations.

2. Control direction of data transfer between the CPS and TSI.

3. Strobe address into the TSI controller from the CPS (by way of the crosswrite circuit).

4. Clear TSI registers.

5. Send controller acknowledge signal to CPS.

b. Address Register and Decoder.

These circuits allow the CPS to select one register on a TSI

controller. Each register has a unique address to which it responds.

c. TSI Command Register.

The information stored in this register by the CPS is used to enable a specific TSI and command it to do a particular operation.

d. TSI Address Register.

The information stored in this register by the CPS is used for transfer of call data from the CPS to the TSI enabled by the TSI command register. The lower byte contains the data, and the upper byte contains the addresses that specify the location in the TSI into which the lower byte is written.

e. TSI Command Response Logic.

This logic monitors responses from the TSI selected by the TSI command register. If a response is not received within a specified time, an error signal is generated.

f. Redundant-Signal Comparison Circuitry.

To detect controller or TSI failures, the two redundant controller-TSI data and control paths are compared on each operation. The result is sent to the TSI/port control store (TSI/PCS) diagnostics circuit.

4.03 Port Store Controller.

The port store controller is the interface between the CPS and the telephony preprocessor. One port store controller PWBA is required for each common control. The port store controller provides call data and status information to the CPS through registers that are addressed by the CPS in the same way that it addresses a memory location. Data is transferred to and from the CPS over a 16-bit bus by way of the crosswrite circuit. The port store controller is made up of the following elements:

a. Port Store Word Registers.

Sixteen 16-bit port store word registers are used for access to

the 16 words in the port store area for each port. A 16-bit bus transaction is initiated when the CPS addresses a port store word register, a control signal indicating direction of transfer is received from the TSI controller (par. 4.02a), and a start signal is received from timing and control.

b. Port Store Data Register.

This register is used to temporarily store 16 bits of data being transferred between the port control store and the CPS. The data is clocked into this register by signals from timing and control.

c. Port Store Mask Register.

When a word is written back into the port control store, a mask is first clocked into the port store mask register from the CPS to indicate which bits are to be changed from what is currently stored. A 16-bit word is then clocked into the port store data register from the port control store and from the CPS, depending on the mask. Timing and control strobes the word to the port control store.

d. Crosswrite and Compare Circuitry.

The crosswrite operation is used to copy data (16 bits at a time) from the on-line to the off-line port control store. The compare operation compares the data in the on-line and the off-line port control stores. Any differences are reported to the TSI/PCS diagnostics by way of the crosswrite circuit.

4.04 Crosswrite.

The crosswrite circuit controls the crosswrite and compare functions. The circuit also provides an interface for data between the differential bus and the TSI controller and port store controller circuits. One crosswrite PWBA is

required for each common control. The crosswrite is made up of the following circuit elements:

a. Differential Bus Interface.

This circuit is used to transfer data and addresses between the differential bus and the port store controller and TSI controller. On transfers to the controllers, parity of the differential bus data is checked and any errors found are returned to the differential bus. On transfers to the differential bus, data parity is generated and sent with the data.

b. Crosswrite and Compare Circuitry.

This circuitry operates in conjunction with the crosswrite and compare circuitry in the port store controller.

4.05 Timing and Control.

The timing and control circuit, operating on a 1.953-micro-second cycle, generates the control signals required to make data transfers between the controller circuits, port store area (PSA) of the port control store (PCS), and program logic (PL) circuits. Three priority queues are also provided for storing equipment (port) numbers that need CPS processing (those equipment numbers having active event codes). One timing and control PWBA is required for each common control. The timing and control circuit includes four interface circuits as described in the following paragraphs.

a. PL Interface.

The PL interface receives inputs from the PL, to indicate when to write the equipment number in queue, and an indication that a second read/write access is required to complete the processing of a port. The PL latches the first and second read data into the PL registers from the PSA and writes data into the PSA.

b. Clock Distribution and Maintenance Interface.

This interface receives the 8.192-MHz clock signal and distributres it throughout the timing and control circuit. A 4-millisecond synchronization pulse from the clock distribution circuit is used to check for synchronization errors and to reset internal counters in the timing and control circuit.

c. Port Control Store Interface.

The PCS interface receives inputs from the PCS to enable storage, in the proper queue, of the equipment number that has an event code to report. Parity errors are also received from the PCS. Outputs to the PCS include the 12-bit address of the storage location for the port being served, and read, write, and memory-enable signals. Enable signals are also provided to gate data into and out of the controller circuits.

d. Controller Interface.

The controller interface includes 12 bidirectional lines that either are used to send the address of a PCS (PSA) memory location to timing and control or are used by timing and control to transfer an equipment number from queue to the port store controller. Signals are received from the controller to indicate that it either requires a PSA memory access or wants to read the contents of a queue. Timing and control provides signals to the controller indicating queue status, or the completion of a memory cycle, and to gate data into and out of the controller.

4.06 Port Control Store.

a. Each of the DCO trunks served by a common control is allotted 256 bits of storage (one PSA). For lines, 240 PSAs can serve as many as 1080 lines. The PCS contains random access memories

(RAMs) for storing port information and address selectors for selecting a particular port store area in a RAM. The PCS also contains parity-check circuitry and tristate buffers for use with bidirectional input/output buses. Four PCS PWBAs are required for each common control.

b. The PSA bit layout for the 256-bit storage area of one port is shown in figure 3. The layout shows the data read operations. Because the CPS bus has a 16-bit capacity, each CPS read involves only one 16-bit word. To read the entire PSA for one port, the CPS must do 16 accesses in 16 successive memory cycles. The following is a brief description of the data each PSA word contains:

1. Word 0 - contains the fast control and sense supervisory bits.

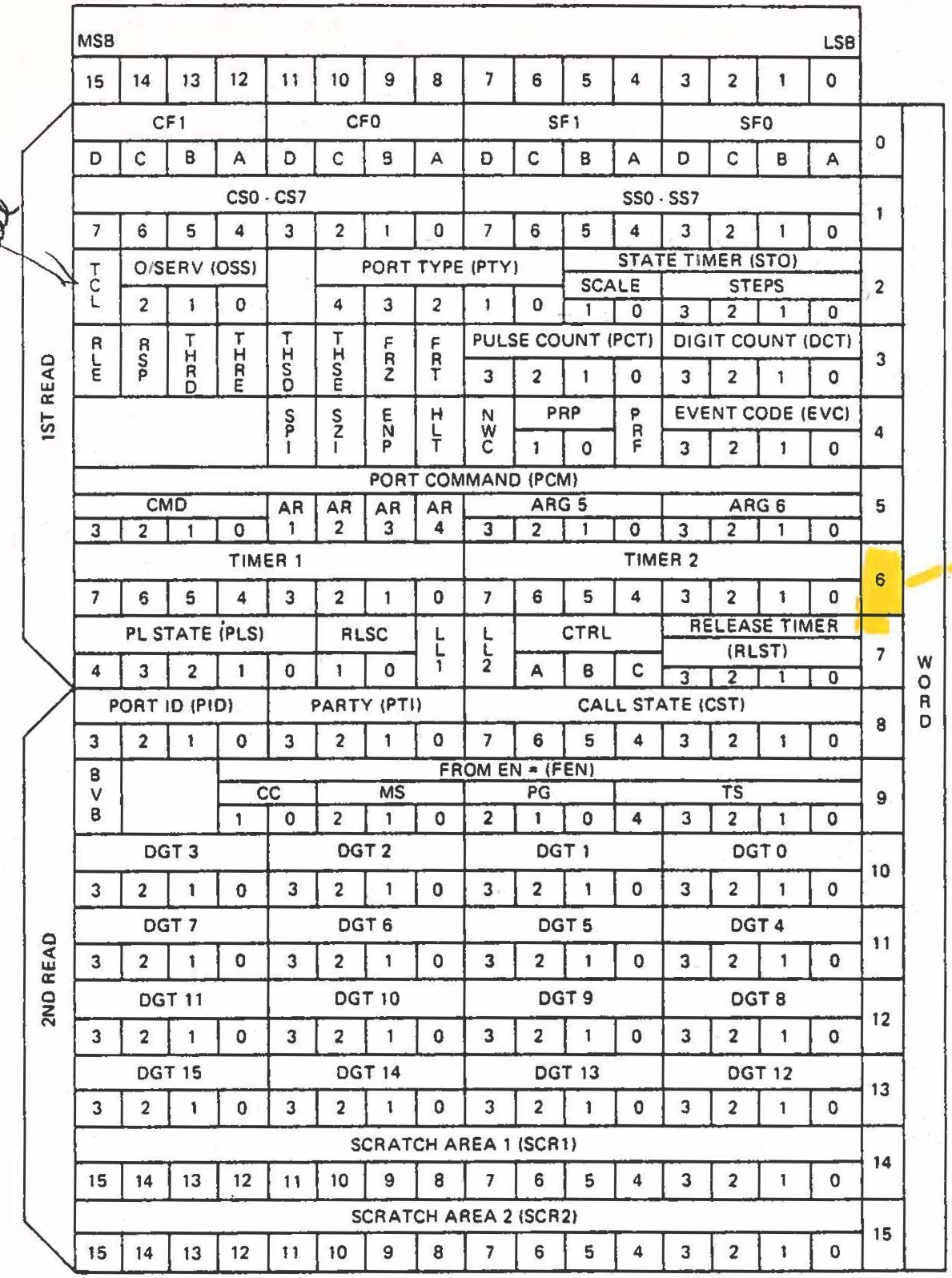
2. Word 1 - contains the slow control and sense supervisory bits.

3. Word 2 - contains the state-timer field, the port-type field, the out-of-service field, and the test call (TCL) bit.

a) The state-timer field specifies the elapsed time before the processor is notified when an event is not detected. The scale bits indicate the time required for the timer to step from 0 through 15 (as indicated in binary). Scale 00 = 256 milliseconds, 01 = 2.048 seconds, 10 = 16.38 seconds, 11 = 131.075 seconds.

b) The port-type field identifies the type of port as follows:

0000 Not equipped



	MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1ST READ	CF1				CF0				SF1				SF0				0
	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A	
	CS0 - CS7								SS0 - SS7								1
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
	TCL	O/SERV (OSS)				PORT TYPE (PTY)					STATE TIMER (STO)						2
		2	1	0		4	3	2	1	0	SCALE		STEPS				
											1	0	3	2	1	0	
	RLE	RSP	THRD	THRE	THSD	THSE	FRZ	FRT	PULSE COUNT (PCT)				DIGIT COUNT (DCT)				3
									3	2	1	0	3	2	1	0	
					SPI	SZI	ENP	HLT	NWC	PRP		PRF	EVENT CODE (EVC)				4
										1	0		3	2	1	0	
	PORT COMMAND (PCM)																5
	CMD				AR 1	AR 2	AR 3	AR 4	ARG 5				ARG 6				
	3	2	1	0					3	2	1	0	3	2	1	0	
	TIMER 1								TIMER 2								6
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
	PL STATE (PLS)				RLSC			LL1	LL2	CTRL			RELEASE TIMER				7
	4	3	2	1	0	1	0			A	B	C	(RLST)				
													3	2	1	0	
	PORT ID (PID)				PARTY (PTI)				CALL STATE (CST)								8
	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0	
2ND READ	BVB		FROM EN = (FEN)														9
			CC		MS			PG			TS						
			1	0	2	1	0	2	1	0	4	3	2	1	0		
	DGT 3				DGT 2				DGT 1				DGT 0				10
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
	DGT 7				DGT 6				DGT 5				DGT 4				11
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
	DGT 11				DGT 10				DGT 9				DGT 8				12
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
	DGT 15				DGT 14				DGT 13				DGT 12				13
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
	SCRATCH AREA 1 (SCR1)																14
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	SCRATCH AREA 2 (SCR2)																15
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

WORD

CP 7552

Figure 3. Port Store Area Bit Layout

00001	Standard line, ground start or prepay pay-station
00010	DTI foreign exchange line
00100	Toll MF sender
00101	DTMF sender
00110	Toll MF detector
00111	DTMF detector
00100	Loop trunk
01001	E&M trunk
01010	Step-by-step incoming trunk
01100	Port group control port
01111	Conference
10000	Line
11000	Step-by-step outgoing trunk
11001	Digital trunk interface (DTI) port
11111	DTI controller

c) The out-of-service (OS) field specifies the OS status of the port as follows:

000	Spare
001	Normal (in service)
010	Manual OS request
011	Manual OS active
100	Automatic OS request
101	Automatic OS active
110	Spare
111	Spare

d) The test call bit is processor controlled and indicates that a test call is in progress for the port.

4. Word 3 - contains the digit-count field, the pulse-count field, the freeze-control area, the through-signaling area, and the release-timing bits.

a) The digit-count field indicates the current number of digits in the digit storage area and is used as an index for fetching and storing the next digit.

b) The pulse-count field indicates the current number of on-hook pulse intervals for the digit being sent or received.

c) Freeze-control inhibits all changes to the PSA, except random access by the call processor. The freeze (FRZ) bit is call processor-controlled. While it is set, all write operations into the PSA (except

from the call processor) are inhibited. The freeze timeout (FRZ) bit is set by the call processor when a freeze is commanded. The first inhibited timeslot to the PSA resets the bit; the second timeslot (4 milliseconds later) causes timeout and a signal to be sent to the maintenance processor, permits resumption of PL operations, and resets the FRZ bit.

d) The through-signaling area contains the following four bits:

1. The through-signaling send data (THSD) bit contains data to be sent over the through-signaling system at the next timeslot.

2. The through-signaling send enable (THSE) bit, when set, causes updating of THSD by supervisory-in signals every 4 milliseconds.

3. The through-signaling receive data (THRD) bit contains the last data received from the through-signaling system.

4. The through-signaling receive enable (THRE) bit, when set, causes updating of supervisory-out data by THRD every 4 milliseconds.

e) The release-timing bits provide for release-timing specification either by a port control command instruction or concurrent with other port control commands. The release-timing enable (RLE) bit, when set, indicates that release timing is initiated when

the supervisory-in field changes to on-hook after an off-hook (seizure/ answer) condition is detected. The release-timing speed-selector (RSP) bit indicates release timing of 20 milliseconds when it is 1 and 208 milliseconds when it is 0.

5. Word 4 - contains the response area (event-code field, processor request flag, and processor request priority bits); part of the command area (new command and halt bits); and part of the supervision-control area (supervisory-in and seizure-in bits).

a) The event-code field is set by the PL because of a port command or by way of an action independent of a command (state timeout, release, etc.) in response to events requiring processor action. The event codes are:

0000	No events detected
0001	Release
0010	State timer timeout
0011	Halt
0100-1111	Port command dependent events

b) The processor request flag (PRF) bit is set when the PSA contains an event code and the equipment number has been placed in queue. This bit starts the PRF watchdog timer.

c) The processor request priority (PRP) bits specify the queue to be used when an event is detected at the associated port as follows:

00	Priority 0
01	Priority 1
10	Priority 2
11	Spare

d) The new command (NWC) bit, when set, indicates that a new command is in the command field (word 5). The bit causes all command sequences, timers, etc., to be initialized and is then reset by the PL.

e) The (HLT) bit is set by software and causes the port command to halt (or finish) in the shortest possible time. After the halt is achieved, the halt code is set in the event-code field.

f) The supervisory-in (SPI) bit indicates the current incoming supervisory state and is under control of the PL.

g) The seizure-in (SZI) bit indicates the recognized state of incoming supervision at the port. The bit is set by the PL when the port command demands the recognition of seizure. Seizure, in this instance, refers to continuous incoming off-hook supervision (seizures, answer supervision, CAMA reversals, etc.).

6. Word 5 - contains the port command field and arguments.

a) The call processor requests PL functions by setting the port command field. The PL reads this field and enters the command logic, which processes the command. Only 0000, 0001, and 1011 are used for LLS. The format of the field is:

0000	No operation
0001	Receive digits
0010	Send digits
0011-0111	Reserved
1000	Receive supervisory event
1001	Send supervisory event
1010	ANI party test
1011	Ring line
1100-1111	Reserved

b) The argument field provides the independent variable upon which the command is to do the desired function.

7. Word 6 and 7 - contain the hardware work area.

a) Each of the two timers step from 0 through 63 in the time period specified by bits 6 and 7 (00 = 4 milliseconds, 01 = 16 milliseconds, 10 = 500 milliseconds). If bits 6 and 7 are both 1's, the scale is disabled and a new scale is defined by arguments 3 and 4.

b) The PL state field indicates the current PL state.

c) The RLSC bits indicate the current state of the release-timing function.

d) The last-look bits (LL1) and LL2) are used in conjunction with the four F0 sense bits to cause momentary interruptions (on-hook, off-hook) to be ignored.

e) The CTRL A and B bits indicate which ringing control (A or B) is on-line.

f) The release timer is set to either 20 milliseconds or 208 milliseconds by the RSP bit when an on-hook is detected. The timer is then decremented to zero and a release event code is generated by the PL.

8. Word 8 - contains call-state information (call-state field, party-identity field, and port-identity field).

a) The call-state field contains a binary code representing the current call state of the port. The call processor accesses this field, when an event is detected by the PL, to determine how the detected event should be processed. The field is updated by the call processor as the port changes call states.

b) The party identity field indicates the identity of a party on a multiparty line. The field can be set either by the PL during an ANI party test on 2- or 4-party lines or by software after receipt of a circle digit. Binary codes 0001 through 1000 identify parties 1 through 8, respectively.

c) The port identity field indicates the ordinal position of the port relative to a call state. For example, in a line-to-line call, the calling line is port 1 and the called line is port 2.

9. Word 9 - contains through-signaling data (from equipment number) and the busy verification bit (BVB).

a) The from-equipment-number field identifies the common control, time-slot interchange, port group, and timeslot involved in the through-signaling data.

b) The BVB is set by the call processor when an operator busy verification call occurs and is reset when the operator releases.

10. Words 10 through 13 - contains the digit storage area for up to 16 digits. The PL retrieves digits from this

area when sending digits to trunks and stores digits here when receiving digits. This area can be used as a scratch area when the PL is not sending or receiving digits.

1. Words 14 and 15 - contain software scratch areas 1 and 2.

4.07 Supervisory Buffer.

The supervisory buffer receives serial sense bits (indicating the status of every port) from the TSI, converts the bits to parallel form, and places them on the port store data bus for transfer to the PCS or PL. Conversely, the supervisory buffer receives parallel control bits (based on decisions made on sense bits received) from the PL, converts the bits to parallel form, and sends them to the TSI. A supervisory buffer serving 2048 ports requires 4 identical PWBAs, 1 for every 2 TSIs. The supervisory buffer is made up of the following circuit elements.

a. Sense-Bit Shift Registers.

These shift registers receive the serial sense bits from the TSI and transfer the bits into RAM buffers 1 and 2 during alternate 40-millisecond cycles.

b. Sense-Bit RAM Buffers.

Sixteen sense bits for each port are serially stored in RAM buffer 1, while 16 others for each port are being read out, in parallel, from RAM buffer 2. The process is reversed during the next 4-millisecond cycle.

c. Sense-Bit Output Data Selectors.

These 2:1 data selectors alternately accept the outputs of RAM buffers 1 and 2 and send the bits to the PCS or PL.

d. Control Bit Latches.

These latches receive 16 parallel control bits for each port from the PL every 12 microseconds and send them to control bit RAM buffers 1 and 2.

e. Control Bit RAM Buffers.

Sixteen control bits for each port are stored, in parallel, in RAM buffer 1 while 16 others for each port are being read out, in parallel, from RAM buffer 2. The process is reversed during the next 4-millisecond cycle.

f. Control Bit 4:1 Data Selectors.

These 4:1 data selectors select RAM buffer outputs, corresponding to one of four 1-millisecond periods of the 4-milli second cycle, to be sent to the output shift registers.

g. Output Shift Registers.

After the control bits for one 1-millisecond period have been simultaneously clocked into the output shift registers, they are serially clocked out to the TSI.

4.08 Buffer Control.

The buffer control generates and supplies the clock and control signals needed by the supervisory buffer to route supervisory bits between the TSI and PCS or PL. Five counters are synchronized to various clock phases and decoded to obtain the required signals. One buffer control PWBA is required for each common control (four supervisory buffer PWBAs). The buffer control is made up of the following major circuit elements:

a. Port Store Address Counter.

This counter counts from 0 through 2047 to generate each PCS timeslot in sequence. The time0 slots are decoded to determine the storage location for supervisory data from other supervisory buffers.

b. Sense-Write Counter.

This counter controls the writing of sense bits from the TSI into the supervisory buffer.

c. Sense-Read Counter.

This counter controls the readout of sense bits from the supervisory buffer to the PCS or PL.

d. Control-Write Counter.

This counter controls the writing of control bits from the PL into the supervisory buffer.

e. Control-Read Counter.

This counter controls the readout of control bits from the supervisory buffer to the TSI.

4.09 Through-Signaling.

Through-signaling circuits on the buffer control PWBA permit certain functions (hookswitch flash, through-dialing, etc.), normally vailable in metallic-path systems, to be provided in the SYSTEM CENTURY digital system. This is done by controlling a bit in memory at one port in response to the detection of certain conditions at another port. Through-signaling is needed between equipment frames when more than one common control frame is used because the calling and called ports could be served by different common controls. The through-signaling circuit is made up of the following major circuit elements.

a. Line Drivers.

A through-signaling bit from the PCS associated with a buffer control is clocked into the buffer register and then sent, by line drivers, to all other common controls.

b. Line Receivers.

One bit from each common control is routed to a line receiver input. The line receiver outputs become RAM inputs.

c. RAMs.

The through-signaling bit is stored at a RAM address selected by the address selectors.

d. Address Selectors.

The RAM address normally comes from the buffer control. However, after the RAM output is read, the address selectors select an address from the PCS.

4.10 Common Program Logic.

The common PL uses Pl state and command information from the PCS to generate event codes for the port circuits. These event codes are then stored in the port store areas of the PCS for the ports requiring attention from the CPS. From these event codes, the CPS determines the type of action required. One common PL PWBA is required for each common control. The common PL is made up of the following major circuit elements:

a. Data Registers.

Information from the PCS is strobbed into the PL state register, command register, and port service status register. This information is then decoded and applied to the event-code-generation logic and to the write-PL-state control logic.

b. Event-Code-Generation Logic.

This logic produces event recognition signals that are applied to a 16:4 encoder that generates the 4-bit event code.

c. Write-PL-State-Control Logic.

This logic generates the next PL state, based on information in the PL state and command registers.

d. State-Timeout Registers.

Two registers provide the state-timeout function. When the register outputs decrement to 0, the event-code-generation logic generates an event code.

e. Release-Timing Circuitry.

This circuitry monitors various bits in the PCS and steps the PL through the appropriate PL states until release occurs.

4.11 Receive-Supervisory-Event/ Send-Supervisory Event Program Logic.

The receive-supervisory-event/send-supervisory-event (RSE/SSE) PL receives and sends supervisory signals for the trunks from and to the PCS. The circuit also contains two timers that are used by

this and other PL circuits. One RSE/SSE PL PWBA is required for each common control. The RSE/SSE PL is made up of the following major circuit elements:

a. Receive-Supervision-Detection Logic.

This logic sorts out incoming supervision and classifies it as:

1. Seizure/release.
2. Wink/hookflash.
3. Stop dial.
4. Delay dial.

b. Send-Supervision-Generation Logic.

This logic generates the following outgoing supervisory signals for trunks:

1. Wink.
2. Hookflash.
3. Wink-off.
4. Delay dial.

c. PL Common Timer.

The timer circuitry provides timing and control signals used by other PL circuits to advance PL states, set PCS registers, etc.

4.12 Receive-Digits Program Logic.

The receive-digits PL converts received dial-pulse (DP), dual-tone multifrequency (DTMF), or toll MF signals to a 4-bit binary code representing the digit received. The digits are stored in the port store area of the PCS for the associated port. One receive-digits PL PWBA is required for each common control. The receive-digits PL is made up of the following functional elements:

a. Port-type steering logic.

b. Receive-digits start logic.

c. Digits-expected check logic.

d. Dial-pulse detection logic.

e. Tone-detector decoding logic.

f. Interdigital- and critical-timeout check logic.

4.13 Send-Digits Program Logic (Trunks Only).

The send-digits PL causes the digits in the digit storage area of the PCS to be outpulsed, either as dial pulses or as toll MF tones. Presending and postsending supervision is provided by the send-digits PL, under software control, in conjunction with the RSE/SSE PL. One send-digits PL PWBA is required for each common control.

4.14 Receive-Digits/Send-Digits Program Logic.

The receive-digits/send-digits (RD/SD) PL decodes DTMF and toll MF codes into a 4-bit binary format. The circuit also converts from 4-bit binary to two-of-six code (2/6) for toll MF sending. One RD/SD PL PWBA is required for each common control. The RD/SD PL is made up of the following circuit elements:

a. Digit Storage Register.

This register temporarily stores the contents of the digit storage area of the PCS for the port being processed.

b. Digit Count (DCT) Register.

During the receive-digits process, this register indicates the position in the digit storage area of the PCS where the next digit is to be stored. During the send-digits process, this register allows the bits representing each digit to be transferred from the digit storage register to the pulse counter in the PCS at the proper time.

c. Pulse Counter Register.

The pulse counter (PCT) register inputs from the PCT in the PCS. During the receive-digits process, the PCT and PCT register are incremented by received dial

pulses; the output is stored in the digit storage area specified by the DCT register. During the send-digits process, the PCT register is decremented to out-pulse the digit values stored there for dial-pulse sending, or the contents are converted to 2/6 code for toll MF sending.

4.15 Ring-Line Program Logic.

The ring-line PL causes ringing to be applied to a line, when required. Ringing is provided for normal, emergency rering, and revertive calls. One ring-line PL PWBA is required for each common control. The ring-line is made up of the following major circuit elements:

a. Ring-Phase Generation Logic.

Four ring phases are generated by this circuitry and sent to the ringing interrupters. The ring phases are also used by the ring-phase selection logic on this circuit.

b. Ring-Phase Selection Logic.

The ring-phase selection logic determines the following each time that ringing is applied:

1. Phase on which ringing occurs.

2. Whether ringing is applied to tip or ring side of line.

3. Whether ringing is by way of the main or alternate ringing bus. (Alternate bus is required for revertive calling when both parties have the same ringing frequency but on opposite sides of the line.)

c. Ringing Control Logic.

The ringing control logic enables the proper control bits for the designated ringing bus and path.

5. FUNCTIONAL OPERATION OF COMMON CONTROL

5.01 General.

The following paragraphs describe, without detailed reference to circuit operation, how a typical call is handled by the common control of the SYSTEM CENTURY DCO. Block diagrams are used to show the sequence of connections made. Circuits indicated by broken lines are not part of the common control.

5.02 Dial-Tone Connection.

a. Off-Hook Detection.

A request for dial tone begins when a station user lifts the handset of the telephone (fig. 4). This closes a loop across the tip and ring of the line to signal the line circuit assigned to the station (connection 1). The line circuit sends an off-hook supervisory sense bit to the line group controller (connection 2), which continuously monitors the 90 line circuits under its control. The line group controller sends an off-hook message to the LSC (connection 3) and the line group multiplexer/demultiplexer (connection 4). The LSC marks the line busy and searches for an idle timeslot on the line group highway and port group highway. When a timeslot is found, the LSC sends an LGM assignment command to the line group controller (connection 5) to identify the line circuit that is to be switched to the selected timeslot. The port group highway and timeslot (same number as line group highway timeslot) are also identified. The LSC also marks the timeslot busy and checks the line circuit type to determine if a party test is required. If a test is required, the LSC commands the line group controller and the line group acces to make the test; the results are returned to the LSC. The LSC now sends an origination message to the CBFC (connection 6) and commands the LGM to send the off-

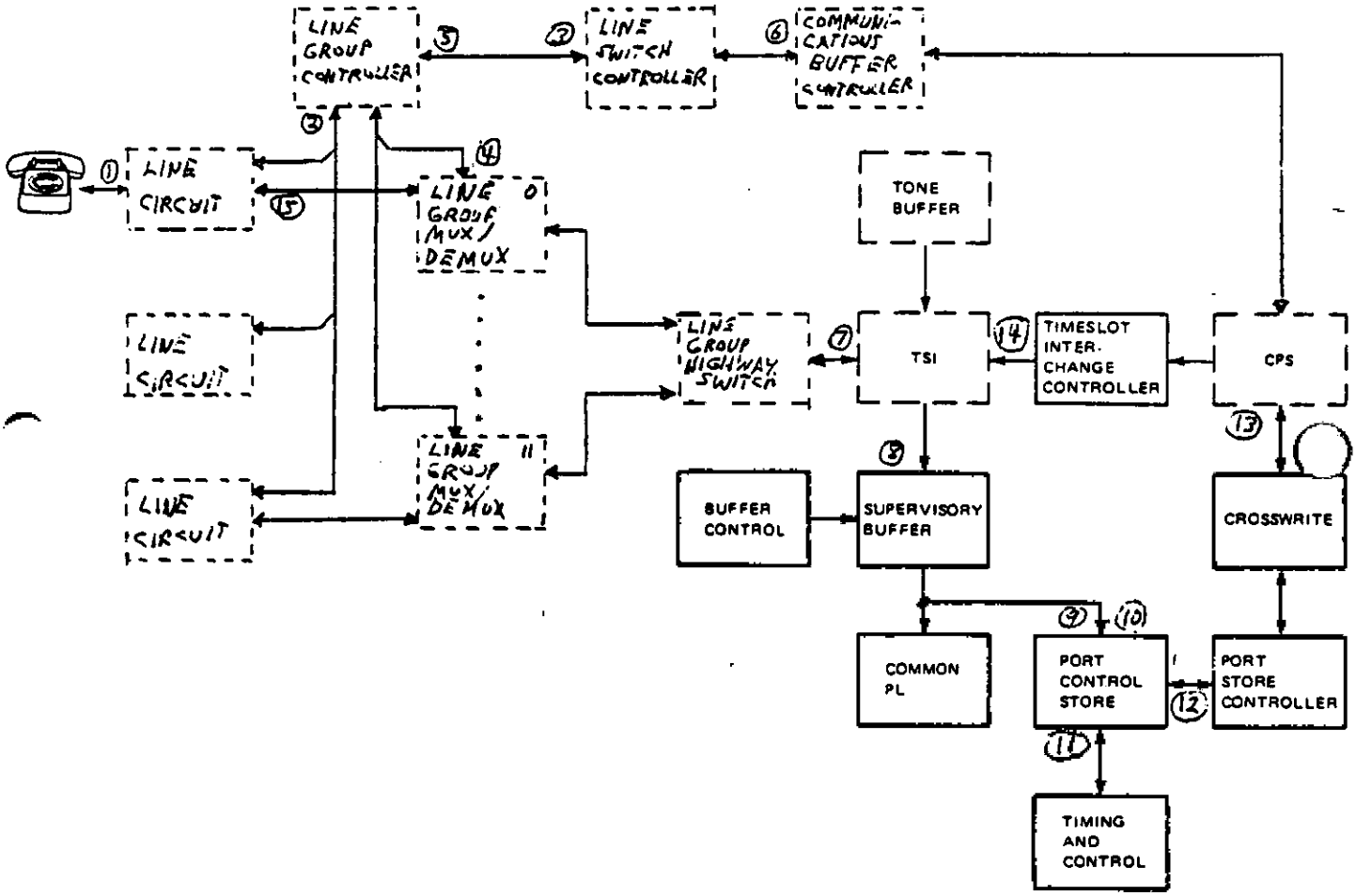


Figure 5. Dial-Tone Connection ~~(LLB)~~
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hook supervisory bit to the TSI, by way of the line group highway switch (connection 7). Each CPS continuously scans the status registers of the associated CBCs. When the CPS detects the origination message, it uses a cross reference table to determine the PSA associated with the port group highway timeslot being used. The off-hook supervisory bit, previously sent to the TSI, is detected by the supervisory buffer (connection 8) and transferred to the PSA being used for the call (connection 9). Once every 4 milliseconds, each PSA is strobed and the information is read out to the PL. When off-hook is detected, a seizure event code is stored in the PSA (connection 10). The timing and control stores the address of the PSA in the appropriate queue (connection 11). On the next periodic scan of queue states, the CPS recognizes that a queue has an entry in it. The CPS accesses the queue to determine which PSA has an event code. The CPS then reads the PSA (by way of the crosswrite and port store controller circuits) for the line (connection 12) and detects the seizure event code (connection 13). The CPS also stores in the PSA the next call state and command (receive-digits) and resets the various counter storage areas (pulse counter, digit counter etc.) for the line.

b. Dial-Tone Application.

The CPS sends a dial-tone command to the TSI, by way of the TSI controller, to connect dial tone (broadcast tone) to the line (connection 14). The pulse-code modulated dial tone is then converted to an analog signal by a decoder in the line circuit (connection 15) and heard by the calling party.

5.03 Dialing.

When the receive-digits PL (fig. 5) receives the receive-digits command stored in the PSA by the

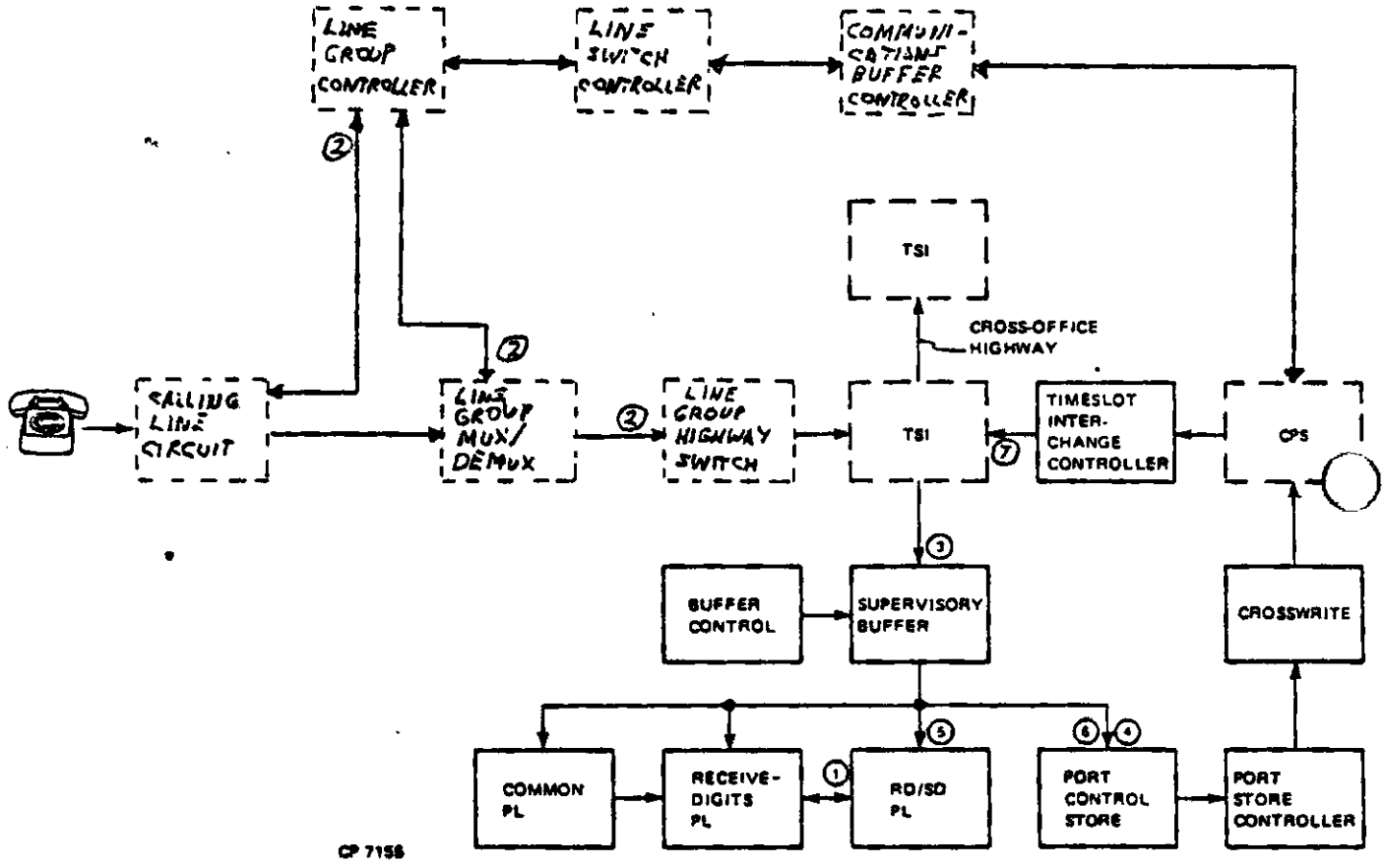

Figure 5. Dialing ~~(LLC)~~

CPS, it enables the receive-digits start circuitry in the receive-digits and receive-digits/send-digits (RD/SD) PL (connection 1). When the calling party starts to dial, the line circuit forwards the dial pulses to the TSI (connection 2). The dial-pulse bits are detected by the supervisory buffer (connection 3) and forwarded to the PSA (connection 4). The bits are then read out to the RD/SD PL (connection 5) where they increment the pulse counter 1 register. When the interdigital timing circuits in the receive-digits PL detect the end of a digit, the 4-bit output of the pulse counter/register in the RD/SD PL is transferred to the digit storage area of the PSA (connection 6). At the completion of dialing, the inter-office equipment number is translated, and the CPS instructs the TSI (connection 7) to set up a calling-to-called-line transmission path. The path is set up by assigning a cross-office highway timeslot (from calling-to-called TSI) for the calling line.

5.04 Ringing/Ringback Tone.

a. The CPS (fig. 6) sends a termination command to the LLS (connection 1). The LSC checks the status of the called line; if it is free, the LSC does a line group highway/port group highway path search. If an idle path is found, the LSC marks it busy, sets up the line group highway switch, and sends an LGM assignment command to the line group controller (connection 2). The line group controller responds with a mux path assigned message when the timeslot data has been written into the LGM. The LSC now sends a connect message to the CPS (via the CBC) to identify the port group highway and timeslot to be used (connection 3).

b. The CPS responds by selecting a tone buffer associated with the same TSI as the called line. To ensure that a conversation path is available when the called

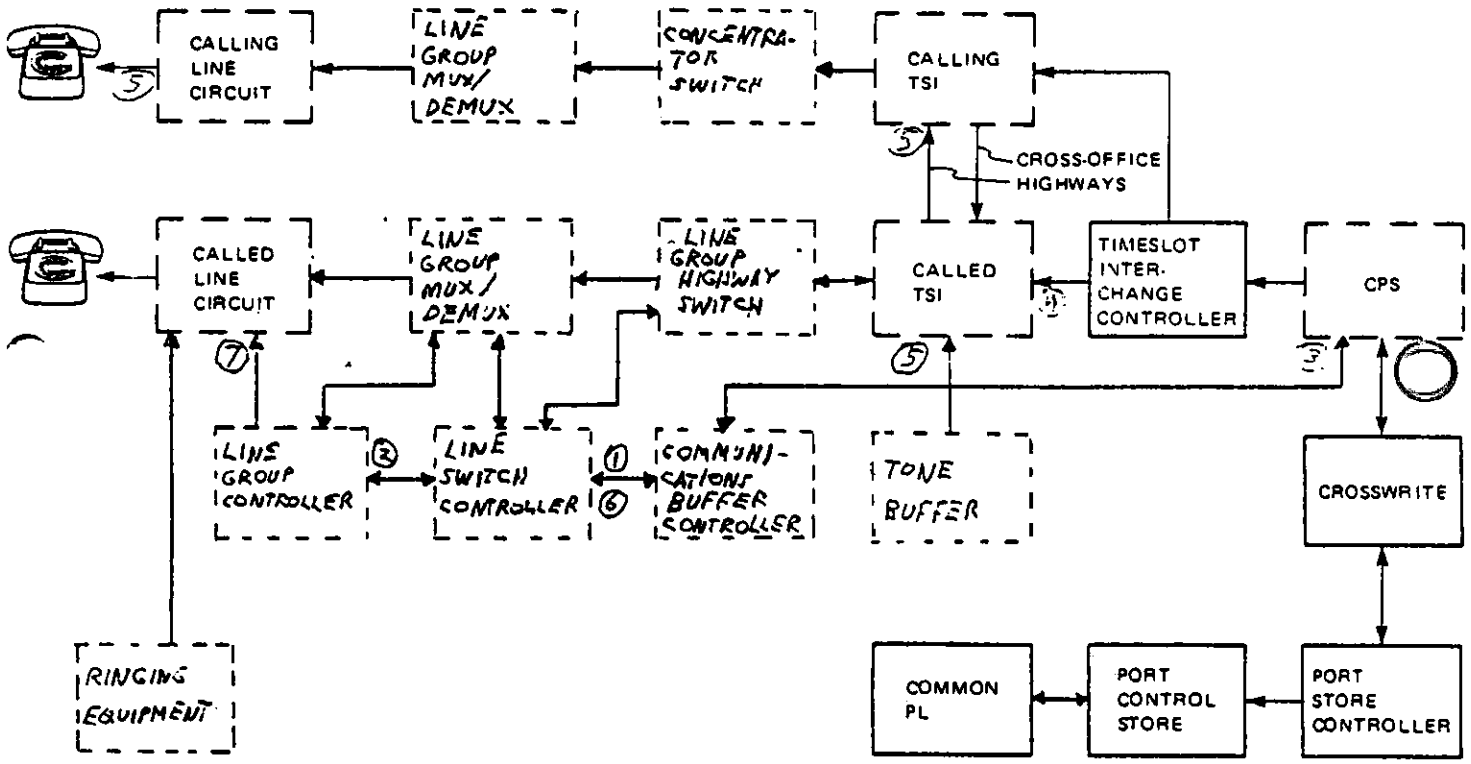

Figure 6. Ringing and Ringback Tone Application (~~LLC~~)

party answers, the ringback tone source and called port are assigned to the same cross-office highway timeslot in the called TSI (connection 4). (All transmission between TSIs is over cross-office highways on a first-come, first-served basis.)

c. The CPS causes ringback tone to be sent to the calling line (connection 5), gets the ring code information for the called LLS line, and sends a ring-line command to the LSC (via the CBC) (connection 6). The LSC converts the ring-line command to a line group controller ring command, causing the line group controller to operate the ring relay on the called line circuit (connection 7).

5.05 Answer.

Ring trip (fig. 7) is detected by the line group controller, which sends a ring-trip message to the LSC (connection 1). The LSC commands the LGM to send the ring trip sense bit to the TSI, by way of the line group highway switch (connection 2). The supervisory buffer detects the ring trip sense bit (connection 3) and stores a ring-trip event code in the PSA (connection 4). When the CPS reads the PSA, it detects and verifies the ring-trip event code (connection 5). The cross-office highway timeslot used for ringback tone to the calling line is assigned to the called line by the CPS (connection 6) to permit called-to-calling-line conversation. The CPS changes the call state of the calling and called lines to "talking line-to-line" in the associated PSAs (connection 7).

5.06 Release.

a. Referring to figure 8, assume the calling party goes on-hook (connection 1). An on-hook supervisory bit is sent to the PSA (connection 2) and an on-hook message is sent to the CPS (connection 3), as descrfbed in paragraph

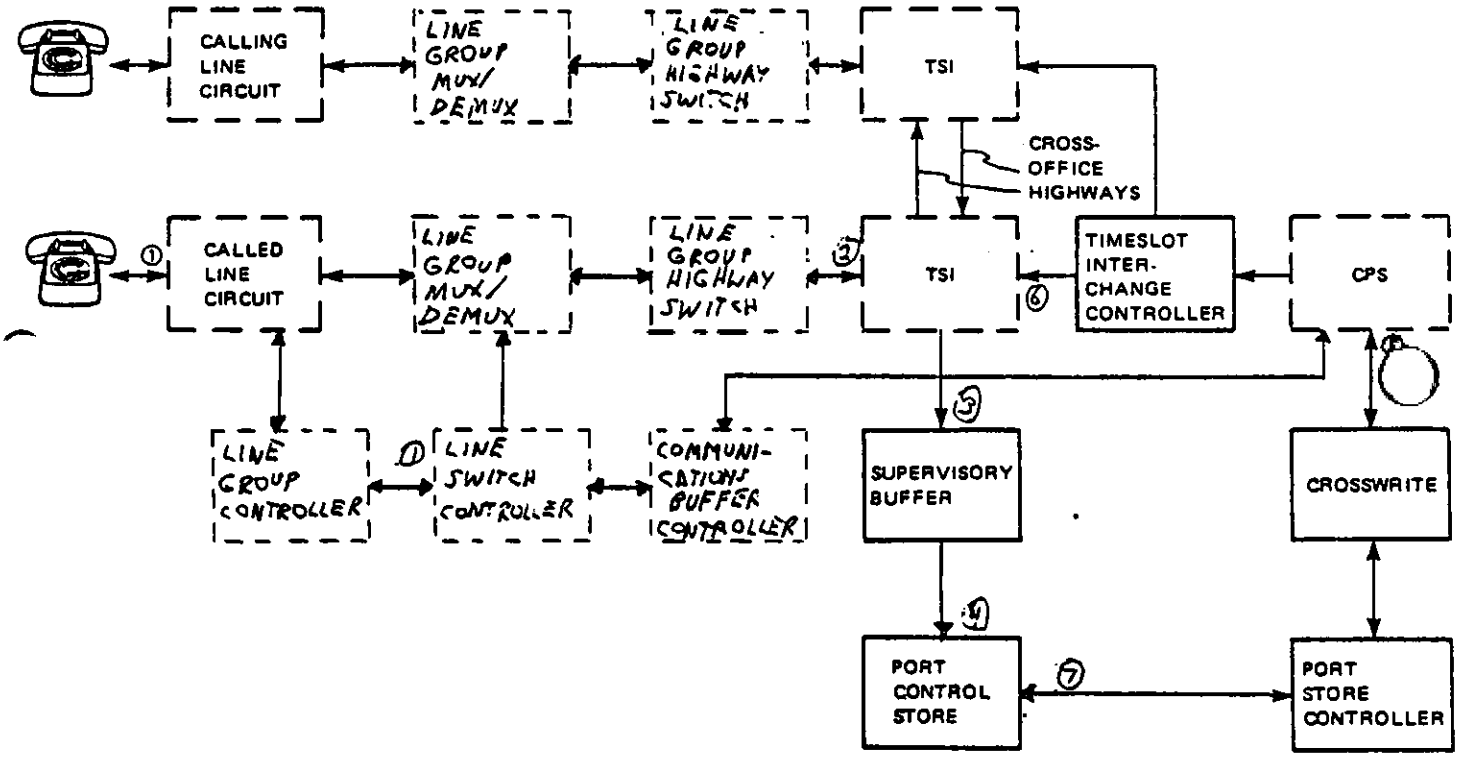

Figure ~~11~~. Answer ~~(LLC)~~

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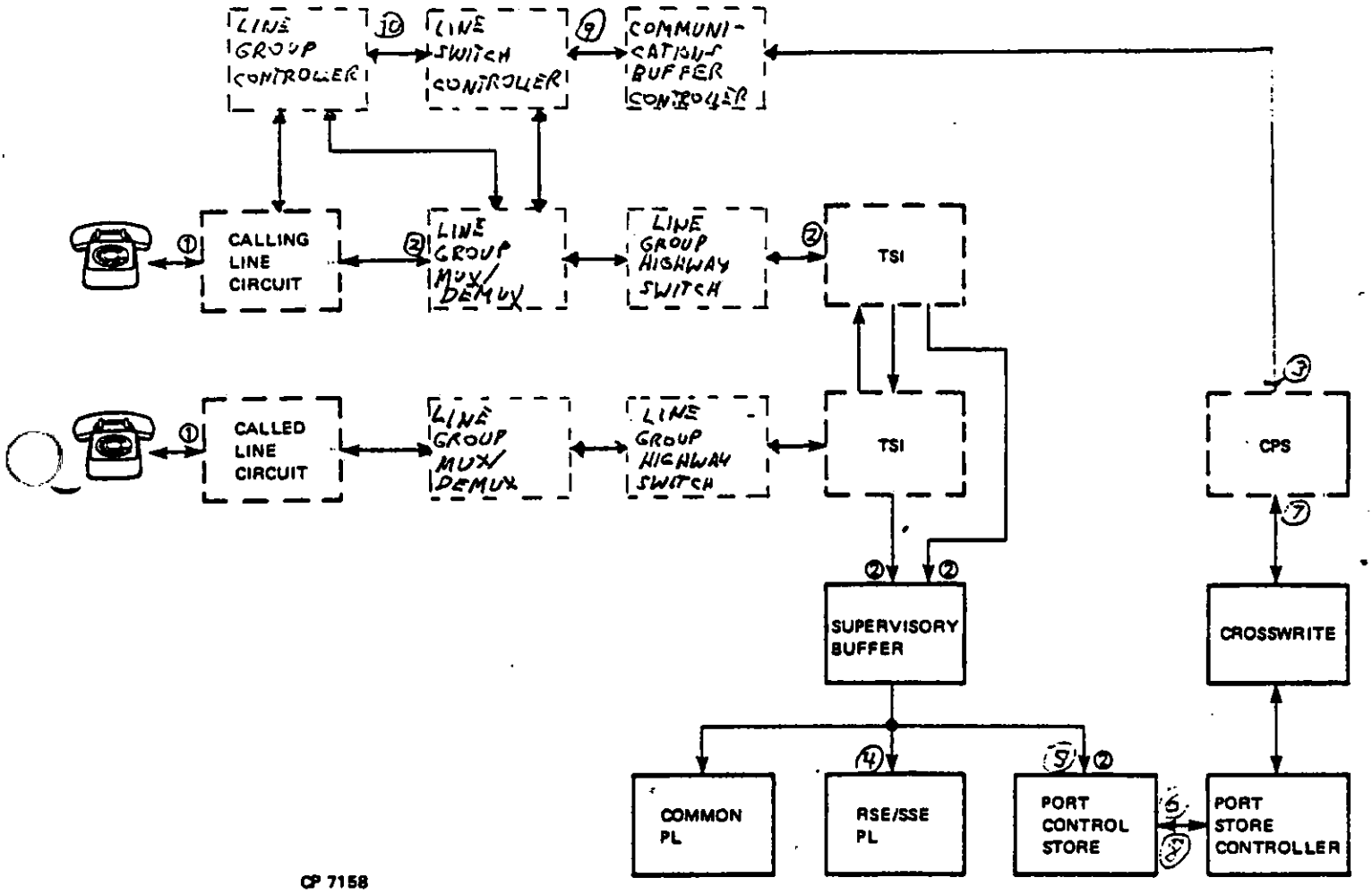

Figure ~~13~~ 8. Release ~~(LLS)~~

5.02. The RSE/SSE PL detects the on-hook bit (connection 4) and sends a release event code back to the PSA (connection 5). When the CPS reads the PSA for the on-hook line (connection 6), it detects and verifies the release event code (connection 7). The CPS sets the call state for the on-hook line to "idle" and the call state for the other line to "release timeout" in the respective PSAs (connection 8). The CPS then sends a disconnect command to the LSC (connection 9). The LSC releases the line group highway switch path and sends an LGM release command to the line group controller (connection 10) to identify the timeslot that is to be released. The LSC also sets the line call state to idle.

b. If the called party goes on-hook before timeout occurs, the release sequence is the same as that just described. If timeout occurs (16.3 seconds), the common PL generates the release event code and sends it to the PSA. The CPS then detects the release event code and release continues as described in paragraph a above.