

**SYSTEM CENTURY®
DIGITAL CENTRAL OFFICE**

**SERVICE GROUP CIRCUITS
DESCRIPTION**

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19.	Toll Multifrequency Detector Interface	20	1.	INTRODUCTION	
20.	Toll Multifrequency Detector Output	22	1.01	This section provides functional descriptions of the circuits that make up the service group of the SYSTEM CENTURY® Digital Central Office (DCO). The service group includes ringing equipment, tone generators, multifrequency senders, and clock circuits.	
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1.02 This section is reissued to provide information on the local line switch (LLS), toll multifrequency sender, and multifrequency signal detector interface. Significant changes and additions are indicated by bars in the margin.

2. RELATED INFORMATION

2.01 A Sales and Instructional Literature Index of latest available publications can be obtained from your Stromberg-Carlson sales representative or from Publications Services, Stromberg-Carlson Corporation, 400 Rinehart Road, Lake Mary, Florida 32746.

3. GENERAL

3.01 The service group comprises the circuits required to generate and distribute ringing voltage, tones, and timing (clock) signals. To ensure uninterrupted service, the most vital circuits in this group are provided in duplicate. These redundant circuits include the ringing generators, precise tone generators, toll multifrequency tone generators, tone buffers, master clocks, and synchronous network clocks.

4. PROGRAMABLE RINGING SYSTEM

4.01 General.

Each ringing generator used in newer offices can be programed to 1 of 15 ringing frequencies and 1 of 5 ringing voltages by setting dual in-line package (DIP) switches inside the generator. The system can have either one generator for each frequency and a standby generator that automatically takes over when an on-line generator fails (par. 4.02) or redundant generators for each frequency (par. 4.03).

4.02 Single Backup Generator Configuration.

A typical system contains up to five local programable generators and one remote programable generator. If a local programable generator fails, the remote programable generator is automatically programed to the frequency and voltage of the failed unit and put on-line. Besides the generators, this configuration contains a programable transfer module (par. 4.04), frequency meter panel (par. 4.05), redundant ringing multiplexer and serializer circuits (par. 4.06), and a ring status interface circuit (par. 4.07). See figure 1.

4.03 Redundant Generator Configuration.

When redundant programable generators are used, one set of generators is used as the main supply and the other set as the standby supply. If the output

voltage of any generator in the main set drops below a predetermined level, the load is automatically transferred to the standby set. Besides the generators, this configuration contains a frequency meter panel (par. 4.05), redundant ringing multiplexer and serializer circuits (par. 4.06), and a ring status interface circuit (par. 4.07). See figure 2.

4.04 Programable Transfer Module.

This automatic unit is used in the single backup generator configuration. The programable transfer module detects the failure of any ringing generator, programs the standby generator to the ringing frequency and voltage of the failed generator, starts the standby generator, and connects it to the load. The programable transfer module contains one set of DIP switches for each local ringing generator. Each set of switches is programed the same as the switches on the corresponding ringing generator at the time of installation. When a ringing generator fails, its associated DIP switches on the transfer module send a control word to the standby generator to program the correct ringing frequency and voltage.

4.05 Frequency Meter Panel.

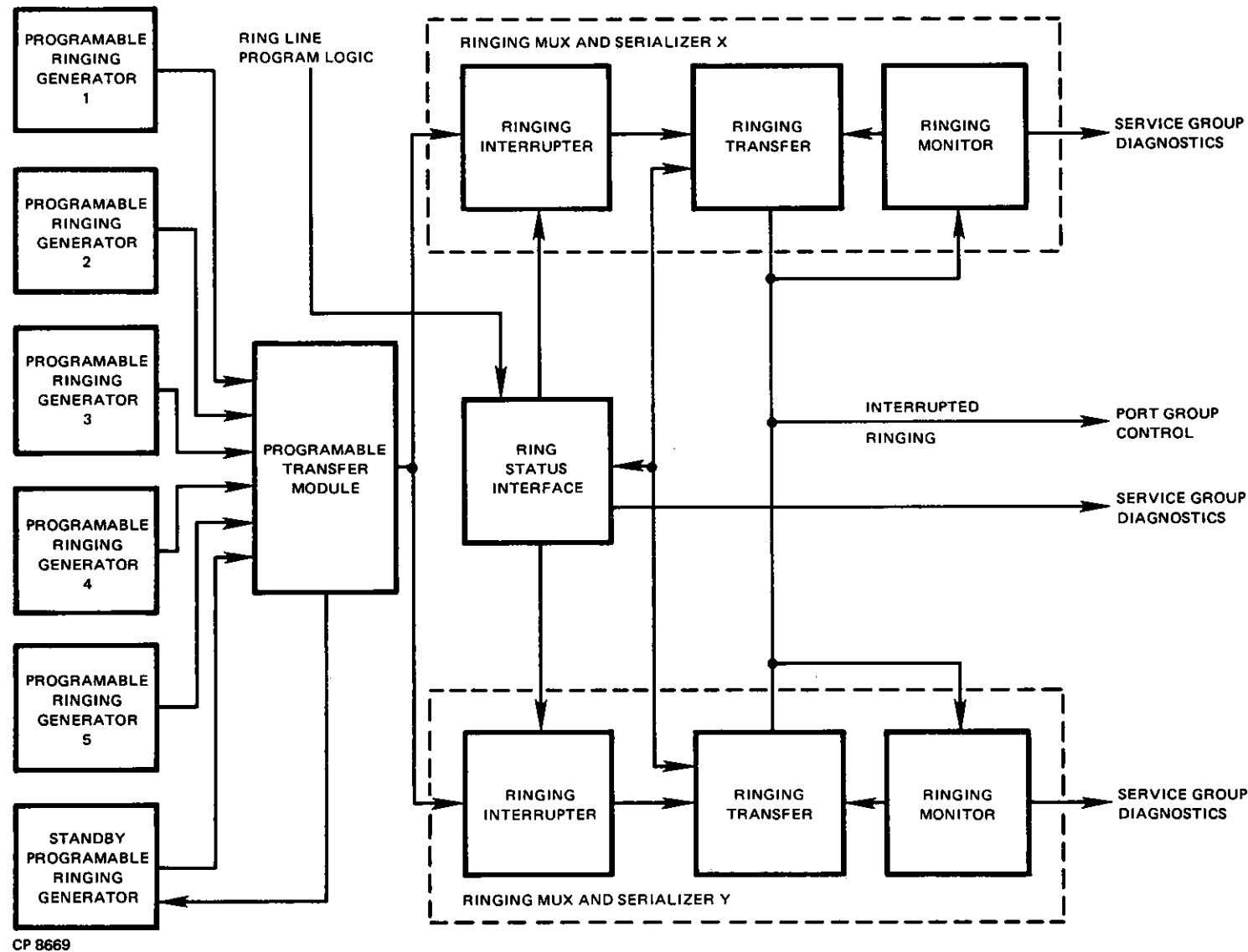
The frequency meter panel contains a digital meter to permit checking of the frequency or voltage of any generator. The generator output displayed is selected by a rotary switch on the panel.

4.06 Ringing Multiplexer and Serializer.

a. The ringing multiplexer and serializer provides cadence for single-frequency ringing and phasing for four-frequency ringing. The circuit also detects ringing generator failures and sends appropriate alarms to the service group diagnostics circuit.

b. Redundant ringing multiplexer and serializer circuits are used in both the single backup generator configuration and the redundant generator configuration.

c. The ringing interrupter portion of the ringing multiplexer and serializer circuit receives continuous ringing voltage from each associated ringing generator. The single-frequency interrupters produce output cadences consisting of two 1.23-second periods of ringing, alternating with two 1.77-second periods of silence, in each 6-second cycle. The four-frequency interrupters each produce four ringing signals with



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Figure 1. Single-Backup Programmable Ringing Generator Configuration, Block Diagram

the same cadence but shifted in phase with respect to each other. Each four-frequency output consists of four 1.23-second periods of ringing, alternating with four 0.27-second periods of silence, in each 6-second cycle. Each period of ringing during a cycle is at a different frequency.

d. The interrupter transfer portion of the ringing multiplexer and serializer selects the outputs of one interrupter (under control of the ring status interface) and sends them to the port group control. A ringing monitor tests the outputs to detect faults in the interrupted ringing signals.

4.07 Ring Status Interface.

This circuit causes the interrupter transfer portion of the ringing multiplexer and serializer to select the outputs of either interrupter X or interrupter Y. This PWBA also forwards status and alarm signals to the service group diagnostics circuit.

5. NONPROGRAMMABLE RINGING SYSTEM

5.01 Ringing Machines (Generators).

The ringing generators used in older offices provide all required ringing frequencies. Redundant ringing machines are used for reliability. One machine is used as the main supply and the other as the standby supply. If the output voltage of the main ringing machine drops below a predetermined level, the load is automatically transferred to the standby machine. The transfer is done by the ringing interrupter transfer control circuit.

5.02 Frequency Meter Panel.

The frequency meter panel contains an ac voltmeter and a frequency meter to permit checking of the four frequencies from ringing generators X and Y. The generator (X or Y) and frequency are selected by a rotary switch on the panel.

5.03 Ringing Monitor and Serializer.

a. The ringing monitor and serializer provides cadence for single-frequency ringing and phasing for four-frequency ringing. The circuit also detects ringing generator failures and sends appropriate alarms to the service group diagnostics circuit.

b. The ringing monitor and serializer circuit is composed of three types of printed wiring board assemblies (PWBAs): two redundant ringing interrup-

ter PWBAs (814057-046) and two ringing interrupter transfer and monitor PWBAs (814057-066) are located in power frame 1, and a ringing interrupter transfer control PWBA (814057-026) is located in the maintenance and administration frame. The interrelation of these PWBAs is shown in figure 3.

c. Either ringing generator X or ringing generator Y applies continuous ringing voltage superimposed on -48 volts to its associated ringing interrupter. The single-frequency interrupters, in turn, produce output cadences consisting of two 1.28-second periods of ringing, alternating with two 1.79-second periods of silence, in each 6.144-second cycle. The four-frequency interrupters each produce four ringing signals with the same cadence, but shifted in phase with respect to each other. Each four-frequency output consists of four 1.28-second periods of ringing alternating with four 0.25-second periods of silence in each 6.144-second cycle. Each period of ringing during a cycle is at a different frequency.

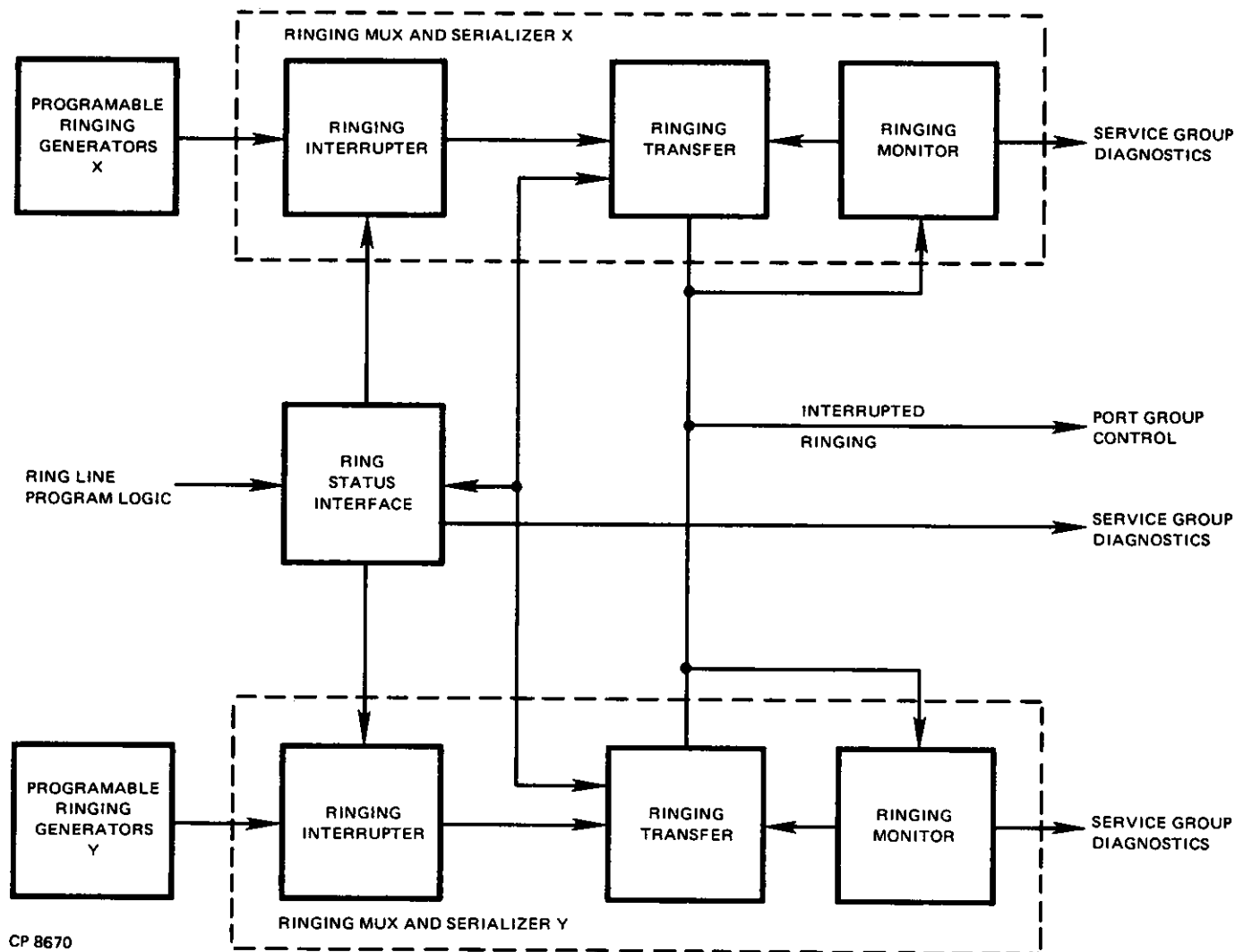
d. The interrupter transfer PWBA selects the outputs of one interrupter (under control of the transfer control circuit) and sends them to the port group control. A ringing monitor on the interrupter transfer PWBA tests the outputs to detect faults in the interrupted ringing signals.

e. The interrupter transfer control PWBA causes the interrupter transfer PWBAs to select the outputs of either interrupter X or interrupter Y. This PWBA also forwards status and alarm signals to the service group diagnostics circuit.

6. RECEIVER OFF-HOOK TONE GENERATOR

6.01 The receiver off-hook (ROH) tone generator used in older systems, in power frame 1, produces a distinctive tone signal, designed to get the attention of a subscriber who has left a receiver off-hook. The tone generator is a precise tone system in that it does not generate harmonics that could interfere with dual-tone multifrequency signaling. If a low-voltage condition occurs at the generator output, a TONE FAILURE lamp lights on the generator and the service group diagnostics circuit is signaled to indicate that a failure has occurred.

6.02 LLS lines are served by redundant digital ROH tone generators in each LLS frame.



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Figure 2. Redundant Programmable Ringing Generator Configuration, Block Diagram

7. PRECISE TONE GENERATOR

7.01 Redundant, digital precise tone generators in the maintenance and administration frame provide the following functions:

a. Develop precise tone frequencies of 350 Hz, 440 Hz, 480 Hz, 620 Hz, and 1004 Hz for dial tone, high tone, low tone, busy tone, ringback tone, and test tone.

b. Generate intermediate clock rates of 11.2 kHz, 230.4 kHz, 256 kHz, 281.6 kHz, 332.8 kHz, and 435.2 kHz for use by the toll multifrequency (MF) tone generator, plus a 1.024-MHz base frequency.

c. Automatically switch to the standby generator if the on-line generator fails.

7.02 Figure 4 is an orientation diagram showing the relative functional position of the precise tone generator with respect to the other circuits associated with tone generation. Figure 5 is a block diagram of the precise tone generator.

7.03 All frequencies produced by the precise tone generator are digitally derived from the 2.048-MHz system clock. The clock is used to generate a two-phase clock, each phase of which is divided and mixed with a derivative of the other phase. This mixture is further divided to produce a rate which is 16 times the desired output frequency. Those frequencies that are to be used for generating the toll MF tones are sent to the toll MF tone generator. Those used to generate precise tones are applied to program-cycle generators on the precise tone generator PWBA.

7.04 The program-cycle generators produce binary outputs which are then translated by encoding logic into approximate sine-value binary-coded-decimal (BCD) program inputs to pulse-rate modulators. The pulse-rate modulators produce outputs that comprise programmed percentages of the 1.024-MHz base frequency.

7.05 Each precise tone generator/toll MF tone generator pair operates continuously and is either on-line or a standby in case of failure. Failure detection is provided in such a way that a failure (whether on-line or off-line) disables the output of the failed pair, causes a switchover to the good pair (if required), and sends a fault indication to the maintenance processor.

8. TOLL MULTIFREQUENCY TONE GENERATOR

8.01 The toll MF tone generator converts the six digital source signals (11.2 kHz, 230.4 kHz, 256 kHz, 281.6 kHz, 332.8 kHz, and 435.2 kHz) from the precise tone generator into pulse rate modulated square waves of 700 Hz, 900 Hz, 1100 Hz, 1300 Hz, 1500 Hz, and 1700 Hz for use in MF pulsing.

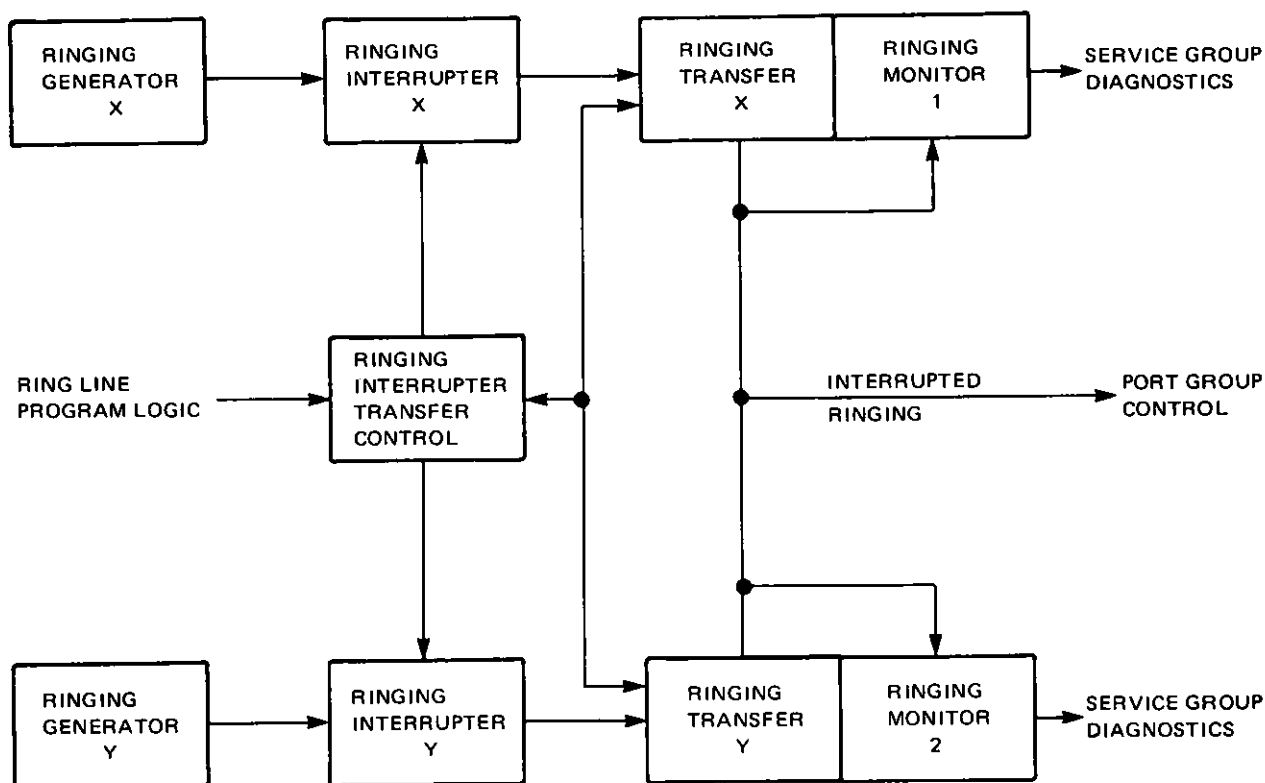
8.02 The six source signals from the precise tone generator are applied as clocks to six program-cycle generators (fig. 6). The program-cycle generators produce binary outputs that are then translated by encoding logic into approximate sine-value BCD program inputs to pulse-rate modulators. The pulse-rate modulators produce outputs that comprise programmed percentages of the 1.024-MHz base frequency from the precise tone generator. These are eventually converted to sine waves by the toll MF sender.

9. TONE BUFFER

9.01 Each redundant tone buffer formats and distributes precise and toll MF tones. The circuit receives digital pulse-rate-modulated (PRM) tones from the toll MF tone generator, buffers the tones, and sends them to the tone plant interface. The tone buffer also receives analog precise tones from the precise tone generator. All of the analog precise tones are converted to pulse-code-modulated (PCM) digital signals by coder/decoder (CODEC) circuits on the tone buffer PWBA. Two of the analog tone inputs are simply amplified and sent to the fire reporting circuit.

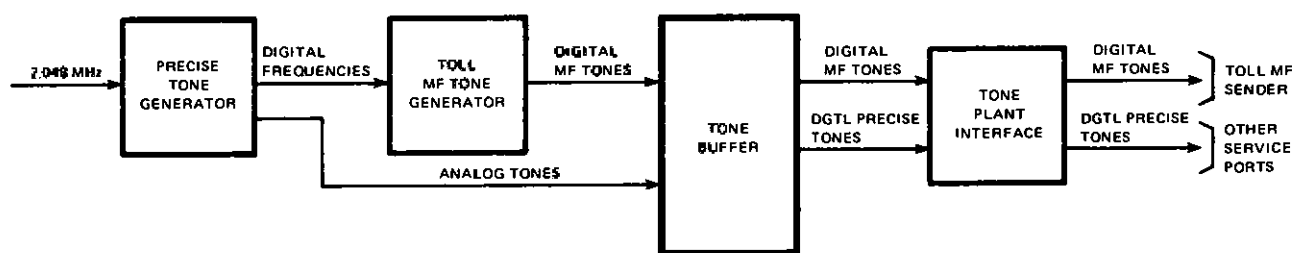
9.02 Figure 7 is a basic block diagram of the tone buffer. The outputs of the CODECs are multiplexed to produce a stream of serial bits that are written into a pair of ping-pong random-access memories (RAMs). The RAM outputs are demultiplexed into a format that is compatible with the timeslot interchange circuitry, which receives the tones. The demultiplexed PCM tones from the RAMs are sent to the tone source selectors on this and the redundant tone buffer PWBA. Simultaneously, demultiplexed PCM tones from the redundant tone buffer are also applied to the tone source selector of both circuits.

9.03 The PCM tone bits selected by the tone source selector are applied to the interrupt gating logic, along with ringing cadence signals from the ring line program logic circuit and the outputs of the inter-



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Figure 3. Nonprogrammable Ringing Equipment, Block Diagram



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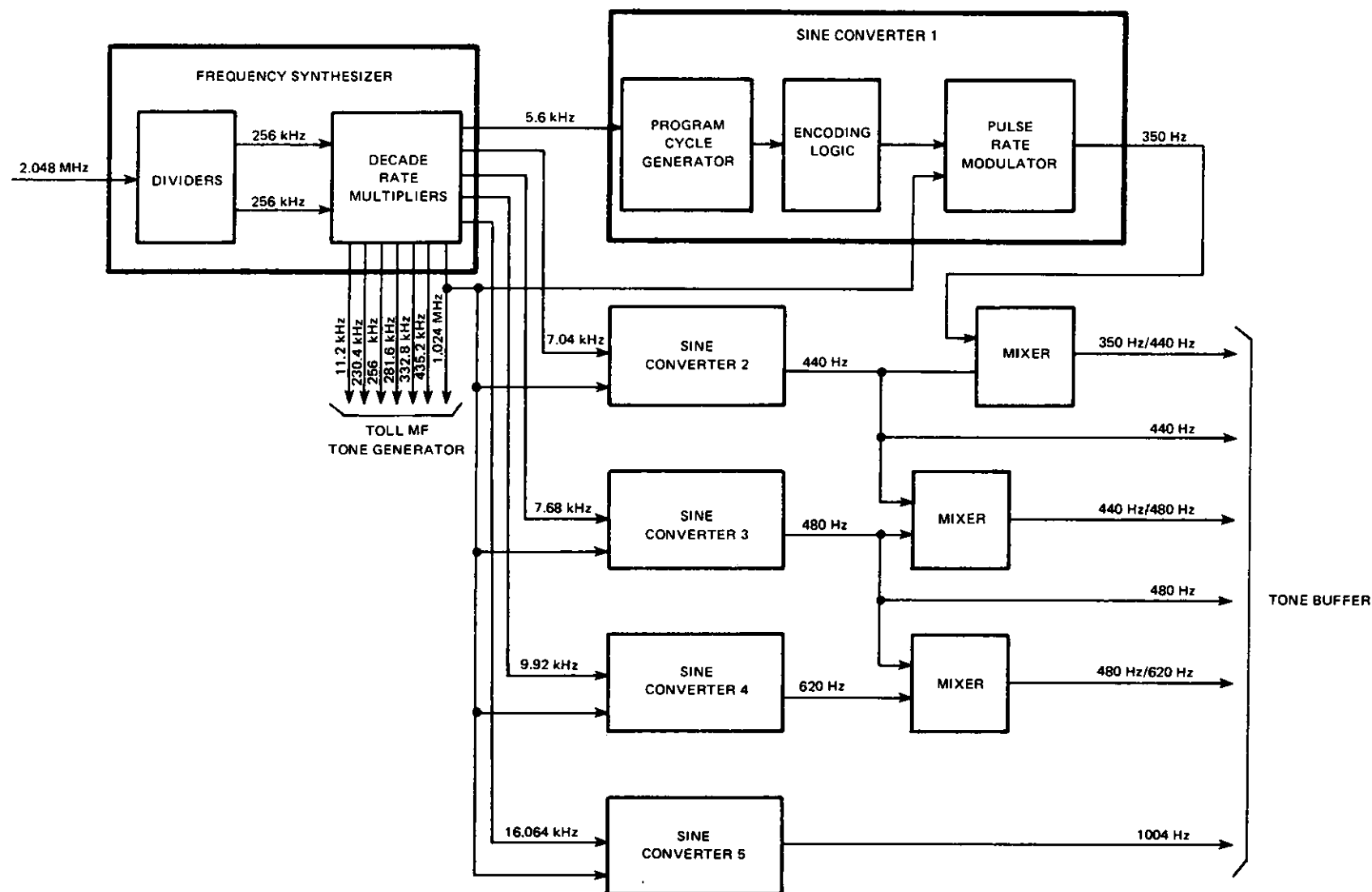
Figure 4. Tone Generation and Distribution

rupt counter. The interrupted tone signal outputs from this gating logic include the four phases of audible ringing (ringback), idle channel silence, and broadcast tones. These are multiplexed into a serial stream that is sent by the tone-out flip-flop and driver circuits to the timeslot interchange.

10. TONE PLANT INTERFACE

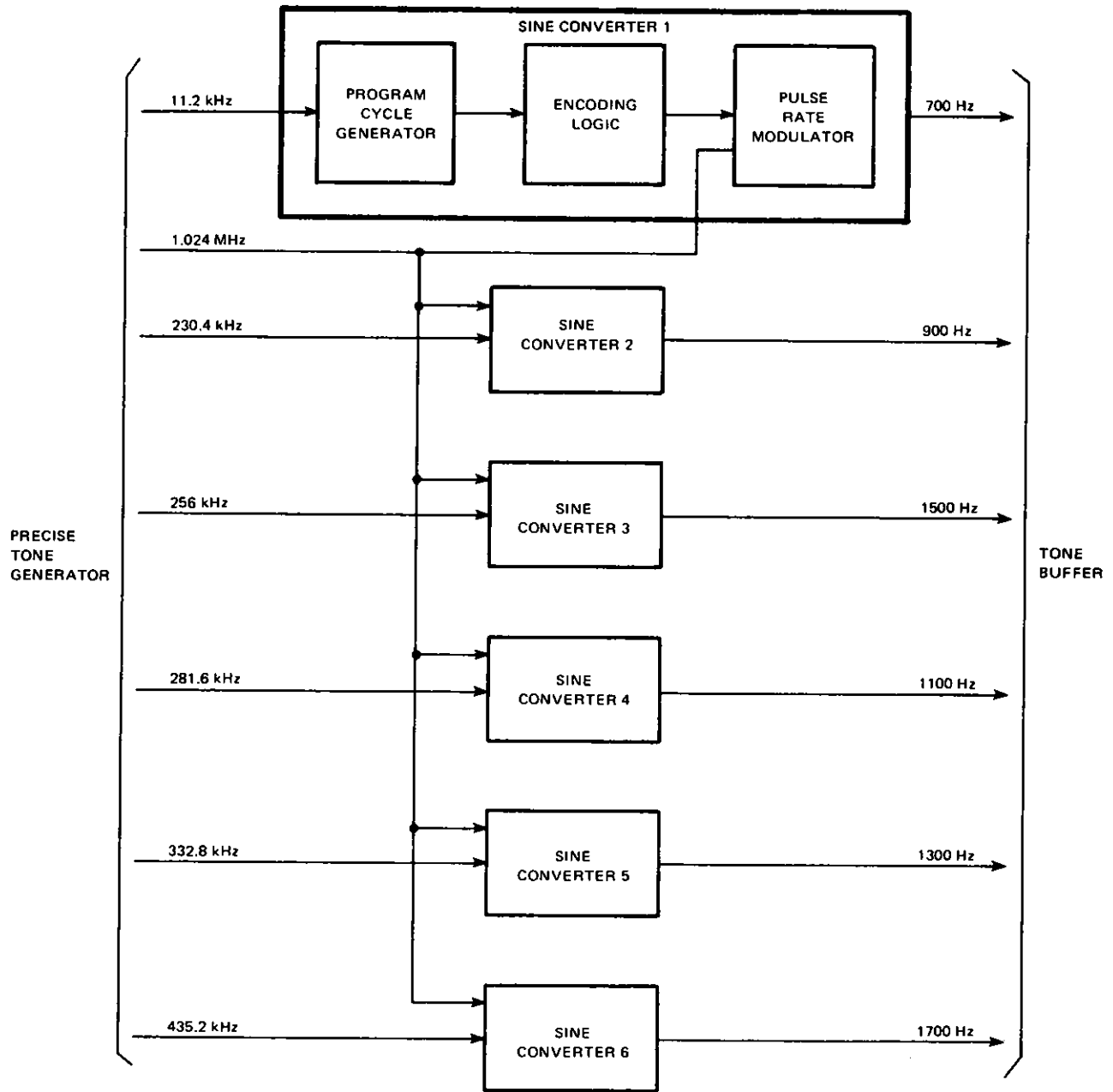
10.01 The tone plant interface serves as a receiver and buffer between the tone buffers and service ports such as the toll MF sender.

10.02 Twelve differential twisted-pair lines enter the tone plant interface from each redundant tone buffer (see figure 8). These pairs carry digital PRM and PCM frequencies from the on-line tone buffer. Six pairs carry 700-, 900-, 1100-, 1300-, 1500-, and 1700-Hz PRM frequencies developed by the on-line toll MF tone generator. The other six pairs carry 350/440-, 440-, 440/480-, 480-, 480/620-, and 1004-Hz PCM frequencies developed by the on-line precise tone generator.



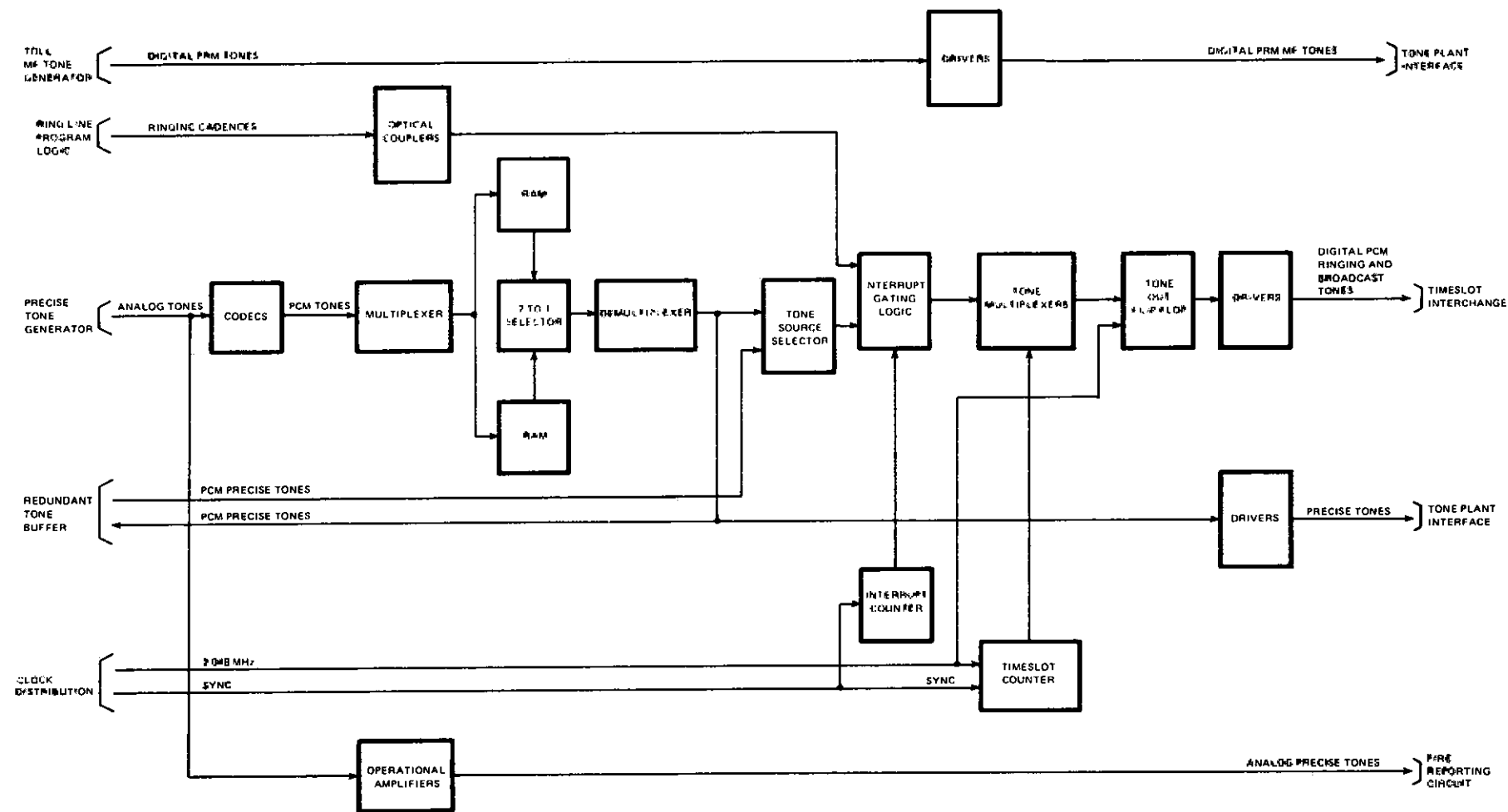
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Figure 5. Precise Tone Generator, Block Diagram



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Figure 6. Toll MF Tone Generator, Block Diagram



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Figure 7. Tone Buffer, Block Diagram

10.03 After conversion to single lines by the differential receivers, the signals are applied to exclusive-OR gates. This ensures that signals from only one tone buffer are passed through the tone plant interface. The PRM signals are then driven to the toll MF sender on six single lines. Likewise, the PCM signals are driven to other service ports on six single lines.

11. MASTER CLOCK GENERATOR

11.01 The redundant master clock generators are the source of all timing signals for the DCO, as shown in figure 9. If a Digital Trunk Interface (DTI) is used with the DCO, a synchronous network clock is used to synchronize the master clock generators with the digital network.

11.02 All timing signals produced by the master clock generator are derived from the output of a 24.576-MHz oscillator in the master clock generator (or synchronous network clock). By passing this oscillator output through frequency-dividing circuits, the clock develops the following signals:

- a. 8.192-MHz system clock with a 33-percent duty cycle.
- b. 122-nanosecond sync pulse occurring every 4 milliseconds (4-millisecond sync).
- c. 4-millisecond sync pulse occurring every 6.144 seconds (6-second sync).
- d. 4-millisecond sync pulse occurring every 131.072 seconds (131-second sync).

11.03 Error detection is done by using a duplicate of the source and frequency-dividing circuits, as shown in figure 10. For its source, the duplicate generating system uses an oscillator made of logic elements and passive components that oscillate naturally at about 24 MHz. An interconnection between the primary and duplicate source permits the primary source to step or synchronize the duplicate at precisely its own frequency. If the primary source fails, the duplicate oscillator continues generating timing signals. The error detection system, after detecting a discrepancy between the primary and duplicate systems, generates an error signal. A capacitor between the sources begins charging when the primary source fails and, after a certain time, disables the duplicate source. An alarm is generated and, if the failure occurred in the on-line master clock generator, a

switchover to the other generator occurs.

11.04 The primary and duplicate systems operate in a similar manner, as shown in figure 10. Both systems initially divide the 24.576-MHz oscillator output by 3 to produce an 8.192-MHz signal. The 8.192-MHz signal from the primary system is sent to the master clock distribution circuit.

11.05 The 8.192-MHz outputs of both divide-by-3 circuits are divided by 16 and applied to an exclusive-OR gate, which signals the alarm circuit if a difference occurs. The outputs of the divide-by-16 circuits are further divided by 2048, 256, 6, and 128 to produce the desired outputs. The primary and duplicate signals are applied to exclusive-OR gates at three additional critical points to detect errors.

11.06 Any signals produced by the error-detecting exclusive-OR gates generate an alarm which lights the alarm LED on the master clock PWBA and sends an error signal to the service group diagnostics circuit.

12. MASTER AND LOCAL CLOCK DISTRIBUTION

12.01 Each redundant master clock distribution circuit (fig. 9) receives 8.192-MHz, 4-millisecond sync, 6-second sync, and 131-second sync signals from both master clock generators. Monitoring circuitry detects any errors in both the on-line and off-line clock and sync signals and reports them to the service group diagnostics circuit. The master clock distribution circuit selects the signal inputs from either the X or the Y master clock generator and distributes these signals to local clock distribution circuits in each common control sector and in the maintenance and administration cell. Clock and sync signals are also distributed to the local clock distribution portion of this PWBA.

12.02 The local clock distribution portion of the PWBA receives 8.192-MHz and 4-millisecond sync signals from the master clock distribution circuit, generates a 2.048-MHz signal, and distributes all three signals to other circuits in the CPU, tone, and pulse cell. Any errors detected in the clock and sync signals received from the master clock distribution are reported to the service group diagnostics circuit.

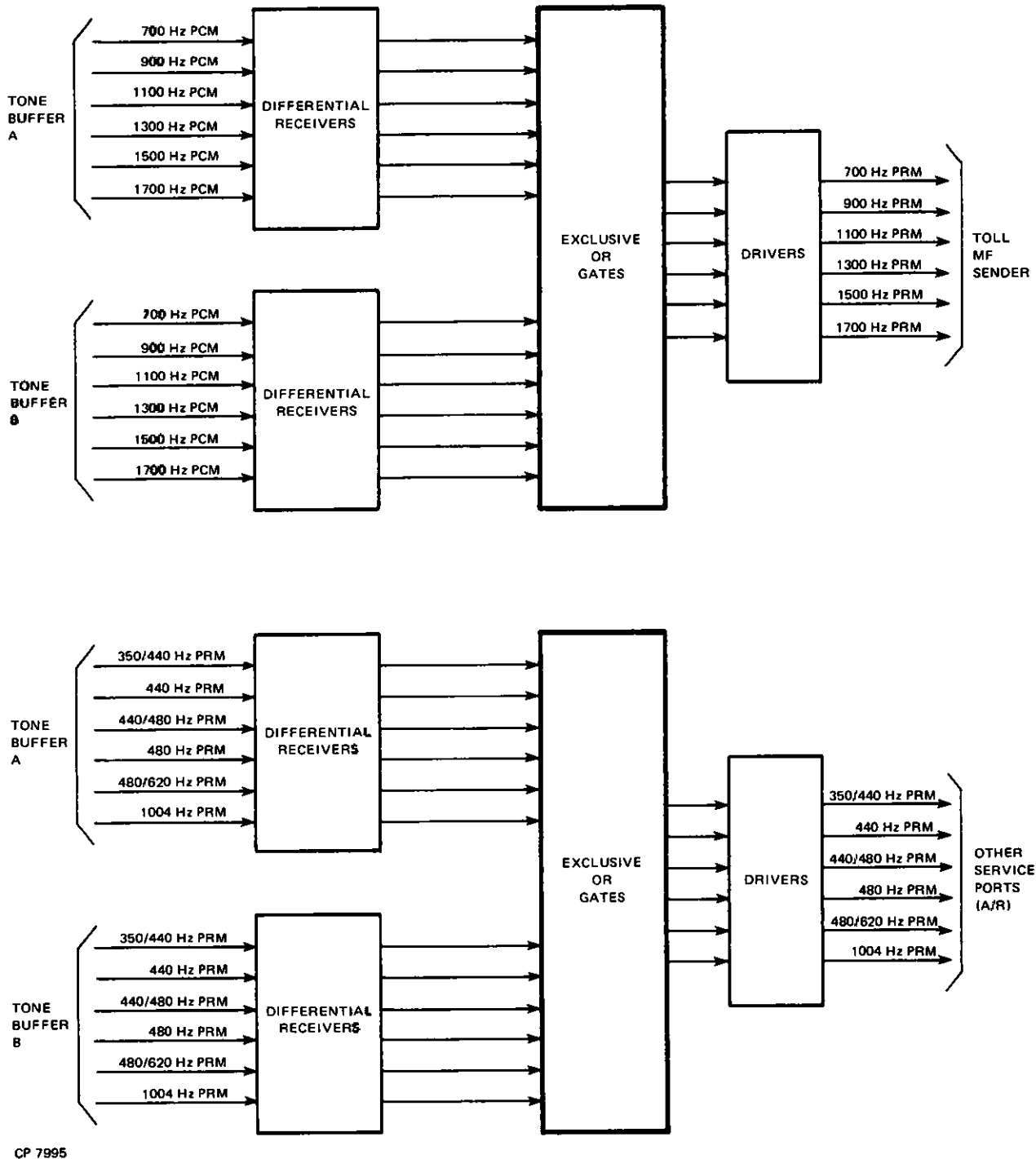
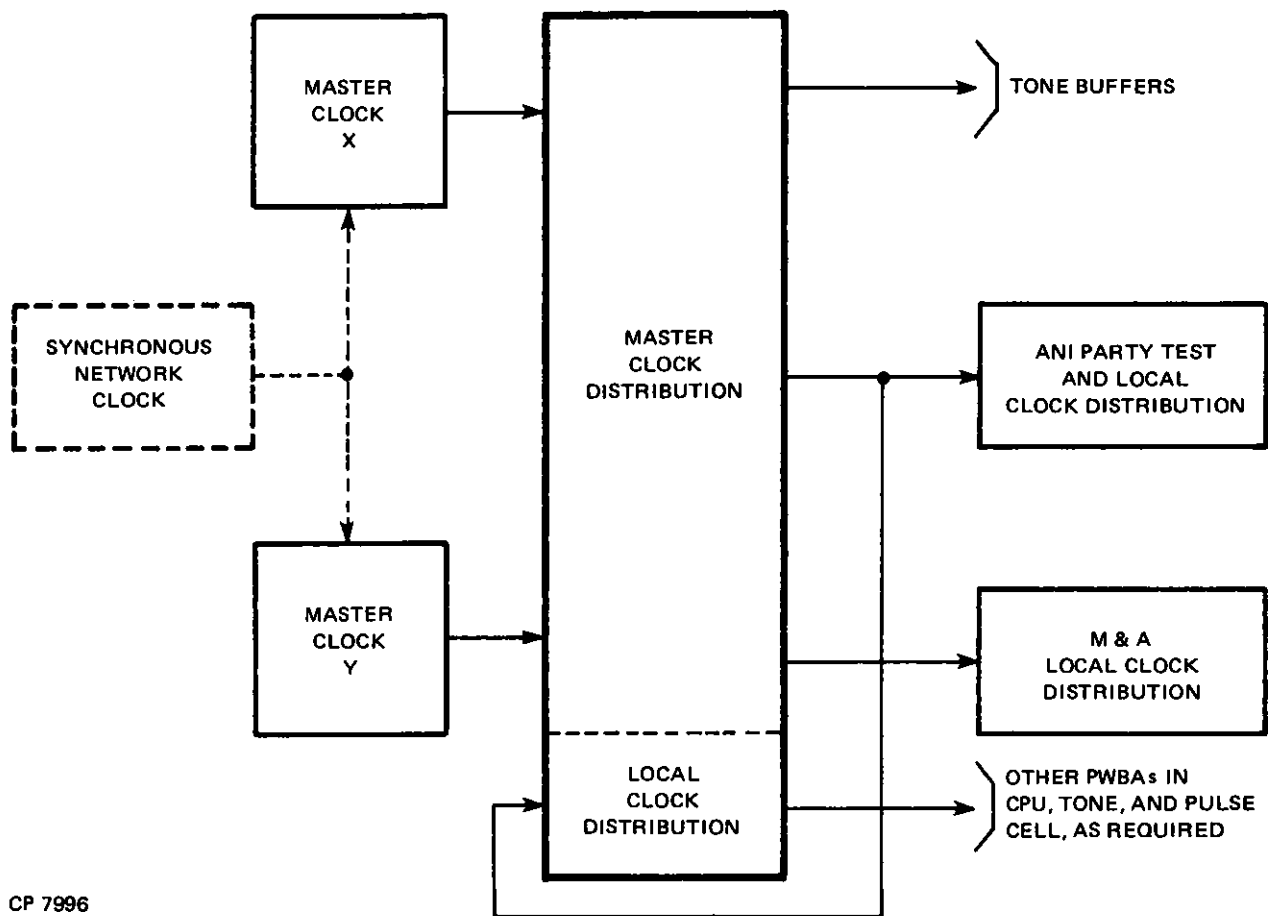


Figure 8. Tone Plant Interface, Block Diagram

13. ANI PARTY TEST AND LOCAL CLOCK DISTRIBUTION

13.01 Only the local clock distribution portion of this PWBA is discussed here. The circuit receives the 8.192-MHz clock and the 4-millisecond, 6-second, and 131-second sync signals from the on-line master clock

distribution circuit and distributes the signals to various circuits in the matrix switch/port control system (common control) cell and to the line group highway switch II circuits in each LLS frame. The circuits receiving the timing signals are the timeslot interchange, buffer control, matrix switch controller, port store controller, matrix



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Figure 9. Clock Distribution

expander, ring line program logic, receive supervisory event/send supervisory event program logic, timing and control, crosswrite, matrix switch/port control system diagnostics, and the ANI party test portion of this PWBA. In addition, the local clock distribution circuit develops a 2.048-MHz clock signal for any of the above circuits that require it.

13.02 The inputs from the master clock distribution circuit are applied to differential receivers (fig. 11). The 8.192-MHz output of the receiver passes through an adjustable delay line and drivers before being sent to the PWBA's that require the 8.192-MHz clock. One driver output also is used to develop a 2.048-MHz signal for circuits that require it.

13.03 The 4-millisecond sync output of the differential receiver is also applied to an adjustable delay line and then strobed into a flip-flop by the 8.192-MHz clock. The flip-flop output passes through a 40-nanosecond delay line and drivers before being sent to the required circuits as 4MS SYNC.

13.04 The 6-second and 131-second outputs of the differential receivers are sent directly to the circuits that require them. These signals also trigger one-shot multivibrators. If a one-shot is not triggered within a certain time, an error signal is sent to the service group diagnostics circuit.

13.05 A similar error-detection arrangement exists for the 8.192-MHz and 2.048-MHz clocks. Each of these signals is ANDed with a test signal from the service group diagnostics circuit and applied to a one-shot multivibrator. If either clock fails, the one-shot times out and generates an error signal. The maintenance processor can test the error detector by making either test signal low. This inhibits the associated clock, making the one-shot time out.

14. LOCAL CLOCK DISTRIBUTION (MAINTENANCE AND ADMINISTRATION)

14.01 The maintenance and administration (M&A) local clock distribution circuit receives the 8.192-MHz clock and the 4-millisecond and 6-second

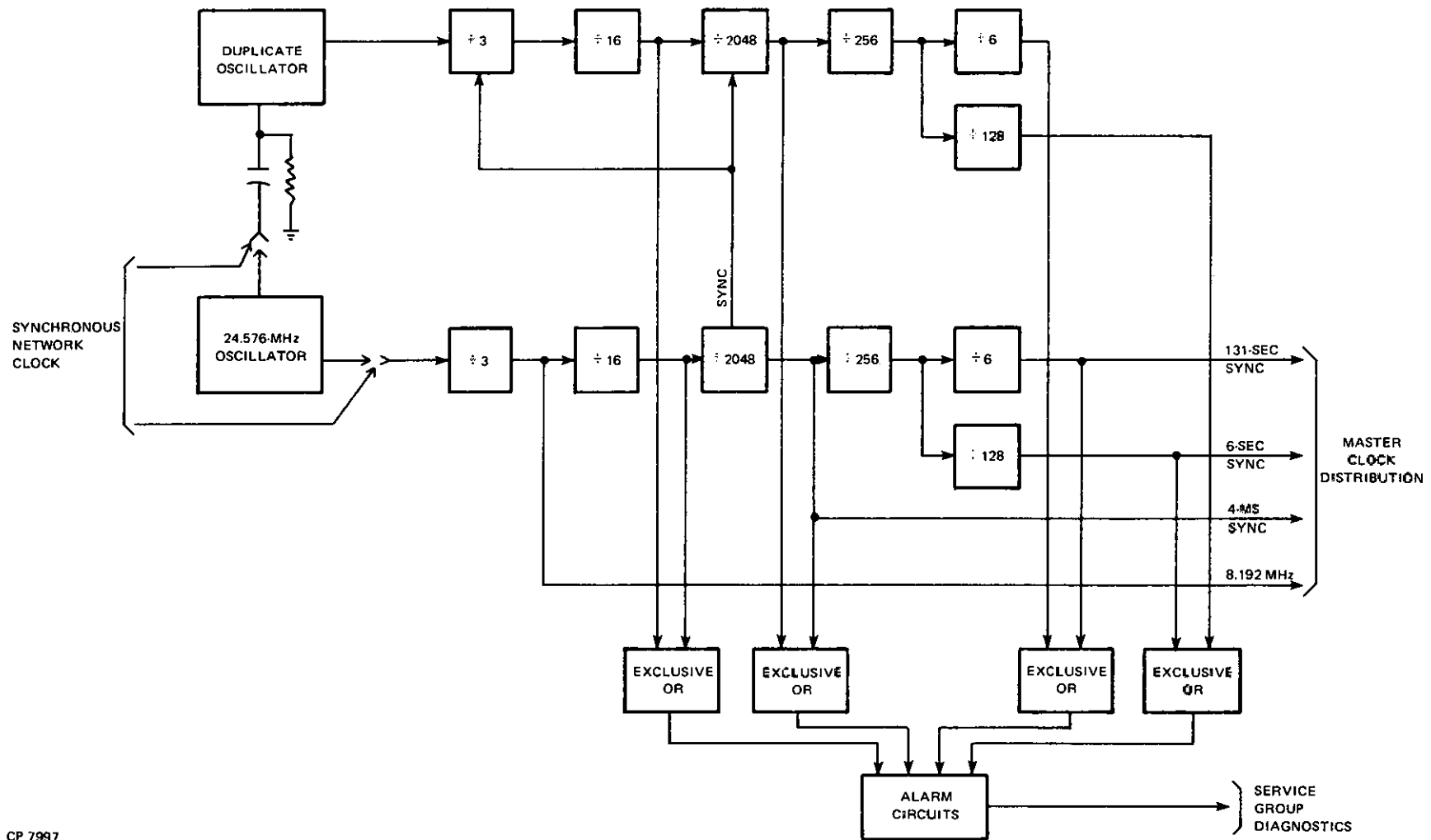


Figure 10. Master Clock Generator, Block Diagram

sync signals from the redundant master clock distribution circuits and distributes the signals to various M&A circuits. The circuits receiving the timing signals are the matrix switch diagnostics, service group diagnostics, and test call generators 1 and 3. In addition, the M&A local clock distribution circuit develops a 2.048-MHz clock signal for the above circuits.

14.02 The inputs from both redundant master clock distribution circuits are applied to differential receivers (fig. 12). The receiver outputs go to a data selector, where a signal from the switchover control circuit selects signals from one master clock distribution circuit (the on-line circuit).

14.03 The 8.192-MHz clock, besides being sent to the M&A circuits requiring it, is used internally to develop a 2.048-MHz signal and to clock the 4-millisecond sync flip-flop.

14.04 The 4-millisecond sync output of the data selector is strobed into a flip-flop by the 8.192-MHz clock. The flip-flop output passes through a 40-nanosecond delay line and drivers before being sent to the required circuits as 4MS SYNC.

14.05 The 6-second sync signal from the data selector is sent directly to the circuits that require it. This signal also triggers a one-shot multivibrator. If the one-shot is not triggered within a certain time, an error signal is sent to the service group diagnostics circuit.

14.06 Error detection is also provided for 8.192-MHz, 4.096-MHz, and 2.048-MHz clocks. The TRUE states of these three clocks are gated with the 2.048-MHz test signal from service group diagnostics and the NOT states of the three clocks are gated with the 8.192-MHz test signal. This produces, in each case, a low pulse every 488 nanoseconds (but not simultaneously) at each input of a latch. Since these pulses occur synchronously, the latch is first set by the pulse from the TRUE frequencies. The outputs of the latch, when it is set, trigger the error-detection one-shot. Then the pulse from the NOT frequencies resets the latch to remove the trigger inputs to the one-shot. Four hundred eighty-eight nanoseconds after the preceding pulse from the TRUE frequencies, the next pulse occurs to retrigger the error-detection one-shot. This occurs before the one-shot can time out, thus keeping its output high.

14.07 The output of the error-detection one-shot is used as a trigger for the clock-error one-shot. The 4MS SYNC signal is applied as the other trigger to keep the clock-error one-shot retriggered. If any of the three clock frequencies fails, both the error-detection one-shot and the clock-error one-shot time out to generate an error signal.

15. SYNCHRONOUS NETWORK CLOCK

15.01 The synchronous network clock (SNC) permits a DCO to have a direct digital connection to other digital equipment in a synchronous digital network. Each redundant SNC derives an 8-kHz clock from a T-1 span line. This clock is used as the primary timing reference for the SNC on which it is derived. The output of the SNC (24.576 MHz) is used as the primary timing source for the DCO by way of the master clock generator (par. 11).

15.02 The 8-kHz clock derived on each SNC is sent to the opposite SNC for use as a secondary timing reference. The A-side SNC also contains a highly stable dual oven-controlled crystal oscillator (OCVCXO) which is used as a third timing reference if both T-1 spans fail simultaneously. The accuracy of the OCVCXO can be updated to that of either span line, at any time, by software command. Software also controls all time-source switchovers, as well as masking and clearing faults.

15.03 The bipolar to unipolar converter (fig. 13) is the interface between the T-1 span and the SNC. The converter provides transfer coupling for ground isolation between the span and a pair of differential receivers in the converter. One receiver is biased positively, and the other is biased negatively; clamping diodes provide over-voltage protection to the receivers. The receiver outputs are ORed to provide full-wave rectification of the bipolar input for compatibility with the bit sync clock.

15.04 The bit sync clock is synchronized to the 1.544-MHz bit stream output of the bipolar to unipolar converter. The bit sync clock output is a 3.088-MHz clock which, after being divided down to 8 kHz, is used as the primary timing reference on that SNC. The 8-kHz clock is also used as a secondary timing reference on the opposite SNC.

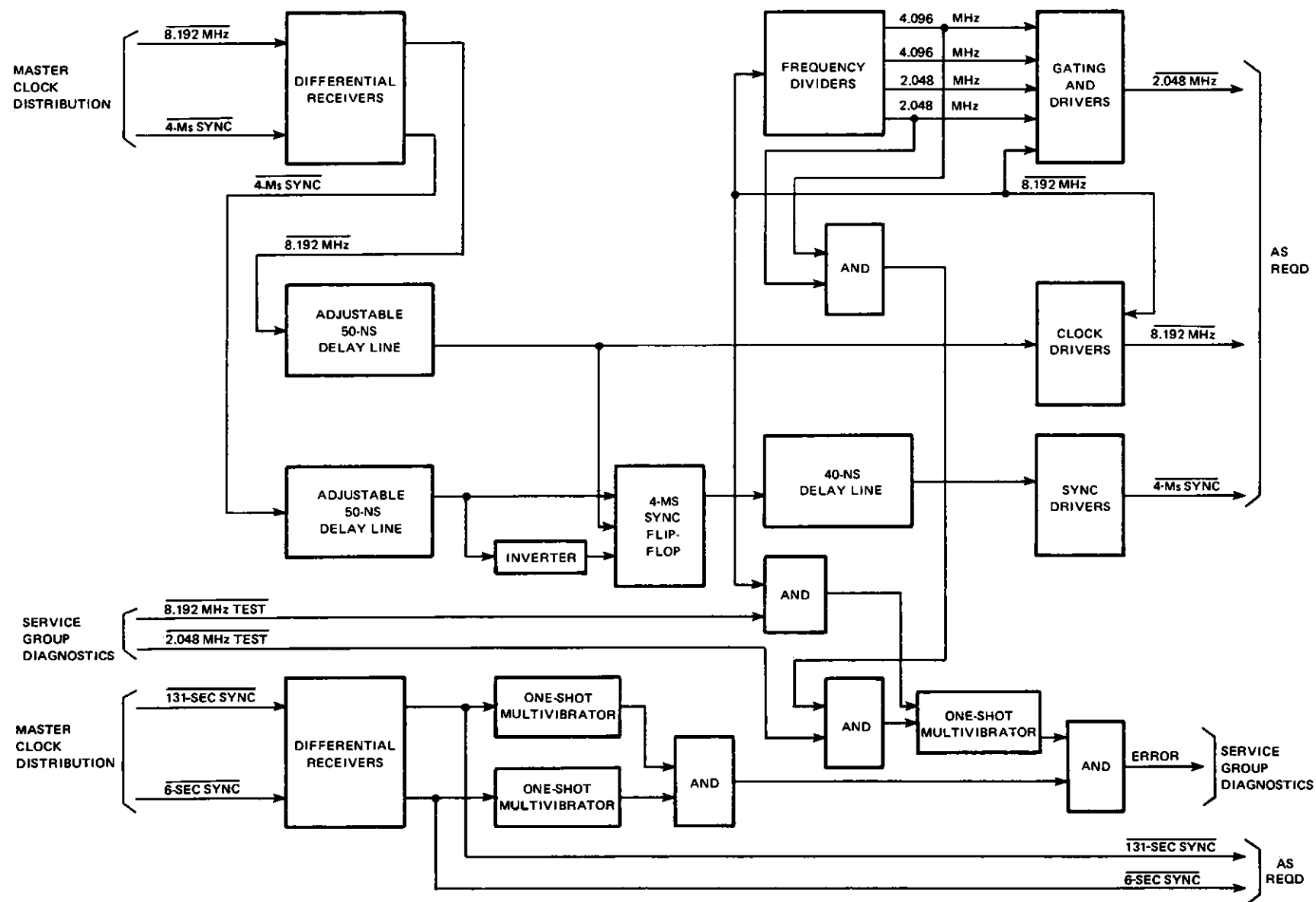


Figure 11. Local Clock Distribution (Common Control), Block Diagram

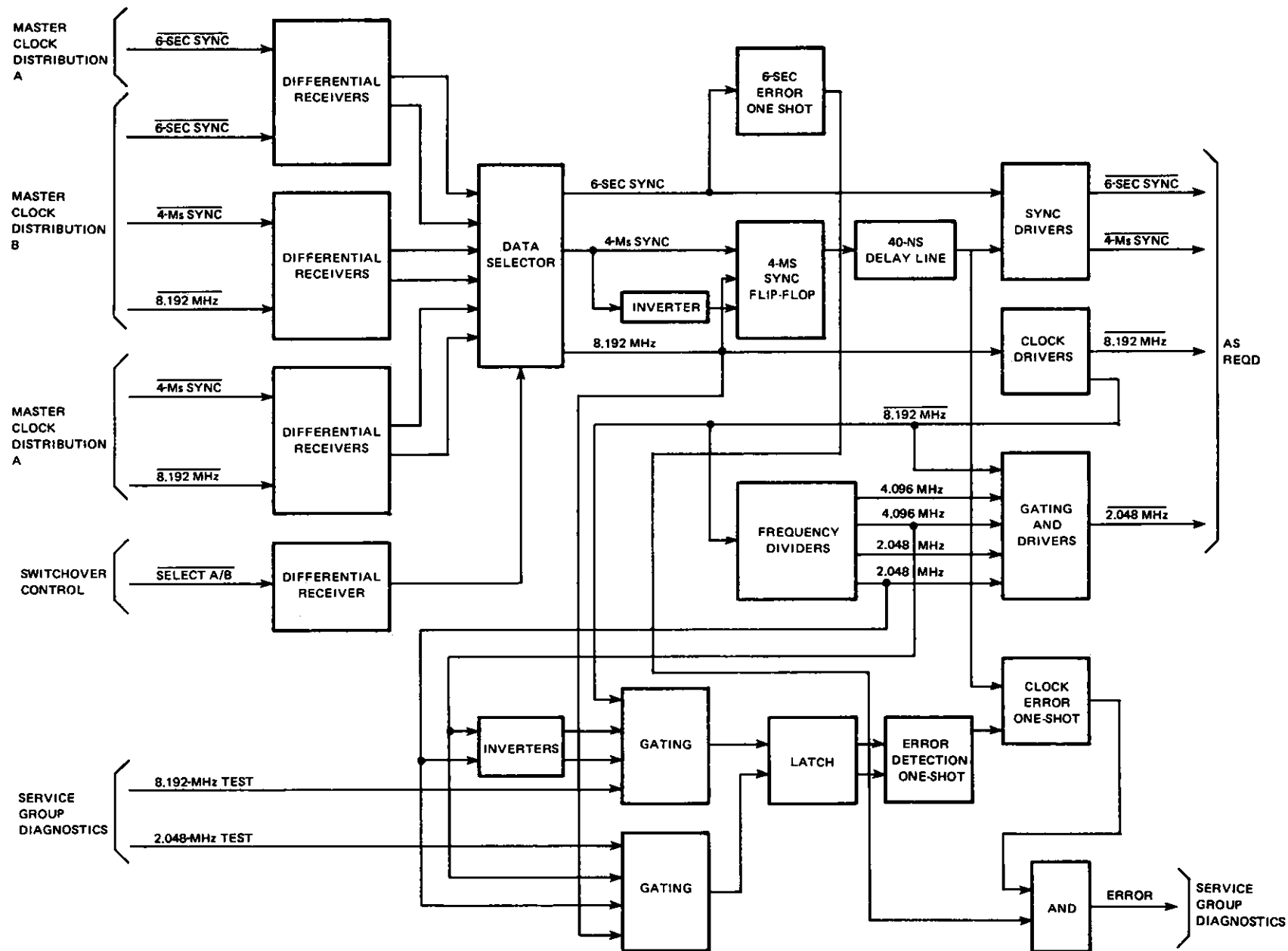


Figure 12. Local Clock Distribution (Maintenance and Administration), Block Diagram

15.05 The span switch receives 8-kHz inputs from the bit sync clock on the same SNC, the bit sync clock on the opposite SNC, and the OCVCXO on the A-side SNC. The span switch output is one of the above, as selected by software control.

15.06 A second order phase locked loop, consisting of a phase detector, low pass filter, voltage controlled crystal oscillator (VCXO), and 3072 divider, is synchronized to the 8-kHz output of the span switch. The VCXO output (24.576 MHz) is the timing source for the associated DCO master clock generator. The 3072 divider is tapped at 48 kHz to synchronize the OCVCXO.

15.07 The OCVCXO is part of another phase locked loop that also consists of a refresh control, phase detector, 4K digital memory, low pass filter, and 3072 divider. This loop is synchronized to the 48 kHz of the second order phase locked loop for two minutes after software initiation, and then the OCVCXO free runs at the frequency stored in the digital memory. The OCVCXO is used as a reference to monitor the outputs of the second order phase locked loops on both SNCs.

15.08 The fault monitor generates an alarm if any of the following occur:

- a. Drift rate between VCXO output and OCVCXO output exceeds certain limit.
- b. OCVCXO is near end of holding range.
- c. VCXO fails.
- d. OCVCXO fails.

16. TONE-DIAL DETECTOR INPUT

16.01 The TONE-DIAL detector input circuit receives dual-tone multifrequency (DTMF) signals from subscribers, converts the tones into dc pulses, and sends them to the TONE-DIAL detector output circuit. Figure 14 is a block diagram of the TONE-DIAL detector input circuit.

16.02 Each 2-out-of-7 (2/7) DTMF input signal is composed of one low tone (697 Hz, 770 Hz, 852 Hz, or 941 Hz) and one high tone (1209 Hz, 1336 Hz, or 1447 Hz). This signal is amplified and applied to two filter networks which separate the two tones.

16.03 Each filter output is applied to an amplifier/limiter which converts the tone into a square wave. The two square waves are then sent to the TONE-DIAL detector output circuit for frequency recognition.

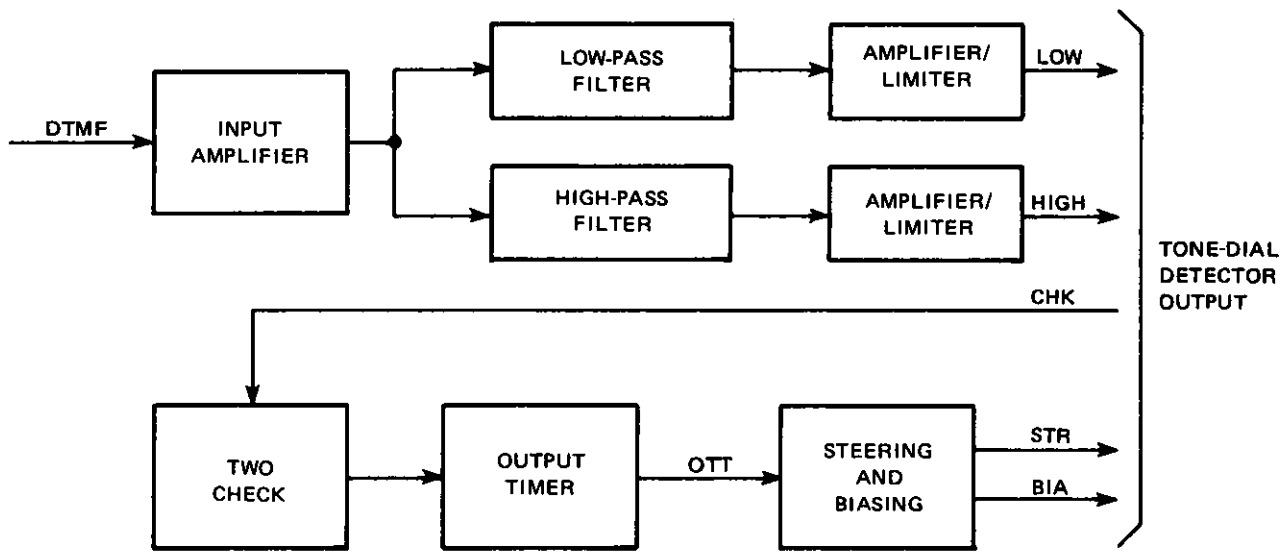
16.04 The two-check circuit receives a CHK signal from the TONE-DIAL detector output when that circuit detects a high and a low signal. The CHK signal energizes the signal timer in the two-check circuit, and the timer checks for the presence of two tones. If the two tones are verified for 25 milliseconds, the signal timer energizes the output timer. The output timer generates a 45-millisecond signal (OTT) for use by the steering and biasing circuit.

16.05 The steering and biasing circuit uses the received 45-millisecond signal to generate a steering ground (STR) signal and biasing (BIA) signal. The STR signal causes the TONE-DIAL detector output circuit to pass the two DTMF signals for 45 milliseconds. The BIA signal is used by the TONE-DIAL detector output circuit to inhibit all frequencies except the two valid ones.

17. TONE-DIAL DETECTOR OUTPUT

17.01 The TONE-DIAL detector output circuit recognizes and detects the low and high DTMF signals received from the TONE-DIAL detector circuit. The signals are then passed on to the multifrequency signal detector (MFSD) interface.

17.02 This circuit is divided into a low channel section and a high channel section, as shown in figure 15. The low channel section contains four narrow bandpass filters, each with an associated channel circuit. The filters are tuned to resonate at 697 Hz, 770 Hz, 852 Hz, and 941 Hz (the four low tones used in DTMF signaling). The -36-volt biasing signal (BIA) from the TONE-DIAL detector input circuit biases the first amplifier stage of each channel circuit. When a low tone is received, the appropriate filter resonates and turns on the first amplifier stage. This energizes the second stage in preparation for receipt of the STR signal (par. 16.05) and partially enables the CHK signal. A complete enable of the CHK signal by the low and high channel signals causes the TONE-DIAL detector input circuit to return the 45-millisecond STR signal. STR turns on the second amplifier stage to generate an output ground signal for 45 milliseconds.



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Figure 14. TONE-DIAL Detector Input Circuit, Block Diagram

17.03 The high channel section is similar to the low channel section, except it has three filter/channel circuits tuned to 1209 Hz, 1336 Hz, and 1447 Hz. Operation is identical to that described for the low channel section in paragraph 17.02.

18. TOLL MULTIFREQUENCY DETECTOR INPUT

18.01 The toll MF detector input circuit receives toll MF signals from trunks in 2/6 form, converts the signals into dc pulses, and sends them to the toll MF detector output circuit.

18.02 Each toll MF input signal is composed of two of the following: 700 Hz, 900 Hz, 1100 Hz, 1300 Hz, 1500 Hz, or 1700 Hz. This signal is applied to a high-pass filter (fig. 16), which forwards the signal to an AGC amplifier. The AGC amplifier output is a constant-amplitude signal that is applied to an audio amplifier.

18.03 The audio amplifier generates two identical signals which are applied to a holdover circuit and also sent to the toll MF detector interface circuit. The holdover circuit, comprised of a rectifier and pulse delayer, rectifies the signal into a -15-volt dc pulse for triggering the pulse delayer. KP, the first signal received, causes the pulse delayer to generate a 55-millisecond inhibit signal (DCM), which is sent to the toll MF detector output circuit.

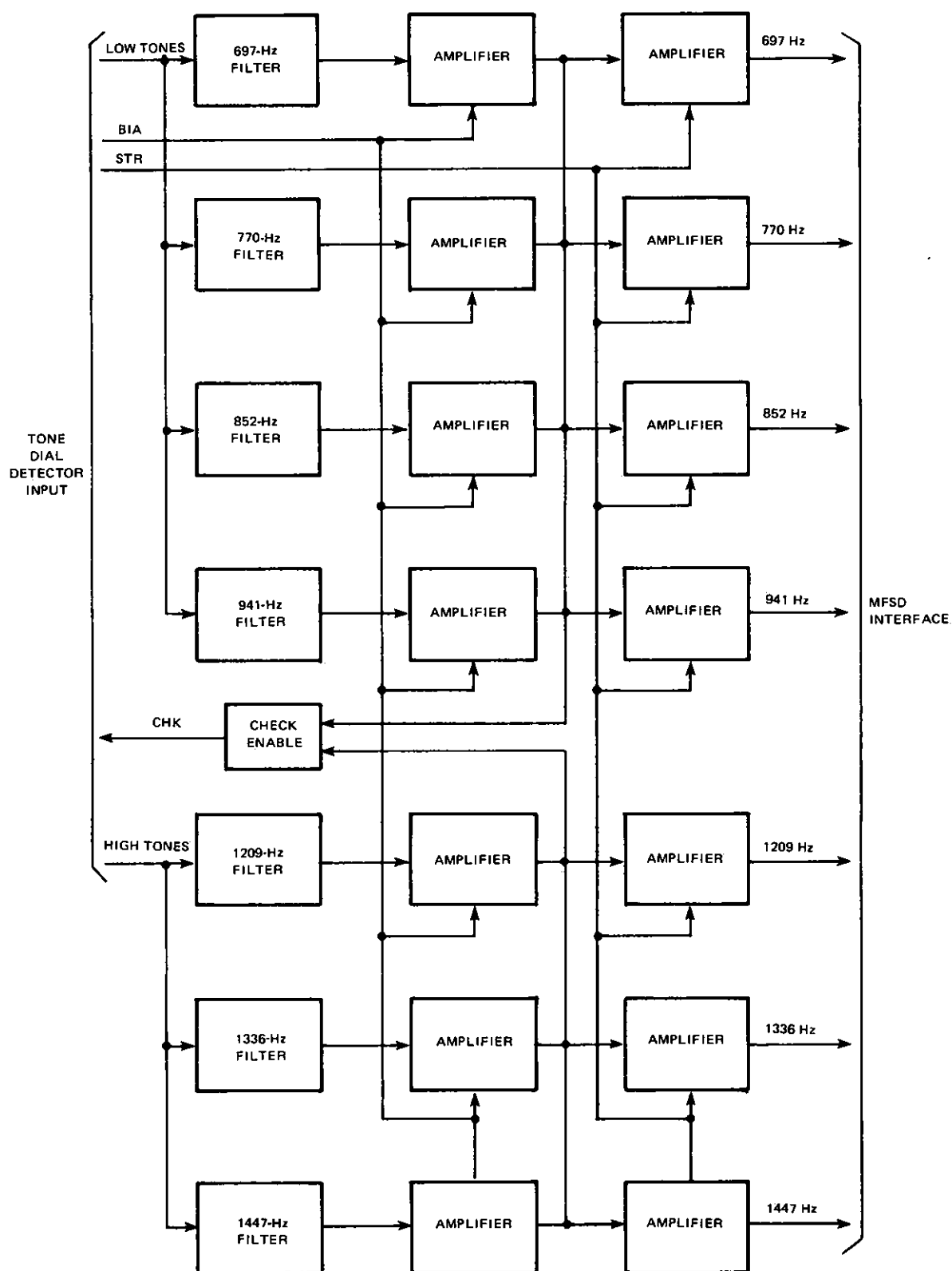
18.04 When DCM is removed, the two components of the KP signal are returned from the toll MF detector output circuit as DO3 and DO6, ANDED together, and used to set a flip-flop. The flip-flop, in parallel with the pulse delayer, reduces the delay (DCM) to 27 milliseconds. Setting the flip-flop also removes inhibit signal CHI from the toll MF detector output circuit.

18.05 As each digit signal is received and processed, it is checked by the toll MF detector output circuit for the presence of two frequency components. If only one is present, the toll MF detector output circuit is inhibited. If more than two are detected, CHO is returned to reset the flip-flop in the toll MF detector input circuit. This generates inhibit signals CHI and DCM, described previously.

18.06 After all digits have been received, a control signal is received. The two components of this signal (DO6 and DE) are returned from the toll MF detector output circuit, ANDED together, and used to clear the flip-flop. The circuit is now ready to receive the next series of signals, beginning with KP.

19. TOLL MULTIFREQUENCY DETECTOR INTERFACE

19.01 The toll MF detector interface receives MF signals from the toll MF detector input circuit, separates the two tones, and sends them to the toll MF detector output circuit. Two toll MF detector interface circuits are contained on each PWBA.



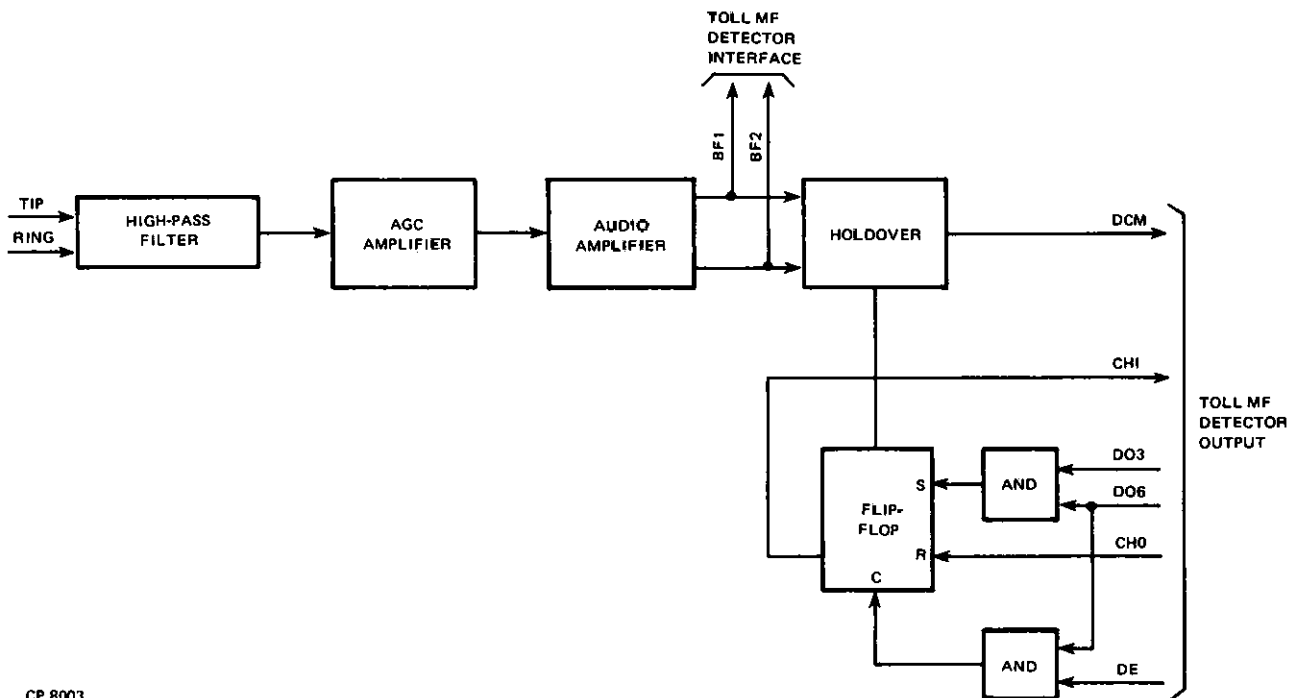


Figure 16. Toll MF Detector Input Circuit, Block Diagram

19.02 The two identical tone inputs from the toll MF detector input circuit are applied to six band-pass filters, tuned to 700 Hz, 900 Hz, 1100 Hz, 1300 Hz, 1500 Hz, and 1700 Hz. The two frequencies that make up each received signal are passed by their respective filters and sent to the toll MF detector output circuit.

20. TOLL MULTIFREQUENCY DETECTOR OUTPUT

20.01 The toll MF detector output circuit (fig. 17) decodes the MF tones received from the toll MF detector interface and sends the tones to the toll MF detector decoder.

20.02 When the KP signal is received at the beginning of a message, the DCM inhibit signal is generated for 55 milliseconds, as described in paragraph 18.03. After DCM is removed, the two components of the KP signal are allowed to pass through the detectors and output gates of the toll MF detector output circuit. DO3 and DO6, the zero outputs of the two KP components are used by the toll MF detector input circuit to shorten DCM and remove CHI, as described in paragraph 18.04. Removal of CHI enables the two-check circuit, which is operated by the one outputs (CH3 and CH6) of the two KP components. If two, and only two, frequen-

cies are present, the two-check circuit enables the output gates to pass the KP signal to the toll MF detector decoder as RD2 and RD10.

20.03 Each digit signal generates DCM for 27 milliseconds to inhibit the detectors of the toll MF detector output circuit. After DCM is removed, the detectors and the two-check circuit are enabled. The digit signal is then processed and sent to the toll MF detector decoder as two RD() signals.

20.04 If only one frequency component is received, the two-check circuit inhibits the output gates. If more than two components are received, the three-check circuit sends the CHO inhibit to the toll MF detector input circuit (par. 18.05). This generates inhibit signals CHI and DCM, requiring the entire sequence (beginning with KP) to be repeated.

20.05 After the last digit signal in a sequence is received, a control signal is received. This is treated the same as any other signal but, when the two signal components (DO6 and DE) are sent to the toll MF detector input, they restore the holdover circuit to the 55-millisecond condition. The circuit is now ready to receive the next series of signals, beginning with KP.

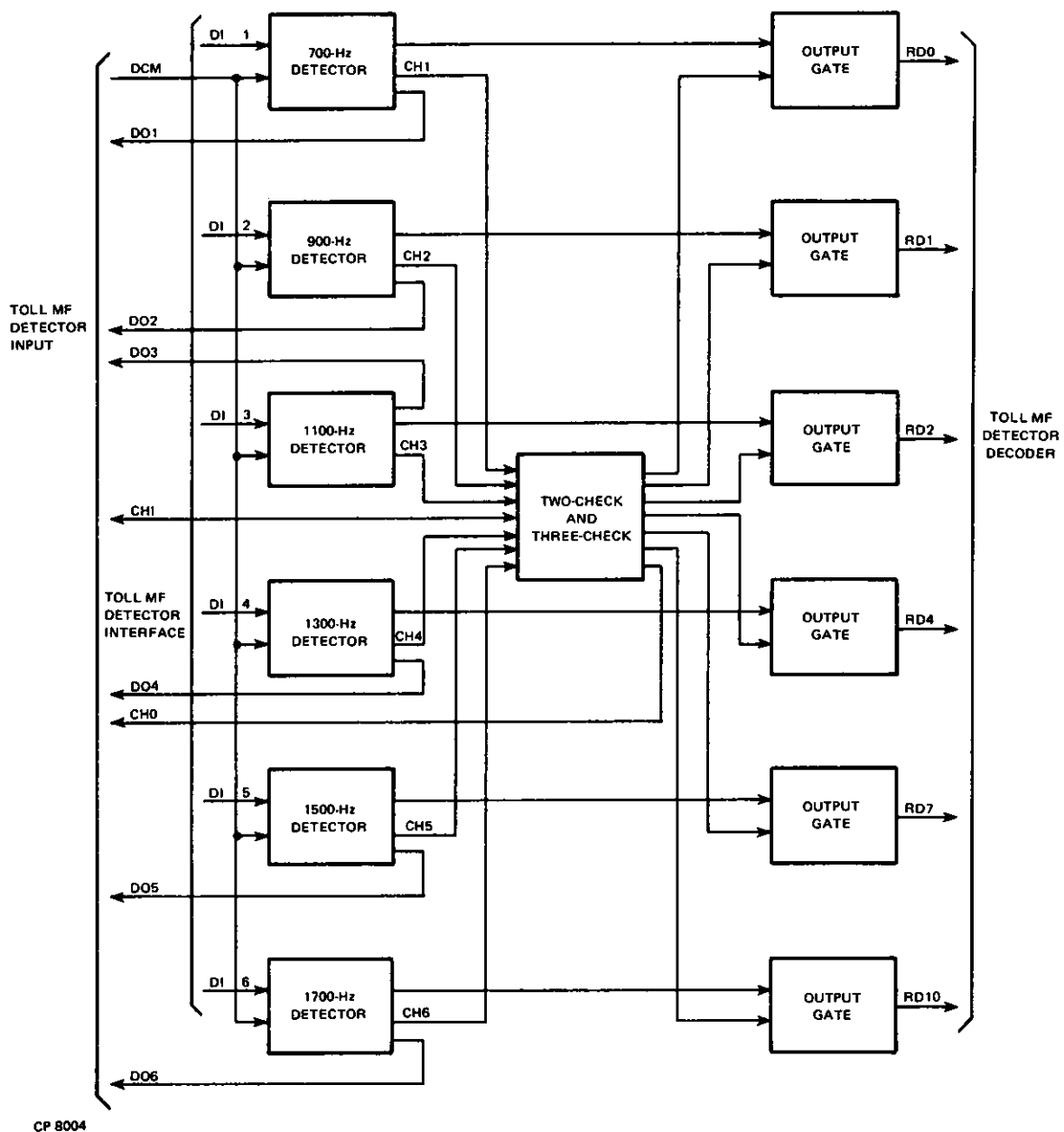


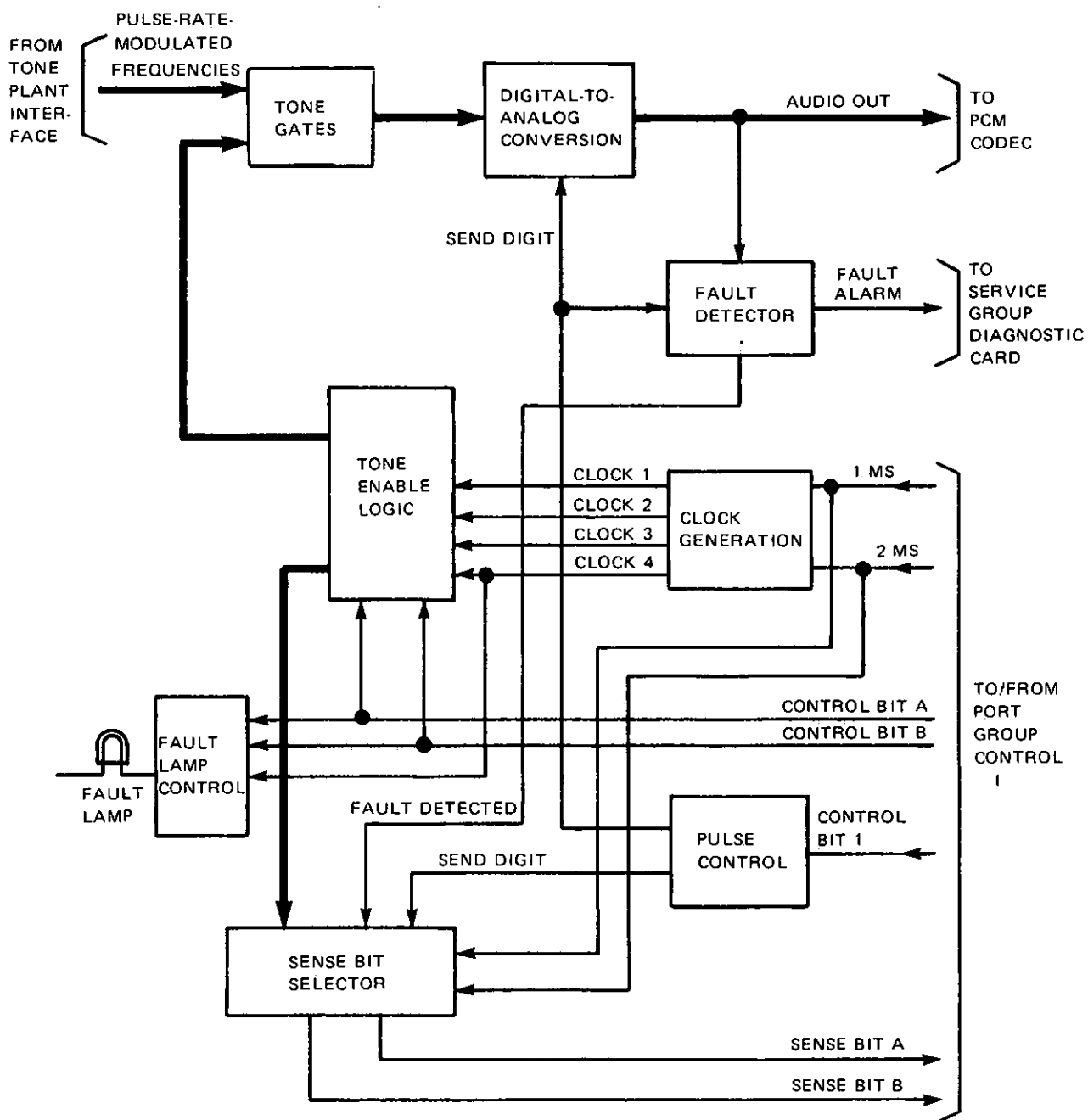
Figure 17. Toll MF Detector Output Circuit, Block Diagram

21. TOLL MULTIFREQUENCY SENDER

21.01 Toll MF, or 2/6 MF pulsing, is used to transfer numerical information between switching centers and to provide calling-party information to an AMA recording center. The toll MF sender circuit is a service port circuit. It receives six pulse-rate-modulated (PRM) frequencies (700 Hz, 900 Hz, 1100 Hz, 1300 Hz, 1500 Hz, and 1700 Hz) from toll MF generators by way of tone buffers and the tone plant interface circuit; selects two of these frequencies as determined by the port control system; converts them to sine waves; and then com-

bines the two sine waves into one tone. This tone is converted to a PCM digital signal by the PCM CODEC for transfer through the timeslot interchange to a port. Two identical toll MF sender circuits are contained on one toll MF sender PWBA 814555-026.

21.02 The six signals from the tone plant interface circuit are ANDed with enabling signals from the tone enable logic as shown in figure 18. By decoding supervisory control bits A and B and the four clock signals developed from the 1-MS and 2-MS signals by the



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Figure 18. Toll MF Sender, Block Diagram

clock generator, the tone enable logic determines which two enabling signals are applied to the tone gates. The two gated PRM signals are applied to the digital-to-analog conversion logic and, during the period that control bit 1 is true at the pulse control logic, the PRM signals are converted from digital pulse trains to analog sine waves. These are then combined into a single analog tone pulse that is outputted to the PCM CODEC.

21.03 The 1-MS and 2-MS signals that drive the clock generation logic are generated by the PGC 1 circuit to define which pair of supervisory bits is being transferred. Converted into four clock signals by the clock generator, 1-MS and 2-MS signals define which pair of control bits is present at the tone enable logic. These two signals also are applied to the sense bit selector to define which of the inputs (tone enables, fault detection,

or pulse enable) are to be gated through as sense bits A and B.

21.04 If the toll MF sender develops either fewer or more than two tones because of a malfunction, the fault detection logic generates a fault alarm to the service group diagnostics and outputs sense bit S0. When the failure has been recognized by the maintenance processor, control bit S7 is issued to the fault lamp control logic to light the lamp. At the discretion of the maintenance processor, the lamp is extinguished later by control bit S0.

21.05 Failure of a component, causing the loss of any of the six parallel paths through a single circuit on a toll MF sender card, disables that entire circuit function, since combinations of tones or frequencies are required. A component failure can affect MF tone generation, toll calling, and/or alarm functions.

22. MFSD INTERFACE

22.01 The multifrequency signal detector (MFSD) interface circuit is a service port circuit that is used to transfer tone and supervisory information between a toll multifrequency (MF) detector and one toll-trunk port, or between a TONE-DIAL detector and an MF subscriber port by way of the TSI. Two identical MFSD interface circuits are provided on each MFSD interface PWBA 814489-026. Figure 19 shows the interconnections of various circuits associated with the MFSD interface circuit.

22.02 Each interface circuit is comprised of eight optical couplers, a multiplexer, and a flip-flop. The functional relationships of these circuit elements are shown in the block diagram in figure 20. Strapping arrangements on this PWBA allow either circuit to be associated with a toll MF detector or a dual-tone multifrequency (DTMF) detector.

22.03 Analog tone signals addressed to the MFSD interface are first sent to either a toll MFSD or a DTMF detector. The toll MFSD has six output leads and produces two output signals out of six (2/6) for each digit (tone) fed into it. The DTMF detector operates in a similar fashion, producing two outputs out of seven (2/7) for each digit fed into it. The two-signal code produced by either MF detector is applied to optical couplers in the MFSD interface where the signal level is converted from -48 volts or ground to +5 volts (TTL-compatible level). The two signals are then applied to an eight-to-two line multiplexer. The two inputs to the multiplexer are converted to a pattern of supervisory sense bits on leads SBSA and SBSB, which are sent to the PGC 1 circuit, to the TSI, and then loaded into the PCS; sense bit pairs on one or both of these leads represent individual digits from the MFSD or the DTMF signal detector.

22.04 Each MFSD interface circuit has an alarm circuit that is activated by the PCS. Receipt of supervisory control bit CBS7 from the PCS sets the alarm flip-flop, which lights the alarm lamp on the edge

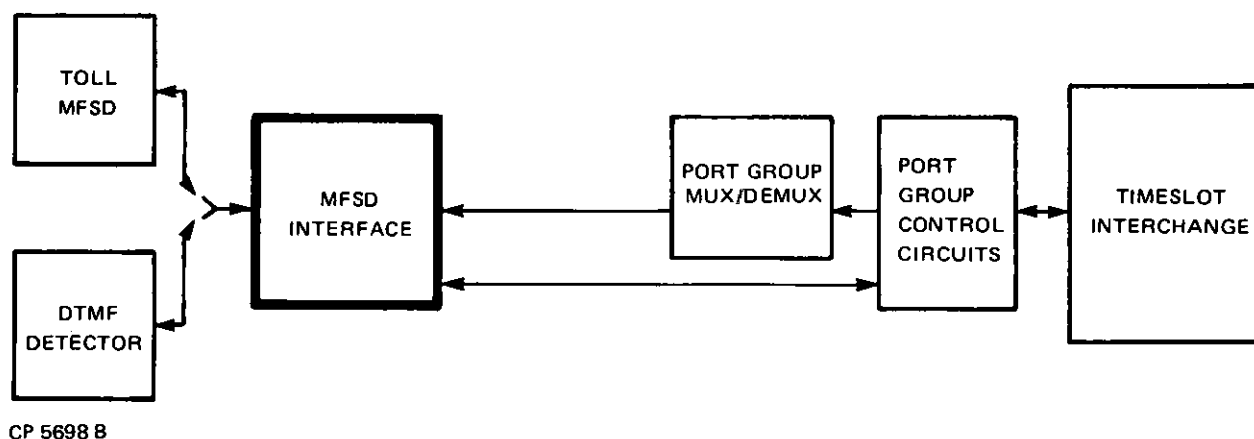


Figure 19. MFSD Interface, Orientation Diagram

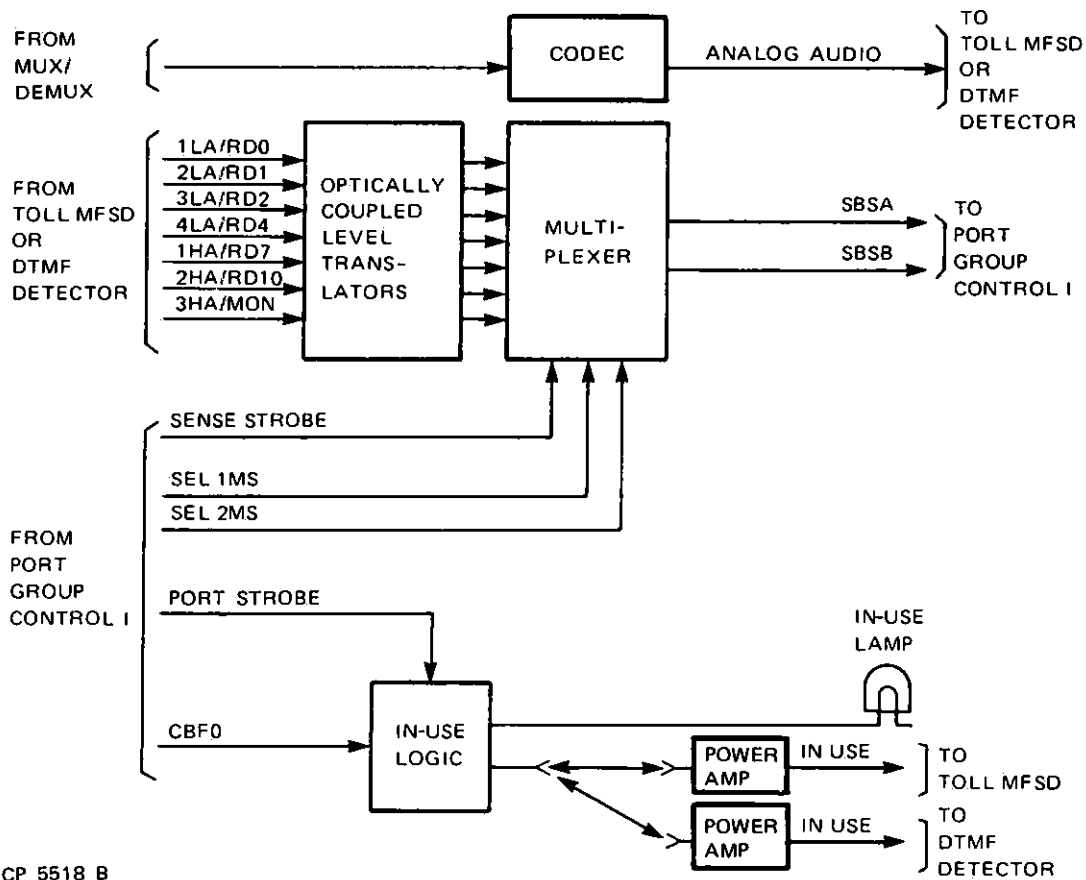


Figure 20. MFSD Interface, Block Diagram

of the MFSD interface. Control bit CBF0 is used to set an IN-USE flip-flop on the MFSD interface circuit when the circuit is busy. This flip-flop, through an optical coupler, lights an LED on the edge of the PWBA and operates two drivers. One driver provides ground to the associated DTMF detector when the interface is not busy. The other driver applies ground to the associated toll MFSD when the interface is not busy. Only one of the drivers is used in a given application, since the MFSD

interface circuit can serve only one type of detector in any application.

22.05 Failure of an interface circuit inhibits service usage of its associated detector. Normally one or two detector outages cause only a small degradation to traffic and, therefore, are considered as minor failures. A component failure in this circuit can cause failure in DTMF dialing, alarms, etc.

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