

[54] **OPERATION AND RELEASE DELAY CIRCUIT**

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[56] **References Cited**

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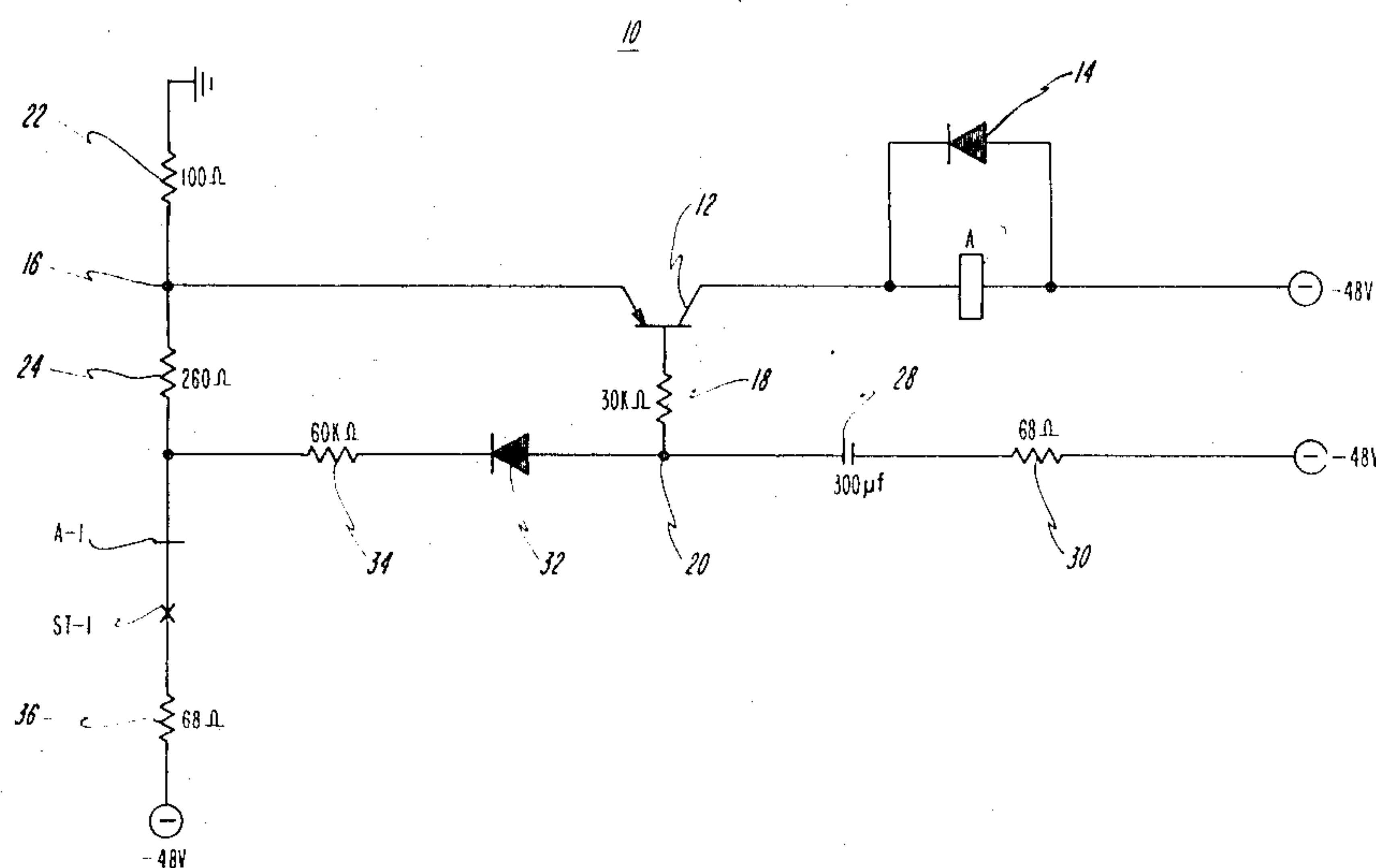
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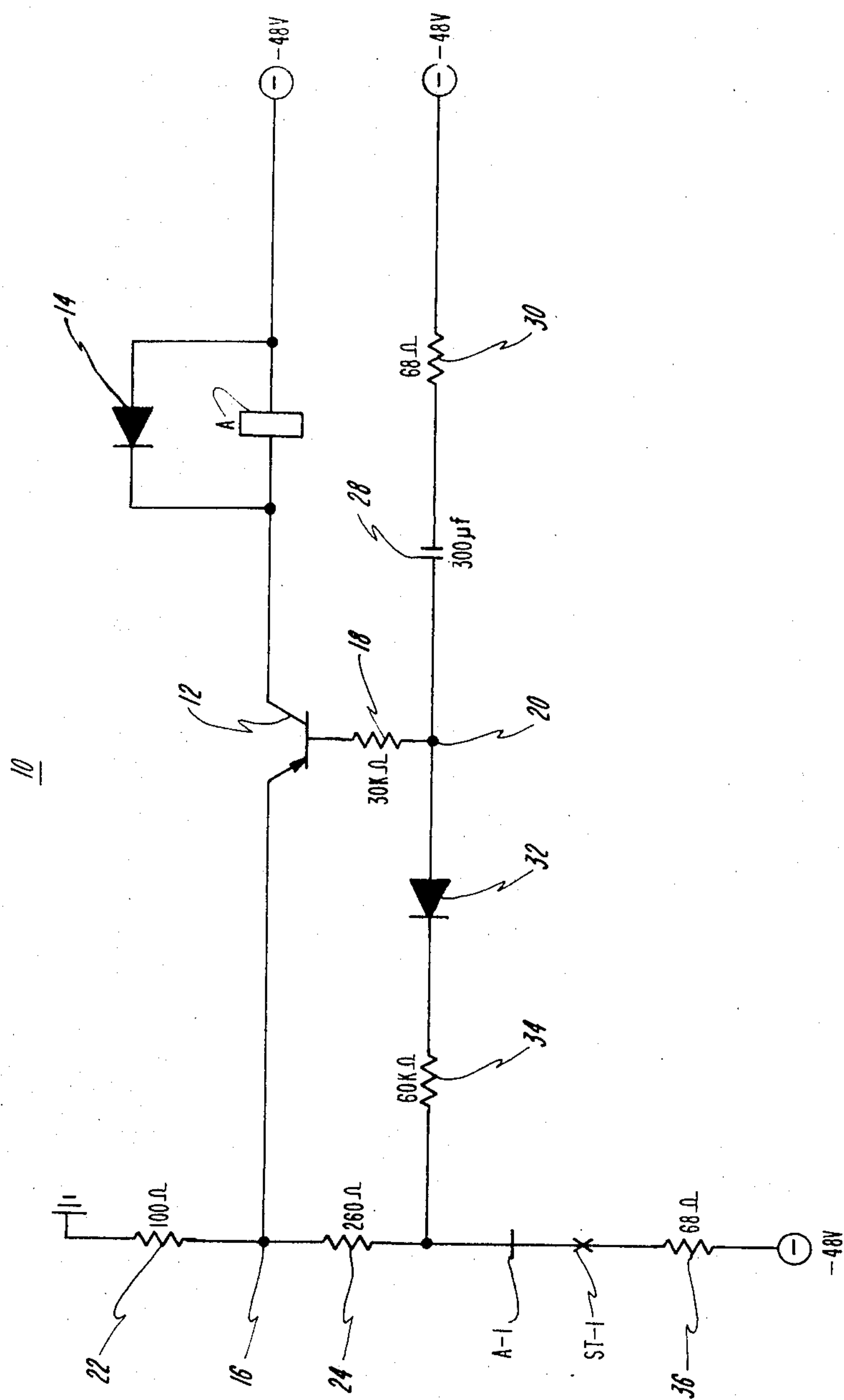
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[57] **ABSTRACT**

An electrical circuit is provided which furnishes delays of predetermined durations in both the operation and release cycles of a selected device. The circuit, which may be fabricated in card mounted form, automatically releases the device a predetermined time after the device has been operated without requiring the application of an externally generated signal to effect the release.

5 Claims, 1 Drawing Figure





OPERATION AND RELEASE DELAY CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates generally to time delay circuitry and, in particular, to circuitry which provides a time delay both in the operation cycle and in the release cycle of a selected device.

Conventional delay circuitry which is currently in use typically employs a capacitor or an R-C filter circuit connected either in series or in parallel with the device whose operation or release time it is intended to delay. Most of these circuits operate to delay only one of the operation time or the release time of the device and the additional delay of the release or the operation, respectively, is typically effected by means of a signal which is generated externally of the delay circuitry.

Although such circuitry has generally been satisfactory in those applications in which it has been employed, it has not by itself performed satisfactorily in instances in which a delay in both the operation time and the release time of the operable device is desired and has required the addition of other time delay components to attain the desired results.

Accordingly, it is an object of the present invention to provide a delay circuit which provides the desired time delays both in the operation cycle and in the release cycle of a selected device.

It is another object of the present invention to provide such a delay circuit which automatically internally releases the selected device a predetermined time after the device has operated without requiring the application of signals from circuitry external to the delay circuitry.

Still another object of the present invention is to provide such an operation and delay circuit which does not require the addition of external devices to existing circuitry to provide delays of the desired durations in both the operation and release cycles of operation.

A further object of the present invention is to provide such a delay circuit which is relatively simple and inexpensive and which may be produced in card mounted form.

BRIEF DESCRIPTION OF THE INVENTION

A new and improved electrical circuit for delaying both the operation and release cycles of a selected device which is operable via a pulse applied to an input thereof. The circuit permits release of the device after it has been operated without requiring the application of an externally generated signal to the input.

In accordance with the invention, a relay has one side thereof connected to a negative voltage supply and the other side connected to ground potential via a transistor. A capacitor is connected via a first resistor to the base of the transistor and via a second resistor to the input, and a voltage divider, connected between the input and the ground potential, is connected intermediate the ends thereof to the emitter of the transistor. In the absence of a negative pulse applied to the input, the capacitor charges via the transistor and maintains the emitter-base bias of the transistor at a sufficiently low value to prevent the transistor from switching on, thereby preventing the relay from operating. When a negative pulse is applied to the input, the relay does not become energized immediately; rather the operation time of the relay is delayed by the discharging of the ca-

pacitor through the resistor connected in series between the capacitor and the input. As the capacitor discharges, the emitter-base bias of the transistor increases and when the transistor switches on, the relay becomes energized.

When the relay becomes energized, a normally closed contact pair, connected in series with the input, opens, and the capacitor begins to become charged again through the resistor connected between the base of the transistor and the capacitor. The time thus required for the capacitor to charge to a voltage magnitude sufficient to bias the transistor off results in a delay in release of the relay of a predetermined duration.

BRIEF DESCRIPTION OF THE DRAWING

Other objects, features and advantages of the present invention will become apparent from the following description of a particular embodiment, taken together with the attached drawing thereof, which is an electrical schematic wiring diagram of an operation and release delay circuit constructed in accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawing, the operation and release delay circuit, generally designated 10, will now be described in detail. A relay, designated "A," is connected between a -48 volt supply and the collector of a PNP transistor 12 and a diode 14 is connected in parallel therewith. The emitter of the transistor 12 is connected to a junction 16 and the base of the transistor 12 is connected via a resistor 18 to a junction 20. The junction 16 is connected via a resistor 22 to ground and via a resistor 24 to a junction 26. The junction 20 is connected via a capacitor 28 and a resistor 30 to a -48 volt supply and is also connected via a diode 32 and a resistor 34 to the junction 26. The junction 26 is connected via a normally closed (break) contact pair A-1 of the relay A, a normally open (make) contact pair ST-1 (which is arranged to be operated by external starting circuitry which is not shown) and a current limiting resistor 36 to a -48 volt supply. (Alternatively, the contact pair ST-1 may be directly connected to the -48 volt supply in many applications.)

In operation, when the operation and release delay circuit is in its idle condition (with contact pair ST-1 open), the capacitor 28 charges via the resistor 22, the transistor 12, the resistor 18 and the resistor 30, the transistor 12 becomes switched "off" and the relay A is de-energized. When a start signal is provided, the contact pair ST-1 is closed and the capacitor 28 discharges via the diode 32, the resistor 34, the normally closed contact pair A-1, the closed contact pair ST-1 and the resistor 36 to the -48 volt supply. With the contact pairs A-1 and ST-1 closed, the resistors 22 and 24 act as a voltage divider and the potential of the emitter of the transistor 12 increases with respect to the potential at the base of the transistor 12 until the transistor 12 is switched "on" and current begins to flow through the relay A.

When the current flow through the relay A becomes sufficiently large, the relay A becomes energized and the contact pair A-1 opens, preventing further discharge from the capacitor 28 via the resistor 34. The

capacitor 28 now charges via the resistor 22, the transistor 12, the resistor 18 and the resistor 30.

During this time, the contact pair ST-1 is reopened by the external circuitry. Capacitor 28 continues to charge until current flow via the transistor 12 is insufficient to maintain the relay A in its energized condition and the contact pair A-1 again becomes closed.

The capacitor 30 charges until the transistor 12 is switched off and the operation and release delay circuit 10 is again in its idle condition and is prepared to receive another start signal via the open contact pair ST-1.

A working model of the operation and release delay circuit 10 which utilized component values shown in the drawing provided a twelve to thirteen seconds operation delay time and a 25 to 28 seconds release delay time with an approximate supply potential of -50 volts.

As will be apparent to those who are skilled in the art to which the invention pertains, the operation and release delay times may be modified for particular applications by varying the electrical parameters of the components which are utilized in the operation and release delay circuit and by varying the supply voltage. In particular, modification of the resistance of the resistor 34 will vary the operation delay time and modification of the resistance of the resistor 18 will vary the release delay time. In addition, modifications of the ratio of resistances of the resistors 22 and 24 and of the capacitance of capacitor 28 will also result in changes in the operation and release delay times.

Thus, a delay circuit constructed in accordance with the present invention provides time delays of desired durations in both the operation and release cycles of a selected operable device, may be relatively inexpensively and simply fabricated in card mounted form without requiring the addition of external circuitry to provide time delays in both the operation and release cycles, automatically begins the release cycle when the device is operated and releases the device a predetermined time after it has been operated without requiring the application of an additional externally generated signal.

While the invention has been described with reference to a particular embodiment thereof, it will be appreciated by those who are skilled in the art to which the invention pertains that various modifications in form and detail may be made therein without departing from the spirit and scope of the appended claims.

What is claimed is:

1. An electrical delay circuit for delaying, for predetermined periods of time, the operation and release from operation of a device which is arranged to be operated by the application of an electrical current there-through, the delay circuit comprising:

a direct current source comprising a first and second potential wherein one of said potentials is ground, first switching means interposed between the device and said source, having operated and unoperated conditions and being effective to prevent a control signal from operating the device unless the first switching means is in its operated condition, said first switching means including a control input lead;

biasing means connected to the input lead, being effective upon the application of an electrical control signal to maintain the first switching means in its

unoperated condition for a first predetermined period of time and thereafter to permit the first switching means to change to its operated condition;

second switching means connected between the input and the control signal and being responsive to the operation of the device to disconnect the biasing means from the control signal, the biasing means being effective upon disconnection from the control signal to return the first switching means to its unoperated condition after a second predetermined period of time, and

said biasing means including resistive voltage dividing means operable to provide a third potential to the first switching means during the time said switching means remains unoperated and a control signal is applied.

2. An electrical circuit as claimed in claim 1 wherein the device comprises a relay having its operating coil connected at one end to said first potential and at the other end to the first switching means, the first switching means being arranged when it is in its operated condition to apply said second potential to the other end of the operating coil, the difference between the first and second potentials being sufficient to energize the operating coil when both of the potentials are applied to the coil.

3. An electrical circuit as claimed in claim 2 wherein the first switching means is a transistor having its collector electrode connected to one end of the operating coil and its emitter electrode connected to a source of the second potential, and

the biasing means comprising a capacitor connected to the base electrode of the transistor and being arranged to develop a potential to prevent the emitter-base bias of the transistor from being sufficient to switch the transistor on in the absence of an control signal applied to the input.

4. An electrical circuit as claimed in claim 3 wherein the second switching means comprises a normally closed contact pair of the relay which is arranged to be opened when the operating coil is energized, the contact pair being connected between the control signal and the capacitor, the biasing means further comprising resistive means connected in series with the capacitor and arranged to prevent the capacitor from developing a potential sufficient to switch the transistor into its unoperated condition until a second predetermined time after the contact pair is opened.

5. An electrical delay circuit for delaying, for predetermined periods of time, the operation and release from operation of a device which is arranged to be operated by the application of an electrical current there-through, the delay circuit comprising:

a source of direct current having a grounded terminal and an ungrounded terminal, an electromagnetic relay, and a transistor connected so that the winding of said relay and the emitter-collector path of said transistor are connected in series between said terminals of said source, said relay having at least one controlled contact and a release contact;

biasing means including a combination of a capacitor connected in series between two resistors, one end of said combination being connected to the base of said transistor and the other end being connected to said ungrounded terminal;

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a resistive voltage divider including two resistors, one end of said divider connected to said grounded terminal and the other end of said divider forming a control node, a division point of said divider being connected to the emitter of said transistor, a diode being connected to said control node and to said capacitor at the end nearest the base of said transistor and being poled to prevent charging said capacitor

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itor through said divider, and control means for providing a control signal, the control means comprising a resistor connected to said ungrounded terminal and a switching contact connected at the other end of said divider, said release contact being connected between said switching contact and said control node.

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