

United States Patent

Gueldenpfennig et al.

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[45] Dec. 5, 1972

[54] MONITOR FOR TIMING CIRCUITS

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[52] U.S. Cl. **340/167 A, 340/167 R, 340/167 B**

[51] Int. Cl. **H04q 1/32**

[58] Field of Search **340/167, 171, 167 A, 167 B;**
307/234; 328/109, 111

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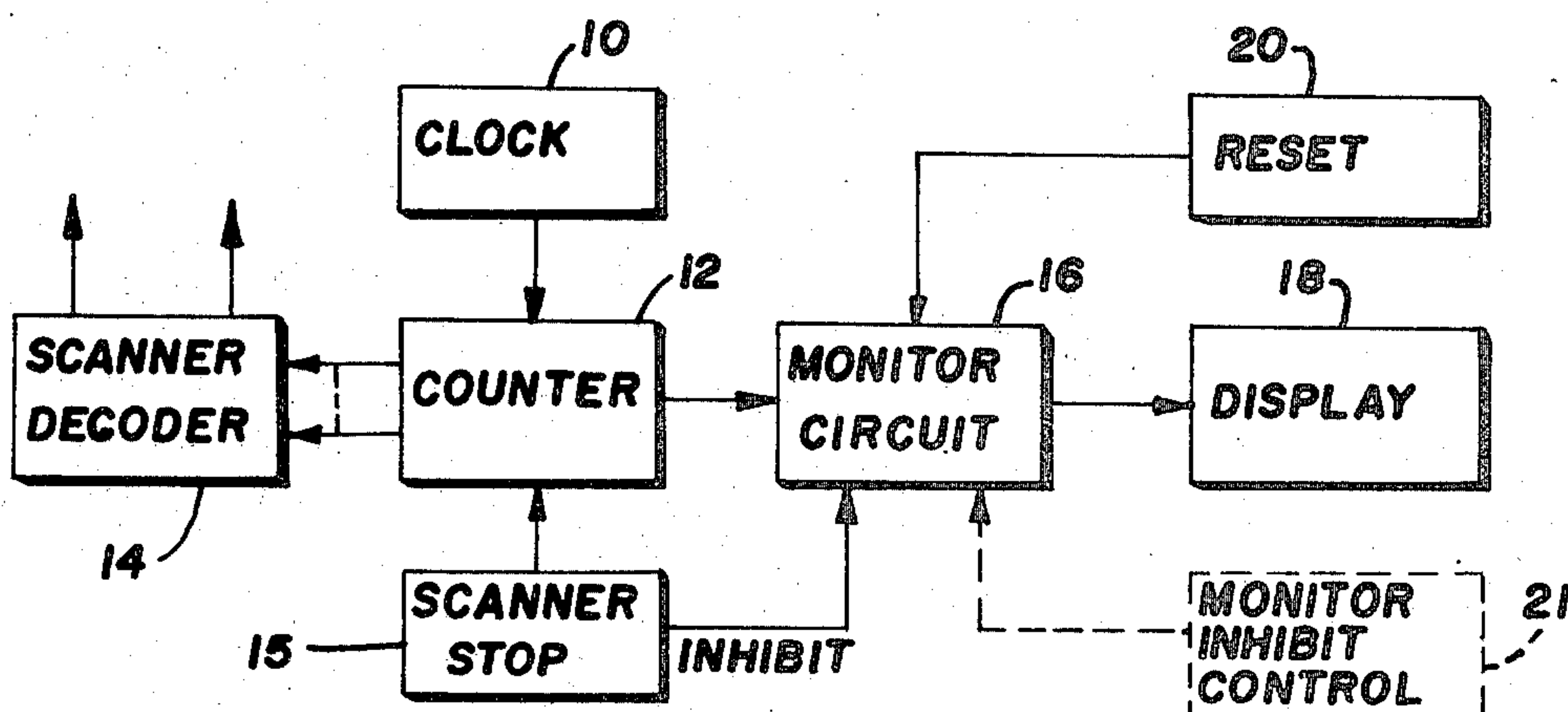
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[57] ABSTRACT

The input of a pair of gates are connected to a timing circuit, that produces periodic pulses having preset time duration and preset separation, in a manner so that the signals applied to the gates are inverted with respect to the other. One gate is inhibited from responding to the signals for a period of time greater than preset time duration and the other is inhibited for a period of time greater than the preset separation. The gates are connected to a latching circuit so that if the signal applied a gate exceeds its inhibiting period, the latching circuit produces a continuous alarm.

13 Claims, 7 Drawing Figures



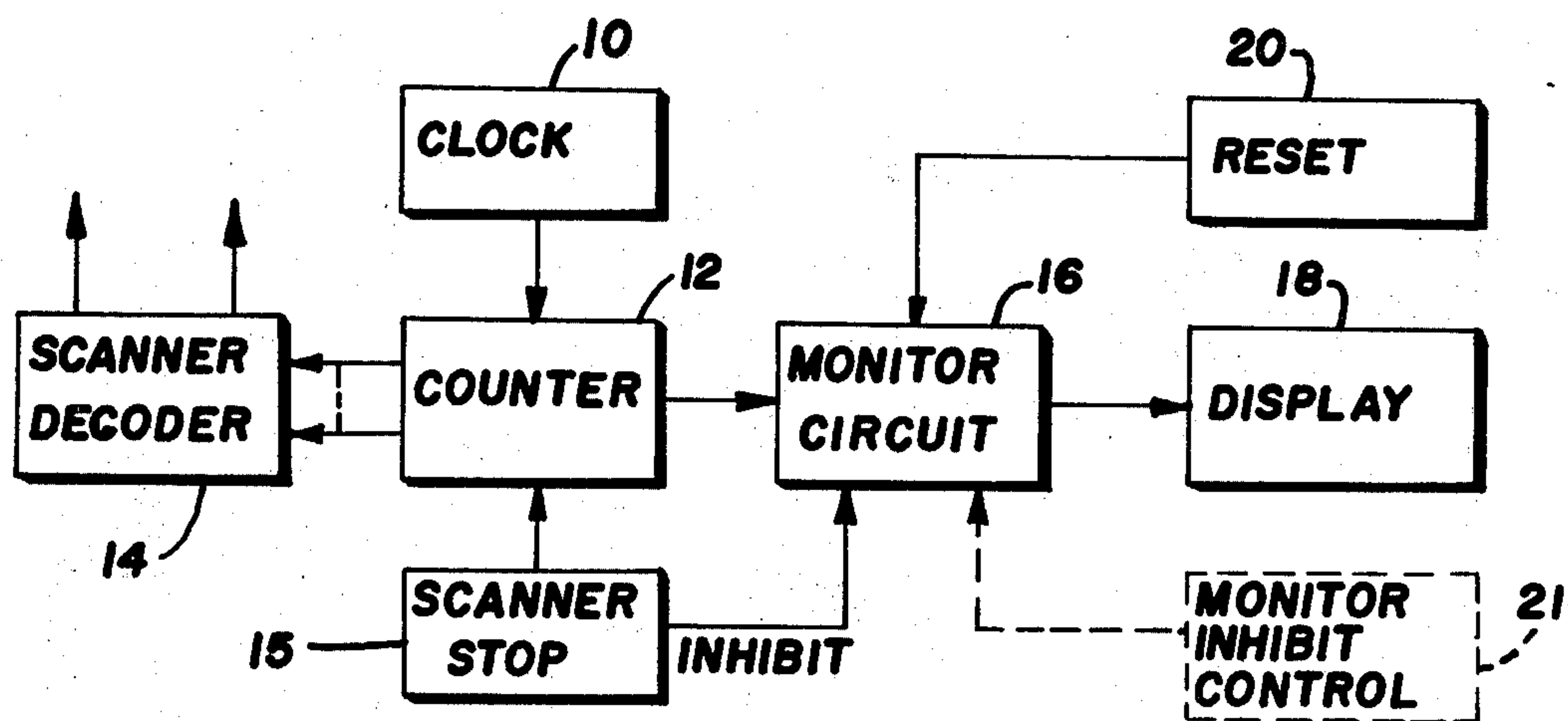


FIG. 1

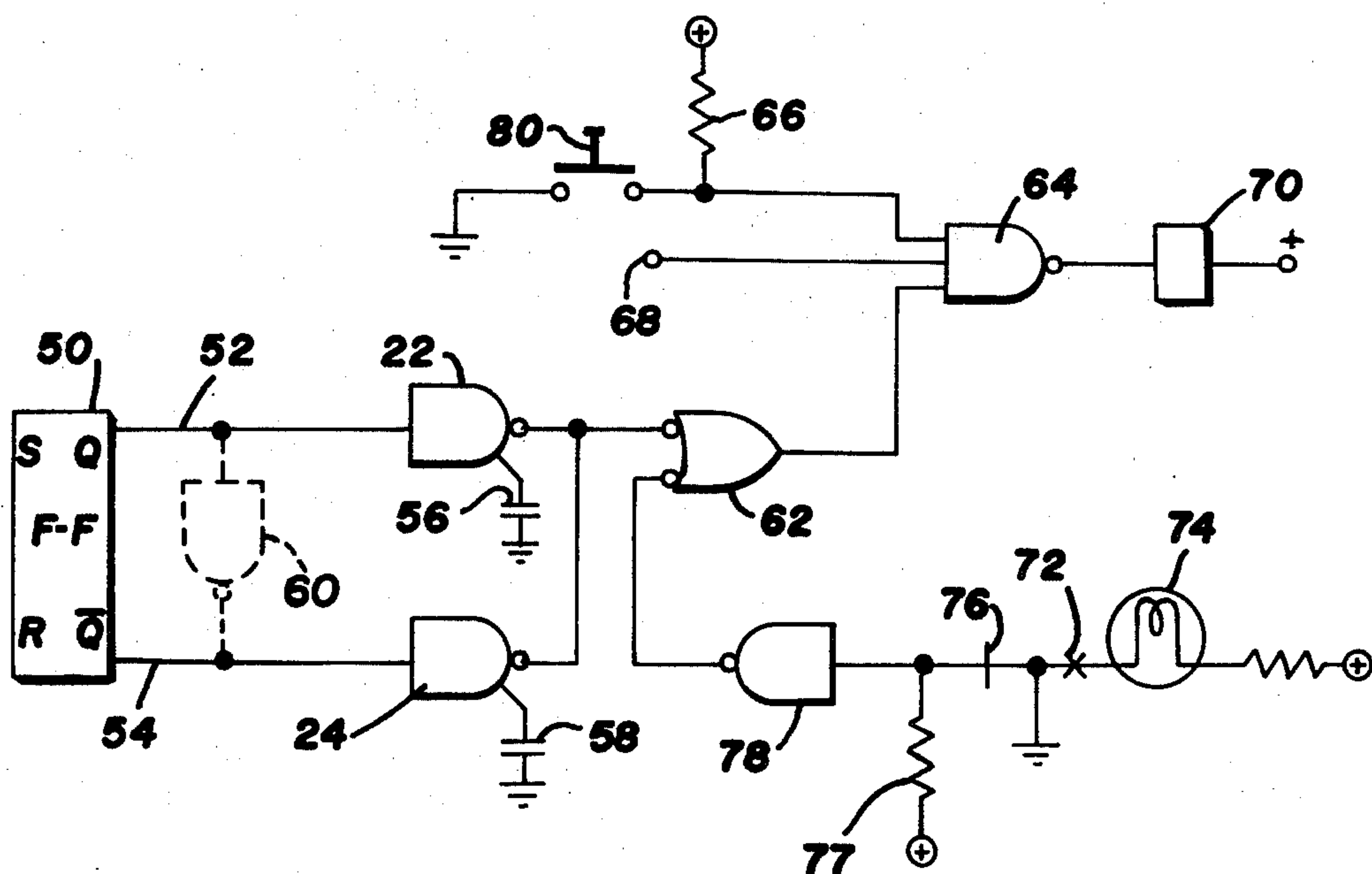


FIG. 2

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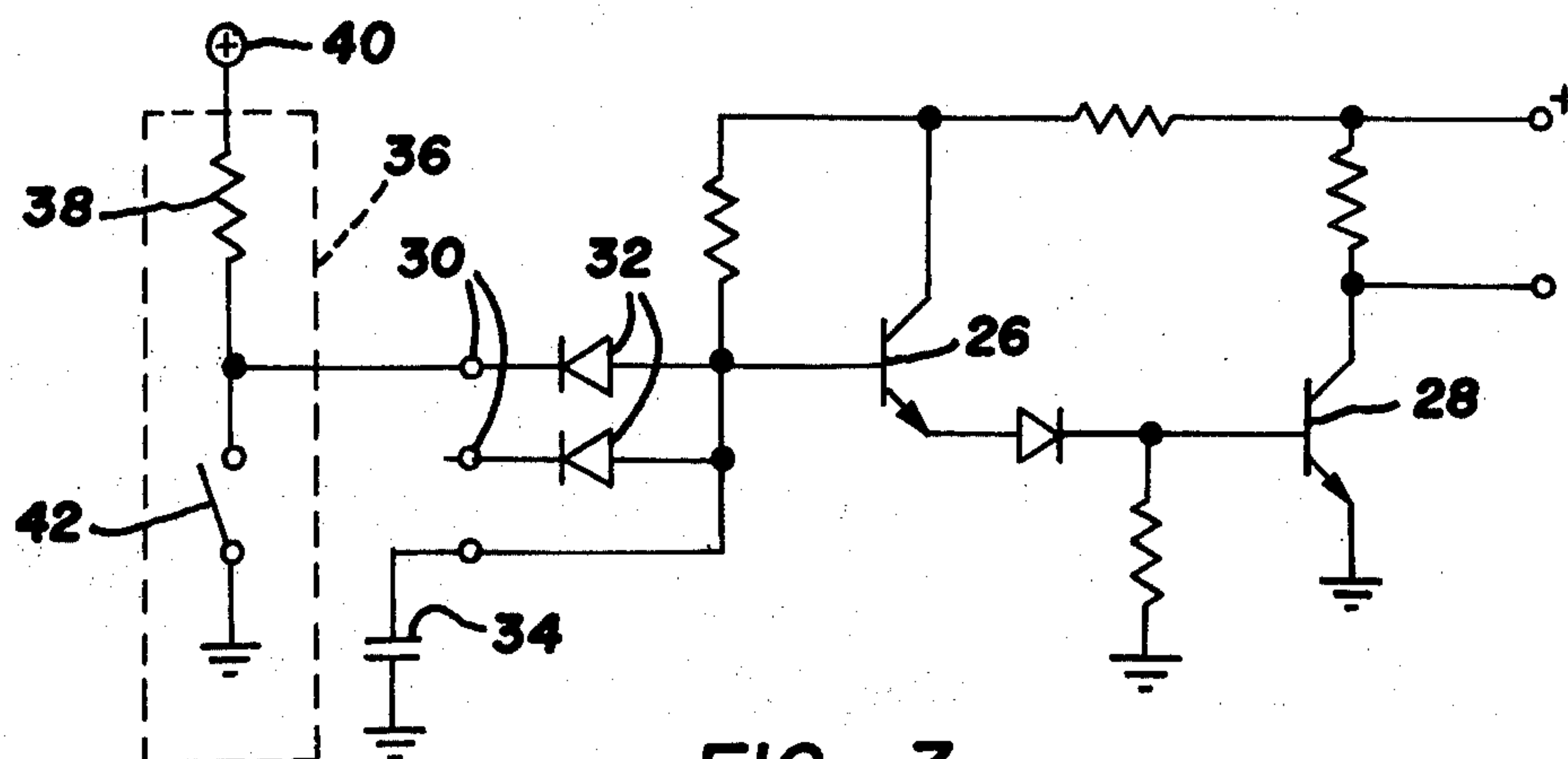


FIG. 3

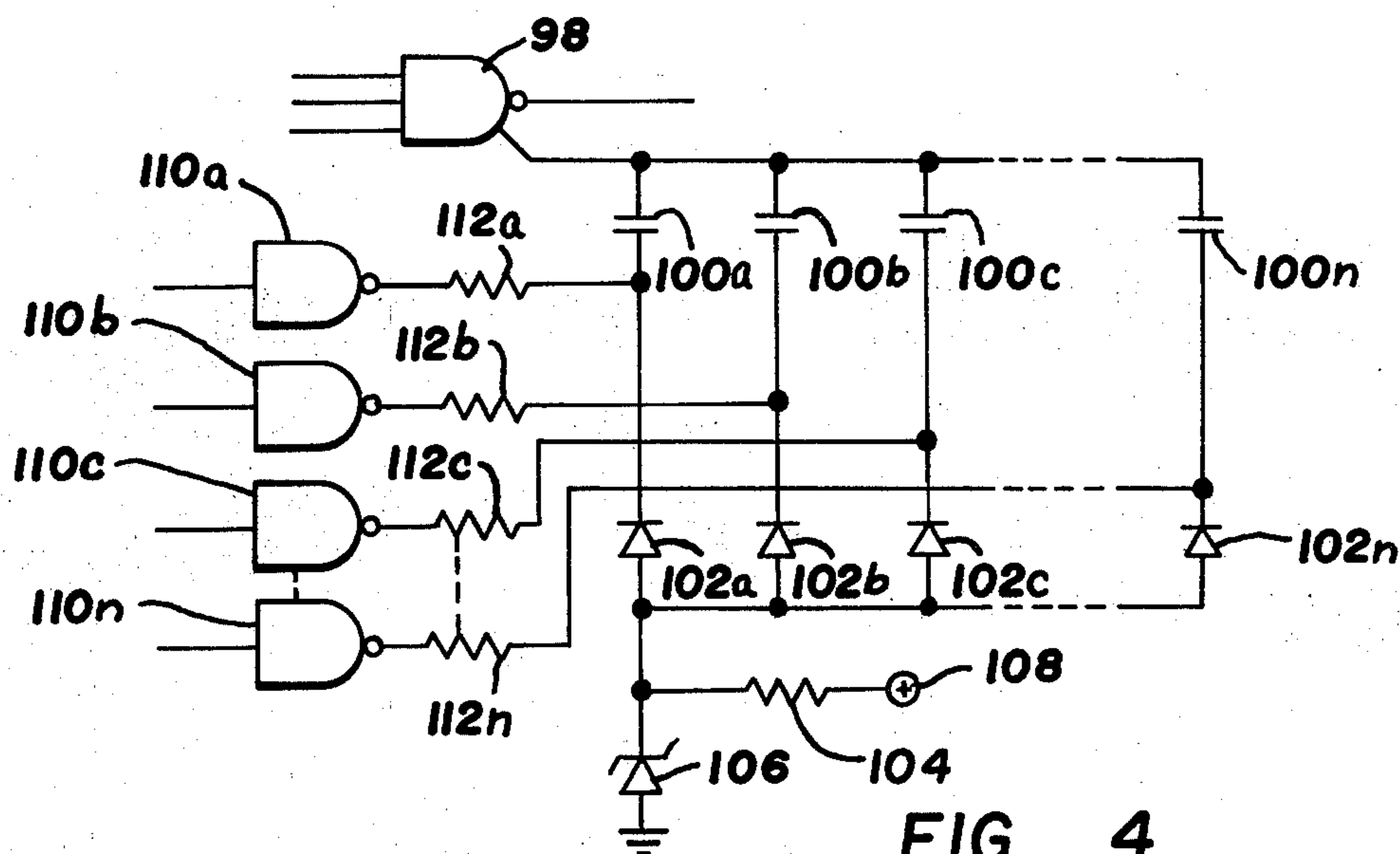


FIG. 4

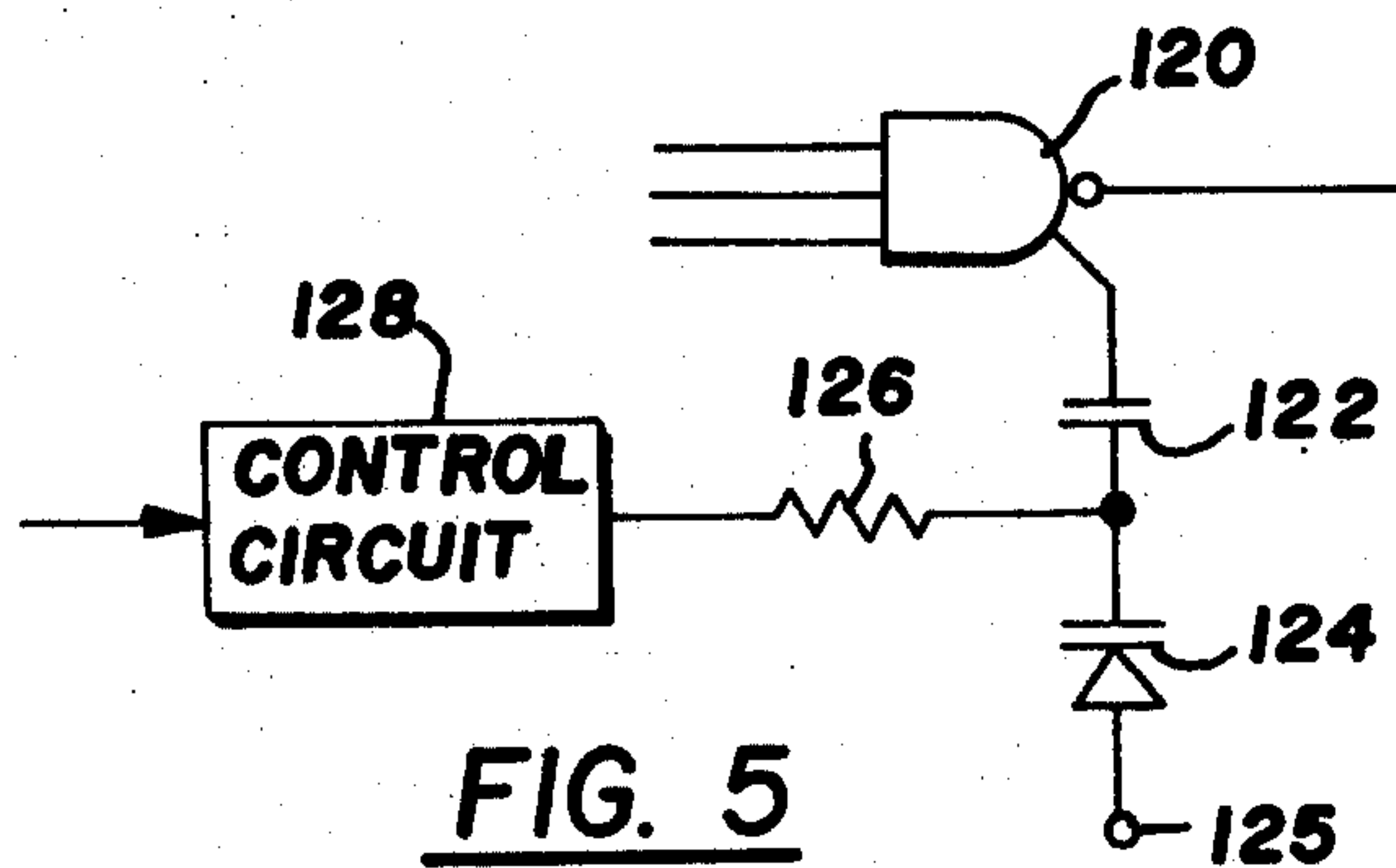
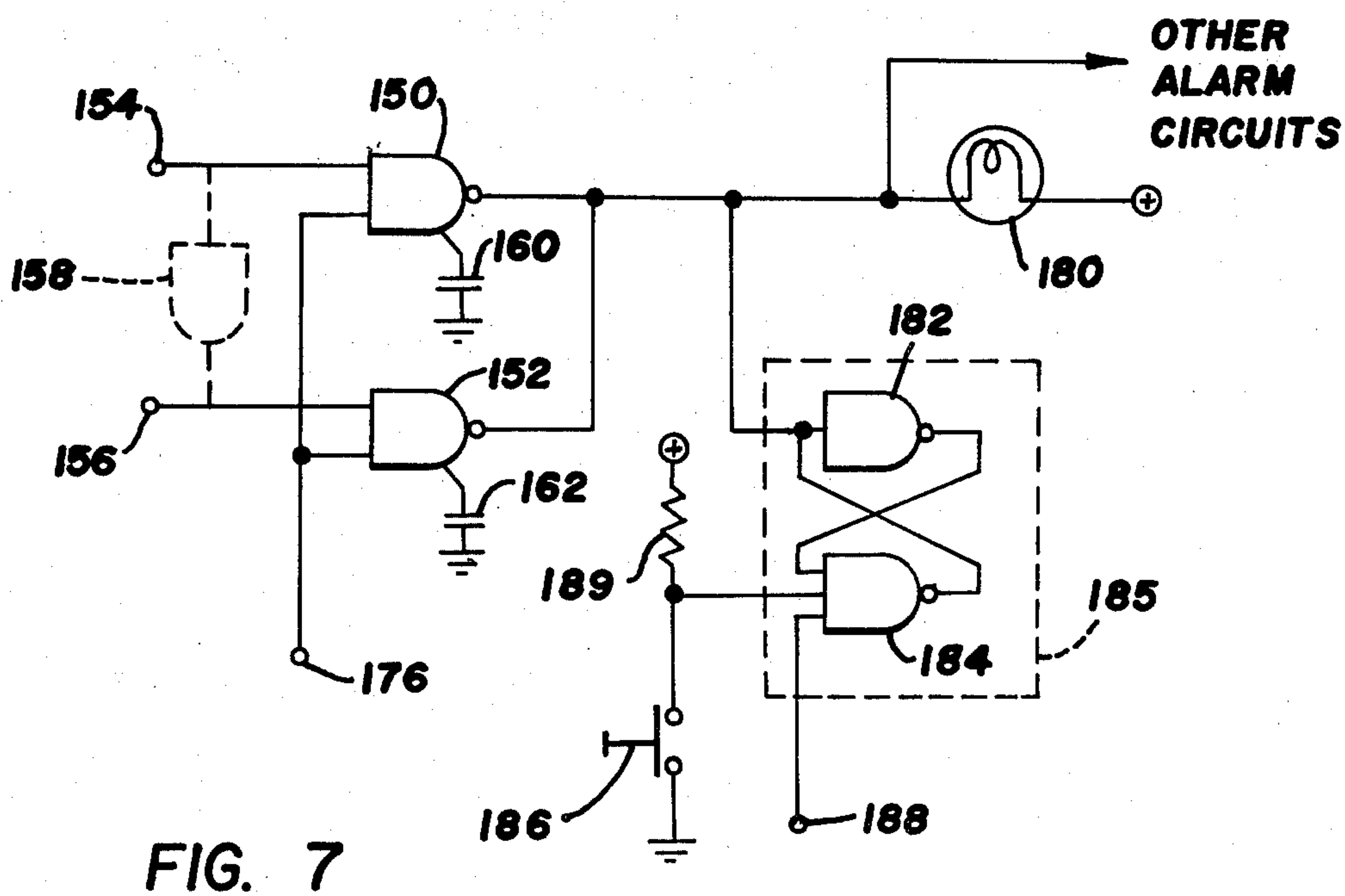
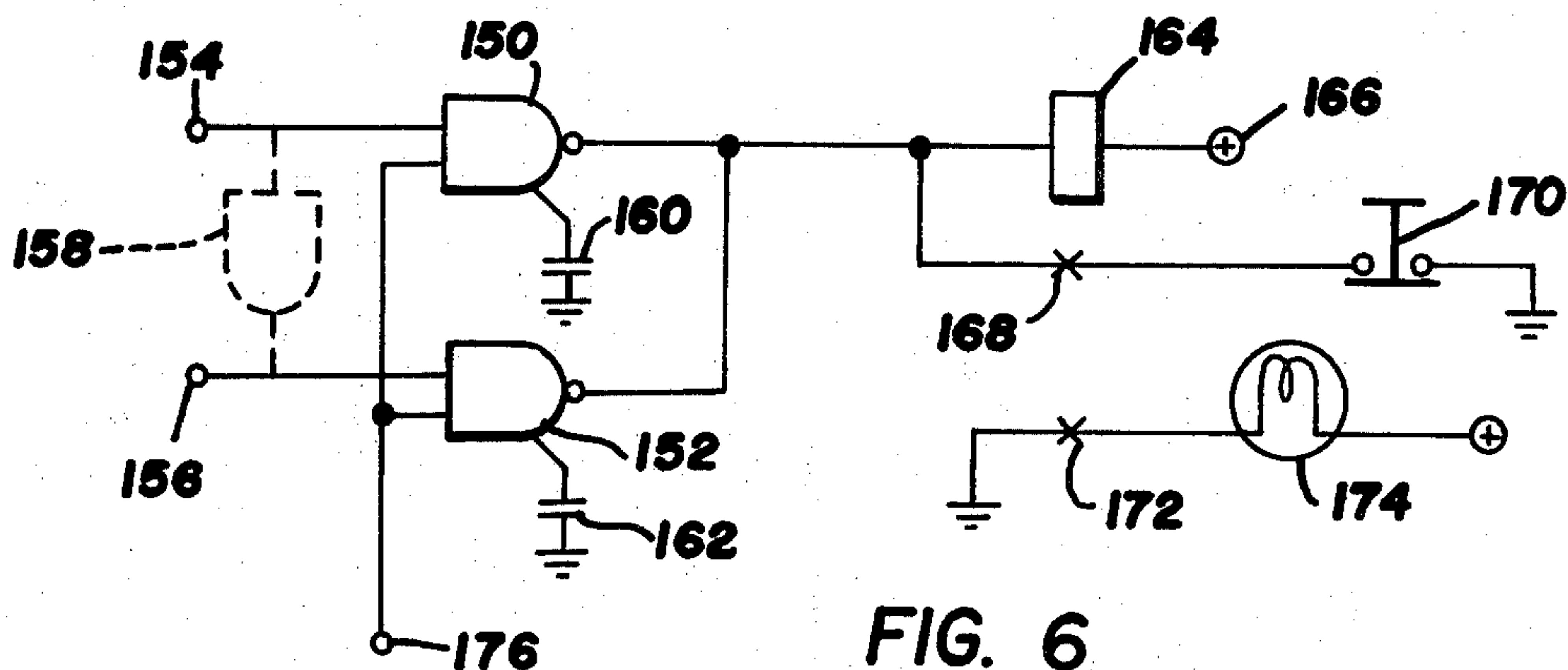


FIG. 5

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MONITOR FOR TIMING CIRCUITS

BACKGROUND OF THE INVENTION

This invention pertains to alarm circuits in general, and more particularly for circuits for monitoring the operation of timing circuits.

In various electronic systems that are clock controlled to provide proper sequential operation, such as for example, computers and telephone exchanges, it is very important to continuously monitor the operation of various timing and sequencing circuits, to detect, as easy as possible, a fault condition, and also to provide an indication as to the source of the failure. Such timing circuits may exhibit a complete failure, or an erratic failure, such as skipped pulses or as undesirable shifts in time duration.

Timing circuits, such as clock circuits, shift registers or scanners, produce square wave type pulses that alternate between high and low levels of output, or between different signal polarities. When a circuit of this type fails, it can fail in either state (high or low level) or either polarity. In order for a monitoring circuit to be effective, it must be able to detect a failure in either of the states or polarities, and provide an appropriate alarm. In many situations, it is desirable that the alarm should continue in spite of the fact that the fault condition has corrected itself, to provide an indication that a fault did occur at one time. The occurrence of the fault can be acknowledged and the alarm or monitor circuit reset by persons responsible for maintaining the system.

Monitoring circuits of this type are required to provide a wide variety of checks throughout entire systems, at various timing rates, and for various combinations of symmetrically and/or unsymmetrically timed wave forms. For example, in systems wherein a master clock provides multiple timing outputs at different timing sequences or rates, it is desirable to monitor each of the timing outputs so that a failure of one can be immediately detected. In addition, there are occasions when it is necessary for each of the stages of the shift register or ring counter to be monitored, wherein each of the stages have different switching sequences. Hence, in order to provide monitoring circuits in a large variety of locations, such monitoring circuits must be relatively inexpensive to be economically feasible. Furthermore, it is highly desirable that a single circuit design will function over a wide range of timing conditions and can monitor symmetrical and/or unsymmetrical timed wave forms, and wherein the circuit can be made to operate under these various conditions by merely changing component values in the monitoring circuit.

In many timing circuits, such as scanning circuits in telephone exchanges, the timing circuit is purposely stopped for a preset period of time so that certain functions can be performed. For example, the junctor and line scanning circuits and their timing circuits are stopped for a sufficient period of time for seizing circuits and completing connections. Once the connections are complete, the scanners are released to continue in their timing sequence. A circuit for monitoring the proper operation of such circuits is required to distinguish between an intended break in the timing sequence and a fault condition.

Timing circuits, may at times, have two or more modes of operation wherein the timing sequence changes in each mode of operation. In such case, the monitor circuit must have provisions for automatically adjusting its operation in accordance with the operating mode in which the timing circuit is functioning.

In systems wherein a very large number of timing circuits require periodic checks, it may be desirable to have a single monitor circuit that can be used to periodically scan the operation of the various timing circuits on a time divided basis. In such case, the monitor circuit must have provisions for automatically adjusting the operation of the monitor circuits in accordance with the pulse rate, pulse duration, and pulse separation of the timing circuits of the various timing circuits.

It is, therefore, an object of this invention to provide a new and improved circuit for monitoring the operation of timing circuits.

It is also an object of this invention to provide a new and improved monitoring circuit that detects a failure in a timing circuit in either state and/or polarity of failure.

It is still a further object of this invention to provide a new and improved circuit for monitoring symmetrical and/or unsymmetrical timed wave forms.

It is also an object of this invention to provide a new and improved monitoring circuit that is economically feasible for extensive use requiring only component value changes for presetting the timing of the circuit to proper operation.

It is still a further object of this invention to provide a new and improved alarm circuit for monitoring the operation of timing circuits that provides a continuous alarm condition requiring a reset from the operator.

It is also an object of this invention to provide a new and improved circuit for monitoring the operation of timing circuits that can distinguish between a controlled break in a timing sequence from a fault condition.

It is still a further object of this invention to provide a new and improved circuit for monitoring the operation of timing circuits that has more than one timing mode of operation.

It is also an object of this invention to provide a new and improved circuit for monitoring the operation of timing circuits that can sequentially monitor a large number of timing circuits having different timing sequences.

BRIEF DESCRIPTION OF THE INVENTION

A circuit for monitoring the operation of a timing circuit producing periodic pulses having preset time durations and preset spacings therebetween, includes a pair of signal translating circuits having their inputs coupled to the timing circuit so that signals applied to the input circuits are inverted with respect to each other. One signal translating circuit is inhibited from responding to an input signal for a period of time greater than the preset time durations, while the other is inhibited for a period of time greater than the time corresponding to the preset spacings. An output circuit coupled to the translating circuit produces an alarm signal when a signal applied to a translating circuit exceeds the inhibiting period.

A further feature of the invention includes the use of a latching circuit as the output circuit to provide a continuous alarm signal. Reset means are produced for resetting the latching circuit.

A still further feature of the invention includes disable means for preventing the monitor circuit from producing an alarm signal in the event the operating condition of the timing circuit is intentionally changed, such as stopped.

Another feature of the invention includes means for automatically varying the inhibit period of the translating circuits so that the circuit can monitor the operation of a timing circuit whose rate of operation is changed and/or can sequentially monitor a large number of timing circuits.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a block diagram of a scanning system including the monitor circuit of the invention.

FIG. 2 is a logic diagram of an embodiment of the monitor circuit of the invention.

FIG. 3 is a schematic diagram of an embodiment of an inhibited signal translating circuit for use in the monitor circuit of FIG. 2.

FIG. 4 is a logic diagram of a second embodiment of an inhibited signal translating circuit for use in the monitor circuit of the invention including means for automatically controlling the inhibit period of the circuit in a step-by-step manner.

FIG. 5 is a logic diagram of a third embodiment of an inhibited signal translating circuit for use in the monitor circuit of the invention including means for continuously varying the inhibit period of the circuit.

FIG. 6 is a logic diagram of another embodiment of the monitor of the invention.

FIG. 7 is a logic diagram of a further embodiment of the monitor circuit of the invention.

THE DESCRIPTION OF THE PREFERRED EMBODIMENT

The monitor circuit of the invention will be explained in conjunction with the telephone scanning system of FIG. 1. However, it is to be understood, that the monitor circuit has application in a large variety of timing systems wherein the timing circuits provide periodic pulses having preset time durations and preset spacings therebetween. A clock circuit 10 applies timing pulses to a counter circuit 12, which, for example, can include a binary counter. The binary output from the counter 12 is applied to a binary-to-decimal decoder 14 having a plurality of output circuits that are enabled in sequence, for scanning for a free junctor or a line circuit (not shown). When a free line or junctor is located, the counter circuit 12 is stopped by the scanner stop circuit 15 and is held at this count until the connections are complete. This type of scanning system is well known in the art and requires no further explanation.

Binary signals from the counter circuit 12 are also applied to the monitor circuit 16 of the invention, which monitors the operation of the counter circuit for fault condition. A fault condition can, for example, include an inoperative counter circuit, skipped counts, delayed counts, etc. In the event of a fault, the monitor circuit actuates a visual display device 18. The person-

nel assigned to the responsibility of maintaining this system, can then operate the reset circuit 20, to reset the monitor circuit to determine if the fault is still present, and if necessary, make the required corrections.

Since the telephone counter circuit 12 is stopped when a free line circuit or a junctor circuit is located, the monitor circuit 16 is disabled by a signal from the scanner stop circuit 15 so that the circuit does not produce an alarm signal. In the event that counter circuit 12 includes more than one mode of operation having different timing, a monitor inhibit control circuit 21 is used to adjust the inhibit or time out period of the monitor circuit to the mode of operation of the counter.

The monitor circuit of FIG. 2 includes a pair of signal translating circuits 22 and 24 having an inhibiting circuit for preventing the circuits from responding to input signals for a preset period of time. In the embodiment of FIG. 2, the translating circuits are illustrated as a pair of NAND gate circuits 22 and 24 having the circuit configuration illustrated in FIG. 3. However, it is to be understood that other types of circuit arrangements can also be used to provide the function of the delay or inhibited type insulating circuits. The NAND gate of FIG. 3 includes a pair of transistors 26 and 28 connected as a switching circuit. The transistor 28 is connected as an output circuit and the transistor 26 is connected to drive the transistor 28. Input signals to the gate circuit are applied through the terminals 30 and the diodes 32 to the base of the transistor 26. The arrangement is such that a threshold type circuit is present so that when a positive going pulse exceeds a preset certain level, the transistor 28 is switched into a saturated state via the transistor 26.

The response of the circuit to signals at the terminals 30 is inhibited or delayed by a capacitor 34 connected to the base of the transistor 26. A source of switching or pulse type signals (within the dashed block 36) is illustrated as including a resistor 38 connected between a positive power terminal 40 and ground through a switching circuit represented by a switch 42. The resistor 38 corresponds to the output impedance of the timing circuit to be monitored. It can be assumed that the switch 42 opens and closes at some periodic rate to switch the terminal 30 between ground and some high positive level that exceeds the threshold of the circuit, to produce signal pulses having preset time durations and preset spacing therebetween. Without the capacitor 34, the transistors 26 and 28 would immediately respond to the signals, to produce an output signal. The capacitor 34 acts as a charging circuit providing a time delay circuit. The time delay is determined by the charging path for the capacitor 34 and the circuit threshold level. The time delay circuit prevents the base of the transistor 26 from reaching the circuit threshold level for a period of time greater than the proper time duration of the pulse to be monitored, and, in effect, inhibits the response of the circuit to properly timed pulses.

A flip-flop circuit 50 is included in FIG. 2 to represent a stage of a timing circuit, such as a stage of the binary counter of the counter circuit 12. The Q and $\bar{Q}$ outputs of the flip-flop 50 are connected to the inputs of the gates 22 and 24 respectively so that the pul-

ses applied to the gates are inverted with respect to each other. The size of the capacitors 56 and 58 (corresponding to the capacitor 34 of FIG. 3) are selected so that the respective gate circuits are inhibited from responding to the input pulses for a period of time greater than the proper time duration of the pulses to be applied thereto. In the event that the flip-flop is switched from state to state for equal periods of time, the pulses on lines 52 and 54 will be of equal duration and equal spacing. In such case, the values of the capacitors 56 and 58 will be equal. In the event that the operation of the flip-flop is such that it produces unsymmetrical pulses, i.e. the pulse on and off periods are unequal, the size of the capacitors 56 and 58 are adjusted accordingly to provide the correct value of inhibiting delay. In the event only a single output signal is monitored, such as that of line 52, an inverter 60 is connected to apply inverted pulses from line 52 to the gate 24.

The arrangement is such that a failure in the timing sequence of the flip-flop 50 in either of its stable states will be detected. A failure to switch the flip-flop 50 within the designated time will apply a high level signal to one of the gates 22 and 24 via the lines 52 and 54, or in the event of a single output, via line 52 and the inverter 60, that exceeds the inhibit period of one of the gate circuits. A failure of the flip-flop in either of its stable states of operation is therefore detected. In addition, in case of a single output, a failure in the high or low level state is also detected.

The presence of the high level signal having a time duration greater than the inhibit delay at one of the gates 22 and 24 results in the transmission of an alarm signal from the gate to a NOR gate 62. In response to the alarm signal, the NOR gate applies a high level signal to an input of NAND gate 64. Under normal operation, the NAND gate 64 is partially enabled via a reset circuit including a resistor 66, and also is partially enabled by a signal on terminal 68 and, therefore, responds to the alarm signal to energize a relay 70. When the relay 70 is energized, the normally open relay contacts 72 close to energize an alarm light 74, and the normally closed relay contacts 76 open so that a high level signal from resistor 77 is applied to a NAND gate 78. The output from the NAND gate 78, in turn, applies a latching signal to the NOR gate 62 maintaining the relay 70 energized, thus providing a continuous alarm signal. The maintenance personnel will acknowledge the alarm signal by depressing a reset push button 80, which in turn, causes the NAND gate 64 to de-energize the relay 70 and reset the circuit. In the event the problem causing the alarm condition has not been corrected, the circuit will again latch into the alarm condition. When the monitor circuit of the invention is used for monitoring a scanner or a counter circuit that is purposely stopped, a disable signal is applied to the terminal 68 that prevents the NAND gate 64 from responding to the alarm signal.

FIGS. 4 and 5 include embodiments of inhibited signal translating circuits that can be substituted for the NAND gates 22 and 24 (and their respective capacitors 56 and 58) in the circuit of FIG. 2, and NAND gates 150 and 152 (and their respective capacitors 160 and 162) in the circuit of FIGS. 6 and 7.

The embodiment of the inhibited signal translating circuit of FIG. 4 includes a plural input NAND gate 98 having a variable inhibiting circuit for changing the inhibit period of the translating circuit in a step-wise fashion. The circuit of FIG. 4 includes a plurality of capacitors 100a, 100b, 100c-100n that function as the capacitor 34 of FIG. 3, when switched into operation. The capacitors 100a-100n are connected in series with the diodes 102a-102n, respectively. The other ends of the diodes 102a-102n are connected to a biasing circuit, including a resistor 104 connected in series with a zener diode 106 between a power terminal 108 and ground. The biasing circuit provides a reverse bias to the diodes 102a-102n that normally maintains the diodes in a cut-off condition and thereby open-circuiting their respective capacitors.

A plurality of NAND gates 110a-110n are connected through individual resistors 112a-112n to one end of the capacitors 100a-100n, respectively. The arrangement is such that the capacitors 100a-100n are effectively open circuited until its associated NAND gate 110a-110n is enabled. When a NAND gate is enabled, the connection between its associated capacitor and diode is grounded, thereby completing the circuit for that particular capacitor to function as the inhibiting circuit. As can be seen, the inhibit period of the circuit can be changed in a step-wise fashion by enabling individual ones of the gates 110a-110n, or enabling groups of the gates, thereby controlling the value of the capacitance connected for operation in the inhibit circuit.

The monitor circuit can function to monitor a plurality of timing circuits by receiving the input signals to be monitored at one of the input circuits of the NAND gate 98 and enabling the proper NAND gate 110a-110n to provide the corresponding inhibiting period. During the time the monitor circuit is switched from one timing circuit to another, the NAND gate 64 of FIG. 2 will be disabled for a sufficient period of time to allow the switch over to be completed.

The embodiment of the signal translating circuit of FIG. 5 includes a NAND gate 120 having a continuously variable inhibit circuit. In FIG. 5, the capacitor 34 of FIG. 3 is replaced by a combination of a capacitor 122 connected in series with a varactor 124, connected to a positive input reference potential. The varactor is a voltage variable capacitor, for example, of the type specified in the "Semiconductor Data Book," published by Motorola Semiconductor Products, Inc., Fourth Edition, June 1969, on Page AN-75 through AN-79. The junction of the capacitor 122 and the varactor 124 is coupled through a resistor 126 to a control circuit 128. The control circuit functions to provide a predetermined potential to control the capacitive value of the varactor 124. The control circuit 128 can, for example, be a gated direct current amplifier for applying controlled DC potentials in response to switching signals. The inhibit period of the circuit of FIG. 5 will depend upon the capacitance value of the series combination including the capacitor 122 and the varactor 124.

The circuits of FIGS. 4 and 5 provide a variable inhibit arrangement so that a single monitor circuit of the invention can monitor a plurality of different timing circuits on a time sharing basis and/or monitor a timing

circuit that has more than one timing mode of operation.

In the embodiment of FIGS. 6 and 7, the inhibited signal translating circuits are disabled during the period the monitor circuit is to be non-responsive to timing signals. In FIG. 6, the inhibited translating circuits comprise a pair of NAND gates 150 and 152 and their connected capacitors 160 and 162, each comprising a circuit of the type illustrated in FIG. 3. Input signals from the terminals 154 and 156 are applied to the NAND gates 150 and 152 in a manner so that the signals are inverted with respect to each other. In the event a single timing signal is monitored, the NAND gate 158 (shown in dotted lines) is connected between the input circuits of the NAND gates.

The capacitors 160 and 162 are connected to the NAND gates 150 and 152 in the same manner as the capacitor 34 of FIG. 3 to provide the inhibiting time delay. A relay 164 is connected between a positive power supply terminal 166 and the output circuits of the NAND gates 150 and 152 so that the relay is energized whenever a signal applied to one of the terminals 154 and 156 exceeds the inhibiting time period of the connected NAND gates. A contact 168 of the relay 164 is connected between ground and one end of the relay through a reset push button 170 to "latch in" the relay and thereby provide continuous alarm signal. A second relay contact 172, when closed, energizes the alarm light 174. The circuit of FIG. 6 is reset by depressing the push button 170 which open circuits the relay latching circuit. In the event the alarm signal is still present, the relay 164 will continue to be energized.

A second input of each of the NAND gates 152 and 154 is connected to a disable terminal 176, which can be, for example, one of the unconnected terminals 30 of FIG. 3. In the event the input signals to the circuit of FIG. 6 are stopped, such as in the case of the scanning system of FIG. 1, a ground or low disable signal is applied to the terminal 176 to prevent the NAND gates from responding to input signals for the duration of the disable signal.

The circuit of FIG. 7 is similar to that of FIG. 6, however, including an electronic latching circuit. In FIG. 7, the output of the NAND gates are connected to an alarm light 180 so that the light is energized whenever the signal applied to one of the NAND gates 150 and 152 exceeds its inhibiting period. The output of the NAND gates 150 and 152 are also applied to a latching circuit 185 which includes a pair of NAND gates 182 and 184 connected as a bi-stable flip-flop circuit. An alarm signal from either of the NAND gates 150 or 152 will set the latching circuit so that a continuous low or ground signal be applied to the alarm light 180 via line 187. The latching circuit is reset by depressing a reset push button 186 which removes a positive enable signal from a resistor 189 and applies ground to an input of the NAND gate 164, which resets the latching circuit, provided the alarm condition has been corrected. A third input circuit of the NAND gate 184 is connected to an input terminal 188 and can function as an alternative disable circuit for preventing the latching circuit from being set during the time the monitor circuit is to be non-responsive to input timing signals.

What is claimed is:

1. A timing and monitor circuit comprising:

timing means for producing periodic output pulses having preset time durations and preset spacings therebetween;

first and second delay circuits, the first delay circuit exhibiting a time delay greater than said preset time duration, and said second delay circuit exhibiting a time delay greater than the period of time corresponding to said preset spacings, each of said delay circuits being responsive to input signals having a time duration greater than its time delay for producing output signals; circuit means coupling said first and second time delay circuits to said timing means so that the pulses applied to said second delay circuit are inverted with respect to those applied to said first delay circuit;

a latching circuit coupled to said first and second delay circuits for producing a continuous alarm signal in response to an output signal from said delay circuits, and

circuit means for resetting said latching circuit.

2. A circuit as defined in claim 1 including:

disable means for disabling said monitor circuit from responding to timing pulses.

3. A circuit as defined in claim 1 including:

circuit means coupled to said delay circuit for adjusting said time delays.

4. A timing and monitor circuit comprising:

timing means for producing periodic pulses having preset time durations and preset spacings therebetween;

a pair of signal translating circuits;

circuit means coupling said timing means to the inputs of said translating circuits so that the signals applied to the inputs of said translating circuits are inverted with respect to each other;

circuit means coupled to one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least said preset time duration;

circuit means coupled to the other one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least a period corresponding to said preset spacings, and

circuit means coupled to the output of said pair of translating circuits for producing an alarm signal in response to an output signal from said translating circuits.

5. A circuit as defined in claim 4 wherein:

said circuit means coupled to the output of said translating circuits comprises a latching circuit for providing a continuous signal in response to an output signal from said translating circuits, and circuit means for resetting said latching circuit.

6. A circuit as defined in claim 4 wherein:

said translating circuits comprise gate circuits, and said inhibiting circuit means coupled to said translating circuits includes capacitive means providing a charging circuit for delaying the response of the gate circuits to the input signals.

7. A circuit as defined in claim 4 wherein:

said timing means provides a pair of output signals wherein one signal is the inverse of the other, and said circuit means coupling said timing means to said translating circuits couples individual ones of said

pair of output signals to separate inputs of said translating circuits.

8. A circuit as defined in claim 4 wherein:

said circuit means coupling said timing means to said translating circuit applies said periodic pulses to one of said translating circuits and inverts said periodic pulses prior to applying them to said other translating circuit.

9. A circuit for monitoring the operation of a timing circuit producing periodic pulses having preset time durations and preset spacings therebetween comprising:

a pair of signal translating circuits;

circuit means coupling the timing circuit to the inputs of said translating circuits so that the signals applied to the inputs of said translating circuits are inverted with respect to each other;

capacitive means for providing a charging circuit coupled to one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least said preset time duration;

capacitive means for providing a charging circuit coupled to the other one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least a period corresponding to said preset spacings;

circuit means for adjusting the values of said capacitive means, and

circuit means coupled to the output of said pair of translating circuits for producing an alarm signal in response to an output signal from said translating circuits.

10. A circuit as defined in claim 9 wherein:

said capacitive means includes a plurality of capaci-

tors, and

said control circuit means includes means for selecting at least one of said capacitors to control the duration of said inhibit period.

11. A circuit as defined in claim 9 wherein:

said capacitive means is electrically variable, and said control circuit means controls the value of said capacitive means.

12. A circuit as defined in claim 9 including:

a disable circuit for selectively disabling said monitor circuit from responding to the timing signals.

13. A circuit for monitoring the operation of a timing circuit producing periodic pulses having preset time durations and preset spacings therebetween comprising:

a pair of signal translating circuits;

circuit means coupling the timing circuit to the inputs of said translating circuits so that the signals applied to the inputs of said translating circuits are inverted with respect to each other;

capacitive means for providing a charging circuit coupled to one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least said preset time duration;

capacitive means for providing a charging circuit coupled to the other one of said translating circuits for inhibiting said circuit from producing an output signal in response to an input signal for at least a period corresponding to said preset spacings, and circuit means coupled to the output of said pair of translating circuits for producing a signal in response to an output signal from said translating circuits.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,705,386
DATED : December 5, 1972
INVENTOR(S) : Klaus Gueldenpfennig, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 4, line 26

"insulating" should read
---translating---

Col. 8, line 11

"circuit means" should
begin a new paragraph.

Signed and Sealed this
twenty-eight Day of October 1975

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks