Sept. 9, 1969 R. E. ANDERSON 3,466,505

RELAY INTERLOCK CIRCUIT

Filed Aug. 3, 1966

FIG. 2

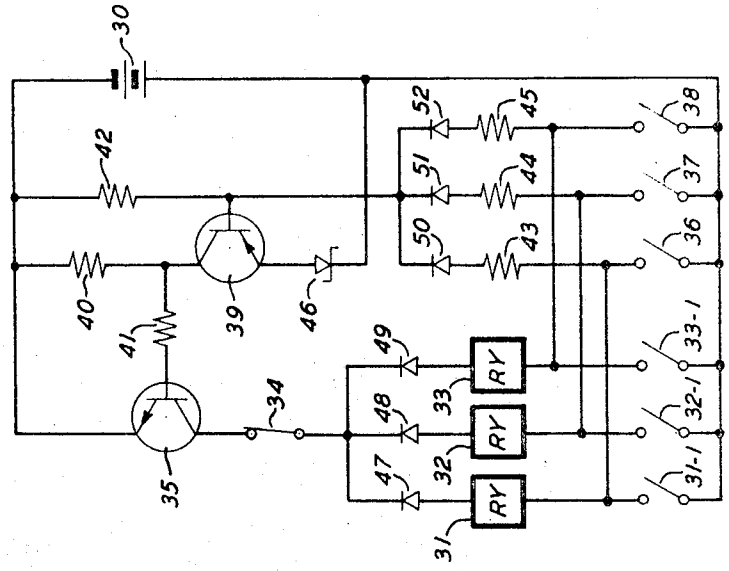
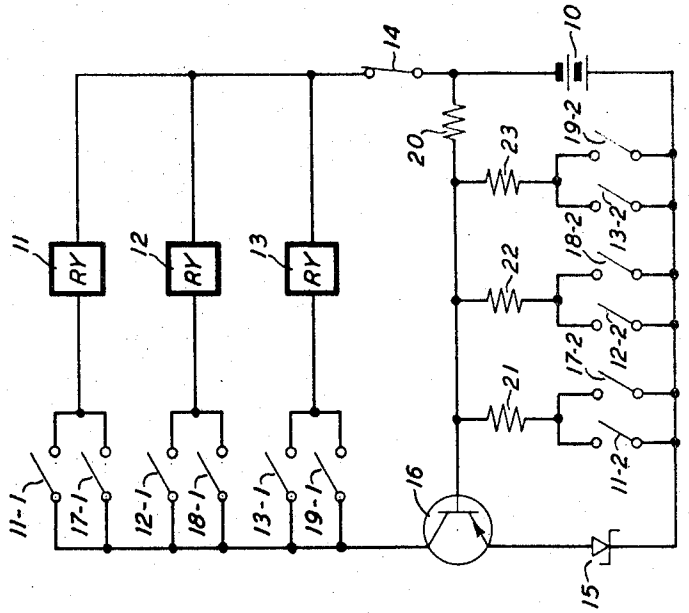


FIG. 1



INVENTOR
R. E. ANDERSON
BY R. B. Ardis
ATTORNEY

United States Patent Office 3,466,505 Patented Sept. 9, 1969

3,466,505

RELAY INTERLOCK CIRCUIT

Robert E. Anderson, North Andover, Mass., assignor to Bell Telephone Laboratories, Incorporated, Berkeley Heights, N.J., a corporation of New York

Filed Aug. 3, 1966, Ser. No. 569,983
Int. Cl. H01h 47/00, 47/32; H02b 1/24
U.S. Cl. 317—136 1 Claim

ABSTRACT OF THE DISCLOSURE

A relay interlock circuit is described in which the exclusive selection of one relay of any number of relays is accomplished with only one set of hold contacts per relay together with a common transistor relay drive circuit. The relay drive transistor is turned ON only when a single relay is selected for energization. When more than one relay is selected at any one particular time, the relay drive transistor is biased OFF thus de-energizing all relays.

This invention relates to relay interlock circuits and, more specifically, to relay interlock circuits which selectively energize from a group of relays any one relay at a time.

A relay interlock circuit is an arrangement of relays together with a power source, associated electronic components, and relay drive circuitry which provides for the specific selection of particular relays until a new relay selection is made or a de-energized command is issued. In certain relay interlock circuit applications it may, for instance, be required to energize but one relay at a time and to maintain such selected relay energized until either the previously selected relay is turned off directly or until another one of a group of relays is selected to be energized.

Although such relay interlock circuits have been devised before, they generally require a large number of relay contacts for relatively complex interlock arrangements, thereby limiting the useful extension of such interlock circuits to a limited number of relays. Further limitations are excessive power consumption for the relay drive circuitry, relatively high voltage requirements of the supply source and, in addition, the possibility of operation of more than one relay at a time during relay transfer periods.

The primary object of the invention is to provide for a relay interlock circuit that may be extended to include any number of relays.

Another object of the invention is to increase the operating efficiency of relay interlock circuits.

A further object of the invention is to assure in a relay interlock circuit the energization of not more than one relay at a time.

To fullfill these objects, the invention provides for a relay interlock circuit having the coils of its relays connected in parallel in the emitter-collector path of a relay drive transistor. Each relay has associated with it a relay selector switch to complete its power path and to control the bias on the emitter-base junction of the drive transistor. The activation of a single relay selecter switch energizes the selected relay, if no other relay is as yet energized. If, on the other hand, another relay is already energized, the subsequent activation of a relay selector switch for another relay reduces the bias on the relay drive transistor to such an extent that it is turned off, thereby de-energizing the previously energized relay. At that instant the relay drive transistor becomes again forward biased, thereby allowing the selected relay to energize. Similarly, if two relay selector switches are activated at the same time, the relay drive transistor bias is reduced to such an extent as to turn the transistor off, thereby preventing the energization of either of the two relays.

More specifically, in one embodiment of the invention the individual coils of a group of relays are connected in parallel in the emitter-collector path of a relay drive transistor. The power path for each relay is completed either through the contacts of a respective relay selector switch or through its own holding contacts which are connected in parallel with the selector switch. Although the emitter-base junction of the drive transistor is normally forward biased, the closing of respective relay selector switches or the closing of respective parallel holding contacts reduces this forward bias on the drive transistor in predetermined steps by connecting resistors in parallel with the emitter-base junction. With all the relay selector switches open, the emitter-base junction of the relay drive transistor is fully forward biased. However, none of the relays can energize since the emitter-collector path of the transistor remains open. When one of the relay selector switches becomes energized, however, the emitter-collector path of the transistor becomes completed, thereby completing the power path for the selected relay, enabling it to energize. The closing of each relay selector switch reduces, in addition, the forward bias on the emitter-base junction of the relay drive transistor. With only a single relay selector switch activated, however, the relay drive transistor remains sufficiently forward biased so that the selected relay may energize. Upon the energization of a relay, its holding contacts close, thereby bypassing the respective selector switch to maintain the selected relay energized even after the opening of the selector switch.

When the selector switches for more than one relay are activated simultaneously several respective shunt resistors are connected in parallel across the emitter-base junction of the relay drive transistor. This changes the bias condition of the transistor to such an extent as to turn it off, thereby preventing the energization of any one of the relays. Similarly, when one or more additional relays are selected while one relay is already energized, the additional shunt resistors thereby switched into the bias circuit also turn off the relay drive transistor to de-energize the relay previously energized and to prevent the energization of any relay until such time that only a single relay selector switch is activated. A previously selected relay may also be de-energized by the momentary interruption of the relay power path by means of a switch at some convenient point in the power circuit.

The present invention provides therefore for a simple and efficient interlock circuit in which only one relay can be energized at any one time, and which circuit can be extended to include any desired practical number of relays.

The above and other features of the invention will be more fully understood from the following detailed description. In the drawing:

FIG. 1 is a schematic diagram of one specific embodiment of the invention requiring two holding contacts per relay; and

FIG. 2 is a schematic diagram of another embodiment of the invention requiring only one holding contact per relay.

In FIG. 1 a relay interlock circuit is shown comprising a power source **10** supplying power to relays **11**, **12**, and **13** through switch **14**, Zener diode **15**, and relay drive transistor **16**. The power path for respective relays may be completed either through holding contacts **11–1**, **12–1**, and **13–1** of relays **11**, **12**, and **13**, respectively, or through relay selector switch contacts **17–1**, **18–1**, and **19–1** which are connected in parallel with respective relay holding contacts. Power source **10** also supplies bias power for the emitter-base junction of relay drive transistor **16**

through resistor **20**. Resistors **21**, **22**, and **23**, on the other hand, function together either with relay holding contacts **11–2**, **12–2**, **13–2**, or with relay selector switch contacts **17–2**, **18–2**, and **19–2**, respectively, to reduce the bias on the emitter-base junction of relay drive transistor **16** whenever either one of the switch contacts or one of the holding contacts is closed.

Before any one of relays **11**, **12**, or **13** has been selected to be energized, all of the relay selector switches are open and all of the relays are de-energized, so that all of the relay holding contacts are necessarily open. Relay drive transistor **16** is therefore not conducting in its emitter-collector path, even though its emitter-base junction is forward biased by power source **10** through resistor **20**. As a result the power drain on source **10** is reduced to a minimum during the standby condition of the interlock circuit.

In the interlock circuit of FIG. 1, any one particular relay may be selected to be energized by closing its corresponding relay selector switch. For instance, when it is desired to energize relay **11**, relay selector switch **17** having switch contacts **17–1** and **17–2** is closed momentarily. The closing of switch contact **17–1** completes the power path for relay **11**, thereby allowing collector current of relay drive transistor **16** to flow to energize relap **11**. Switch contact **17–2**, on the other hand, completes the connection for resistor **21** in the relay transistor biasing circuit. As soon as relay **11** energizes, its holding contacts **11–1** and **11–2** close and are connected in parallel with switch contacts **17–1** and **17–2**, respectively. As a result, holding contact **11–1** keeps relay **11** energized and holding contact **11–2** keeps resistor **21** connected in the biasing circuit even after the release of the momentary-type relay selector switch **17**. Whereas before the closing of switch contact **17–2**, the entire voltage of source **10** was applied through resistor **20** across the series combination of the emitter-base junction of transistor **16** and Zener diode **15**, after the closing of switch contact **17–2** this bias voltage is limited to the voltage appearing across resistor **21**. That is, resistors **20** and **21** now act as voltage divider network to lower the forward bias applied to the emitter-base junction of relay drive transistor **16**. After relay **11** has been energized, relay contact **11–2** performs the identical function as switch contact **17–2**, i.e., it completes the circuit for resistor **21** to maintain the lowered emitter-base forward bias on transistor **16**. As long as only one of the three bias resistors **21**, **22**, or **23** is connected in the circuit, the voltage applied to the emitter-base junction of relay drive transistor **16** is sufficient to forward bias transistor **16**, i.e., the voltage across resistor **21**, V_{R21}, is greater than the sum of the voltage drops across the emitter-base junction of transistor **16**, V_{BE16}, and Zener diode **15**, V_{Z15}, so that $V_{R21} > V_{BE16} + V_{Z15}$.

Any one of the other two relays of the circuit of FIG. 1 may be selected in a similar manner by momentarily closing its corresponding relay selector switch. If, for instance, relay **12** were to be energized, relay selector switch **18** would be closed, whereas relay selector switch **19** would be closed in order to energize relay **13**. On the other hand, any one of relays **11**, **12**, or **13** that is already energized may be de-energized by interrupting its power path by a momentary opening of normally closed switch **14**.

In the case where the relay that has been selected for energization is the first relay to be energized, that is, all of the relays are de-energized prior to the selection of this particular relay, the sequence and operation is identical to the sequence and operation described in connection with relay **11**, except that contacts **12–1** and **18–1**, and **13–1** and **19–1**, function together with resistors **22** and **23**, to energize relays **12** and **13**, respectively. On the other hand, when relay **13**, for instance, is selected to be energized while relay **11** is already energized, the following operating sequence takes place. Because relay **11** is already energized, holding contacts **11–1** and **11–2** are closed. Relay drive transistor **16** is forward biased by the voltage across resistor **21**, and transistor **16** is conducting through closed holding contact **11–1** to maintain relay **11** energized. Since it is now desired to energize relay **13** instead of relay **11**, two functions are performed in sequence; namely, relay **11** is first de-energized and then relay **13** is energized. Both of these operations are accomplished in the proper sequence by closing switch contacts **19–1** and **19–2** of relay selector switch **19**. That is, as soon as relay selector switch contact **19–2** is closed, resistor **23** is connected in parallel with resistor **21**, thereby reducing the bias voltage on the emitter-base junction of relay drive transistor **16** to such an extent as to turn off transistor **16** instantaneously. The result is fourfold and occurs in the following sequence: (1) even though relay selector switch contact **19–1** is now closed, thereby completing the power path for the coil of relay **13**, relay **13** cannot yet energize because of the off condition of transistor **16**; (2) since transistor **16** is turned off, relay **11** becomes de-energized, thereby opening its holding contacts, where the opening of holding contact **11–2** disconnects resistor **21** from the biasing network so that (3) relay drive transistor **16** again becomes forward biased and, hence, turned on, which allows (4) the energization of relay **13** through relay selector switch contact **19–1**. Once relay **13** has become energized, holding contacts **13–1** and **13–2** bypass relay selector switch contacts **19–1** and **19–2** to maintain the relay energized even after switch **19** has been opened again. Relay **13** remains energized until either switch **14** becomes momentarily opened, or until another relay is selected.

Resistors **21**, **22**, and **23** are chosen to have such resistance values that when source **10** is applied through resistor **20** across the parallel combination of any two or more of these resistors a voltage is developed across the parallel resistor combination which is smaller than the sum of the voltages across Zener diode **15** and the emitter-base junction of relay drive transistor **16**. That is, when at any one time more than two of the bias resistors **21**, **22**, and **23**, are connected in parallel in the biasing circuit, relay drive transistor **16** is immediately turned off to positively prevent the energization of more than one relay at any one time. This feature of the invention is particularly valuable in circuit applications in which it is required that never more than one relay be energized at any one time in order to prevent undesired circuit operation or damage to the equipment. The present invention further prevents the inadvertent selection of more than one relay at a time. This result is a necessary consequence of the bias network operation, since the simultaneous selection of two relays at any one time causes two bias resistors to be connected in parallel through their respective relay selector switch contacts which, in turn, reduces the bias on relay drive transistor **16** below the required forward bias level. As a result, no relay can energize as long as more than one relay selector switch is being activated at any one time. As soon, however, as only one relay selector switch remains activated, the relay corresponding to that one relay selector switch energizes.

Another specific embodiment of the invention which requires but one holding contact per relay is illustrated in FIG. 2. The interlock circuit of FIG. 2 comprises a power source **30** supplying power to relays **31**, **32**, and **33** through switch **34** and relay drive transistor **35**. Transistor **35** is of the n-p-n type and is so poled as to allow source **30** to energize respective relays either through holding contacts **31–1**, **32–1**, and **33–1** of relays **31**, **32**, and **33**, respectively, or through relay selector switches **36**, **37**, and **38** which are individually connected in parallel with respective relay holding contacts. Power source **30** also supplies power to control transistor **39**, which in turn controls the conduction of relay drive transistor **35**. Control transistor **39** is of the p-n-p type and is so poled as to supply drive current for relay drive transistor **35**.

This drive current is applied through resistor **41** to the emitter-base junction of relay drive transistor **35** to control the conduction of transistor **35** and thereby control the energization of a respective relay. The conduction of control transistor **39** is in turn controlled by a bias control network including resistors **42**, **43**, **44**, and **45** and Zener diode **46** as activated by relay selector switches **36**, **37**, **38**, and relay contacts **31–1**, **32–1**, and **33–1**. Diodes **47** through **52** serve as current blocking devices to prevent the energization of relays other than the relays selected for energization.

Before any one of relays **31**, **32**, or **33** has been selected to be energized, all of the relay selector switches **36**, **37**, and **38** are open, all of the relays are de-energized, and relay contacts **31–1**, **32–1**, and **33–1** are therefore also open. As a result bias resistors **43**, **44**, and **45** are not yet connected in a bias circuit of transistor **39**. Transistor **39** is therefore in current saturation due to the large base current supplied from power source **30** through resistor **42**. Part of the collector current of transistor **39** flows through resistor **41** and the base-emitter junction of transistor **35**, thereby forward biasing transistor **35**. Relay drive transistor **35** cannot yet conduct, however, because of its still open emitter-collector path.

In the interlock circuit of FIG. 2 any one particular relay may be selected to be energized by closing its corresponding relay selector switch. For instance, when it is desired to energize relay **31**, relay selector switch **36** must be closed momentarily. The closing of relay selector switch **36** completes the power path for relay **31** which allows collector current of relay drive transistor **35** to flow, thereby energizing the relay. As soon as relay **31** energizes, its holding contact **31–1** closes, thereby bypassing relay selector switch **36** to keep relay **31** energized even after the release of momentary type selector switch **36**.

Holding contact **31–1** and relay selector switch **36** perform, however, a dual function in this embodiment of the invention, in that they also control the bias of control transistor **39**. That is, when relay selector switch **36** and later holding contact **31–1** are closed, they also complete the connection for resistor **43** through diode **50** into the bias circuit of transistor **39**. Whereas before the closing of relay selector switch **36** the entire voltage of source **30** was applied through resistor **42** across the combination of the emitter-base junction of transistor **39** and Zener diode **46**, after the closing of switch **36** this bias voltage is limited to substantially the voltage appearing across resistor **43**. That is, resistors **42** and **43** now act as a voltage divider network to lower the forward bias applied to control transistor **39**. As long as only one of the three bias resistors **43**, **44**, or **45** is connected in the bias circuit, however, the bias voltage applied to the base of transistor **39** is sufficient to forward bias transistor **39**; that is, the voltage across resistor **43**, V_{R43}, is greater than the sum of the voltage drops across the emitter-base junction of transistor **39**, V_{BE39}, and Zener diode **46**, V_{Z46}, so that $V_{R43} > V_{BE39} + V_{Z46}$.

Any one of the other two relays of the circuit of FIG. 2 may be selected in a similar manner by momentarily closing the corresponding relay selector switch. If, for instance, relay **32** were to be energized, relay selector switch **37** would be closed, whereas relay selector switch **38** would be closed in order to energize relay **33**. A particular relay that has previously been energized may be de-energized by interrupting its power path by a momentary opening of normally closed switch **34**; either one of relays **31**, **32**, or **33** may be de-energized in this manner.

In the case where a relay that has been selected for energization is the first relay to be energized, that is, all of the relays are de-energized prior to the selection of this particular relay, the sequence and operation for any relay is identical to the sequence and operation described in connection with relay **31**, except that holding contacts **32–1** and **33–1** function together with switches **37** and **38** and resistors **44** and **45** to energize relays **32** and **33**, respectively. On the other hand, when an additional relay is being selected to be energized while one other relay is already energized, the following operating sequence takes place if it is assumed, for instance, that it is desired to energize relay **33** while relay **31** is already in an energized state. Because relay **31** is already energized, holding contact **31–1** is closed; control transistor **39** is still forward biased even though resistor **43** is connected in the bias circuit, and transistor **35** is conducting through the closed holding contact **31–1** to maintain relay **31** energized. Since it is now desired to energize relay **33** instead of relay **31**, two functions are performed in sequence; namely, relay **31** is first de-energized, and then relay **33** is energized. Both of these operations are accomplished in the proper sequence by closing relay selector switch **38**. As soon as relay selector switch **38** is closed, resistor **45** is connected in parallel with resistor **43**, thereby reducing the bias voltage on control transistor **39** to such an extent as to turn off transistor **39** instantaneously which, in turn, turns off transistor **35**. The result is fourfold and occurs in the following sequence: (1) even though relay selector switch **38** is closed, completing the power path for the coil of relay **33**, relay **33** cannot yet energize because transistor **35** is turned off; (2) since transistor **35** is turned off, relay **31** becomes de-energized, thereby opening its holding contact, where the opening of holding contact **31–1** disconnects resistor **43** from the bias network so that (3) control transistor **39** becomes again forward biased, thereby again turning on relay drive transistor **35**, which allows (4) the energization of relay **33** through relay selector switch **38**. Once relay **33** has become energized, holding contact **33–1** bypasses relay selector switch **38** to maintain the relay energized even after switch **38** has been opened again. Relay **33** remains energized until either switch **34** becomes momentarily opened or until another relay is selected.

Resistors **43**, **44**, and **45** are chosen to have such resistance values that when source **30** is applied through resistor **42** across the parallel combination of two or more of these resistors a voltage is developed across the parallel resistor combination which is smaller than the sum of the voltages across Zener diode **46** and the emitter-base junction of control transistor **39**. That is, when at any one time more than two of the bias resistors **43**, **44**, or **45** are connected in parallel in the bias circuit, control transistor **39** is immediately turned off, thereby turning off relay drive transistor **35** to positively prevent the energization of more than one relay at any one time. This feature of the invention is particularly valuable in circuit applications in which it is required that never more than one relay be energized at any one time in order to prevent undesired circuit operation or damage to the equipment.

The present invention further prevents the inadvertent selection of more than one relay at a time. This result is a necessary consequence of the bias network operation, since the simultaneous selection of two relays at any one time causes two bias resistors to be connected in parallel through their respective relay selector switch contacts which reduces the bias on control transistor **39** below the required forward bias level, thereby turning off relay drive transistor **35**. As a result, no relay can energize as long as more than one relay selector switch is being activated at any one time. As soon, however, as only one relay selector switch remains activated, the relay corresponding to that one relay selector switch energizes.

The most significant feature of the interlock circuit of FIG. 2, however, is the requirement of only one holding contact per relay, which feature facilitates the extension of the interlock circuit of the instant invention to any number of relays. The present invention provides, therefore, for a simple and efficient interlock circuit in which only one of any number of relays can be energized at any one time.

It is to be understood that the above-described arrangements are illustrative of the application of the principles of the invention. Numerous other arrangements may be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. In a relay interlock circuit comprising a plurality of relays each having an operating coil connected to at least one of its make contacts, a source of driving current having a first terminal connected to each of said one make contacts and a second terminal, a relay drive transistor having a base electrode, an emitter electrode connected to said second terminal, and a collector electrode connected to each of said operating coils to form a plurality of series paths each including said source of driving current, the emitter-collector path of said relay drive transistor, and the said operating coil and said one make contact of an individual one of said relays, a plurality of switches for selecting an individual one of said relays for activation, an individual one of said plurality of switches being connected in parallel with each individual one of said make contacts, a voltage divider network comprising a first resistor connected to said second terminal and a plurality of second resistors each connected in series with said first resistor and an individual one of said make contacts across said source of driving current, a device for developing a reference voltage connected at one end to said first terminal of said source of driving current, and control means connected to the other end of said reference voltage device, to the junction between said first and second resistors and to the base electrode of said relay drive transistor to cause conduction through said relay drive transistor when the circuit through an individual one of said plurality of said second resistors is completed and to terminate conduction through said relay drive transistor when the circuit through more than an individual one of said plurality of said second resistors is completed, a first and a second plurality of diodes for preventing current through unselected relays, an individual one of said first plurality of diodes being serially connected with each of said second resistors between said first resistor and an individual one of said make contacts, and an individual one of said second plurality of diodes being serially connected with the operating coil of each individual relay between the relay make contact and the collector electrode of said relay drive transistor.

References Cited

UNITED STATES PATENTS

3,311,795 3/1967 Gilbert ..... 317—137

LEE T. HIX, Primary Examiner

U.S. Cl. X.R.

307—115; 317—137, 148.5