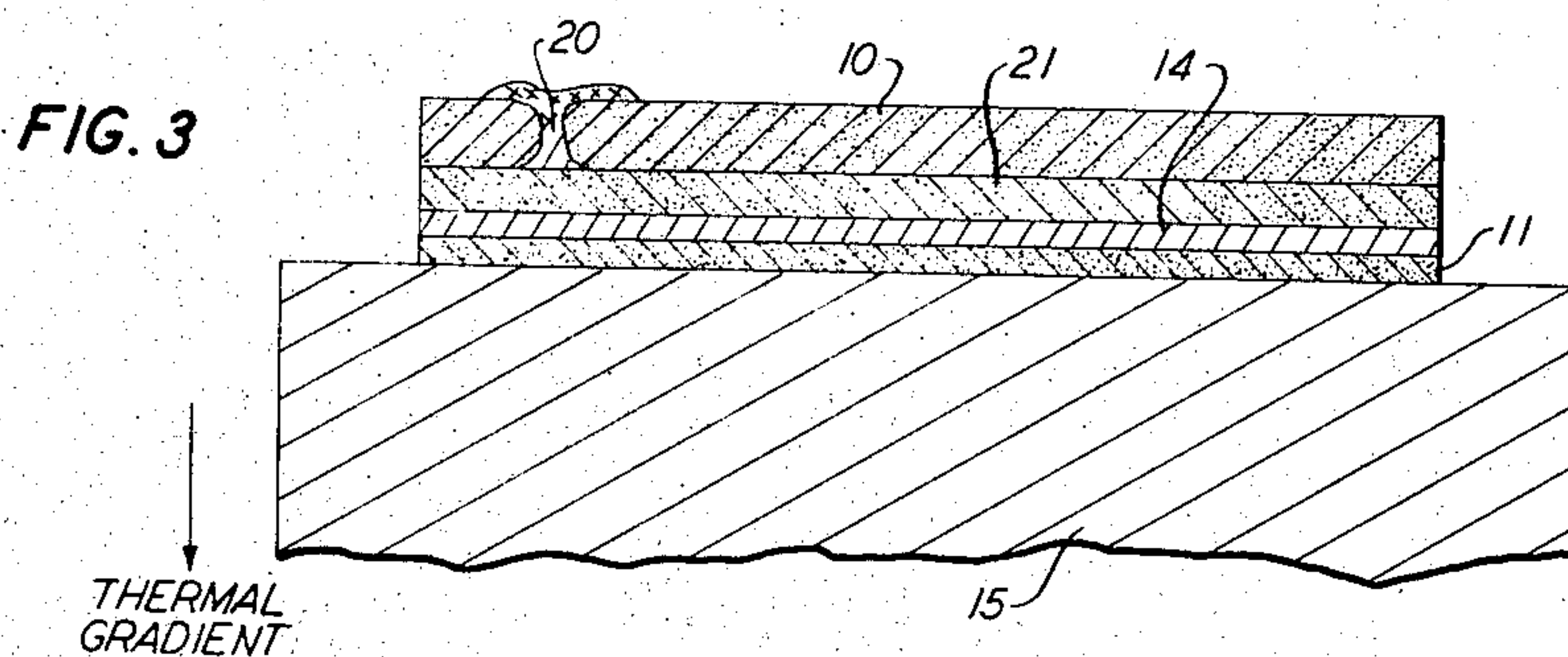
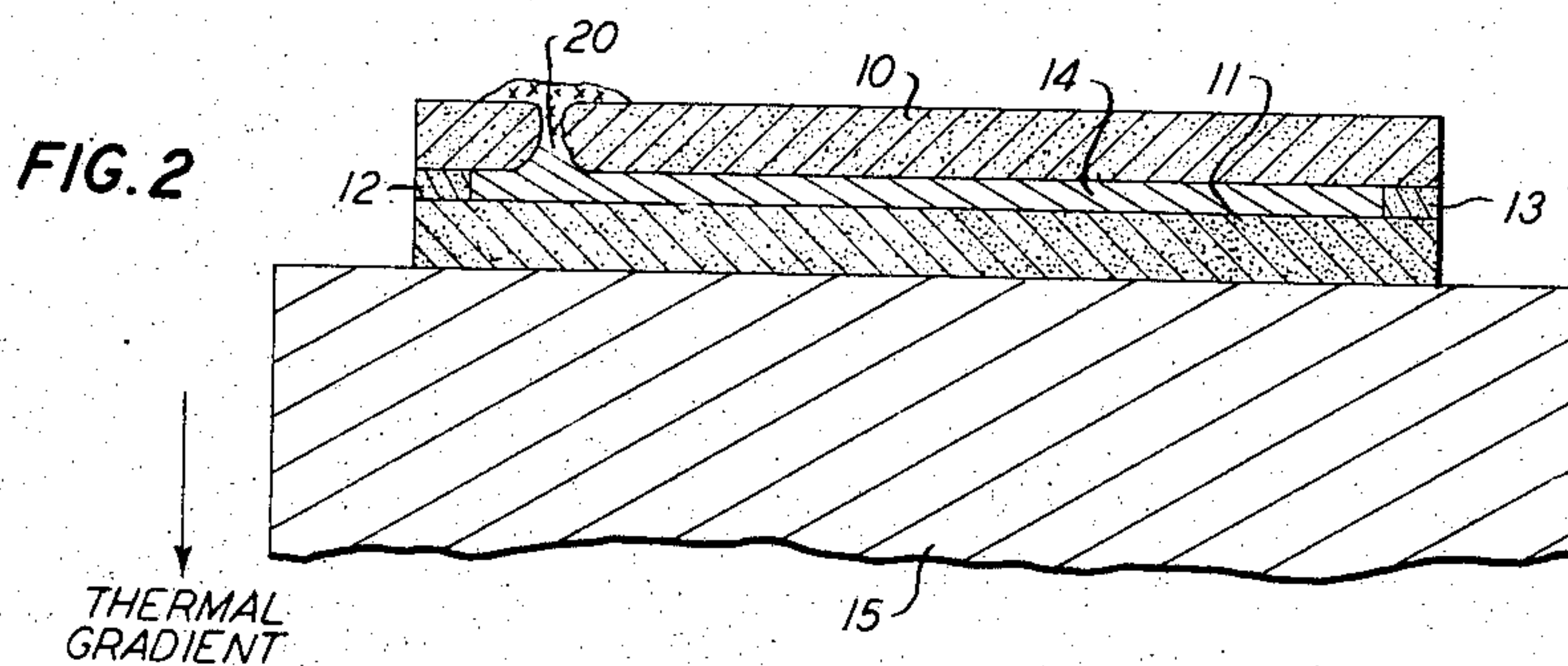
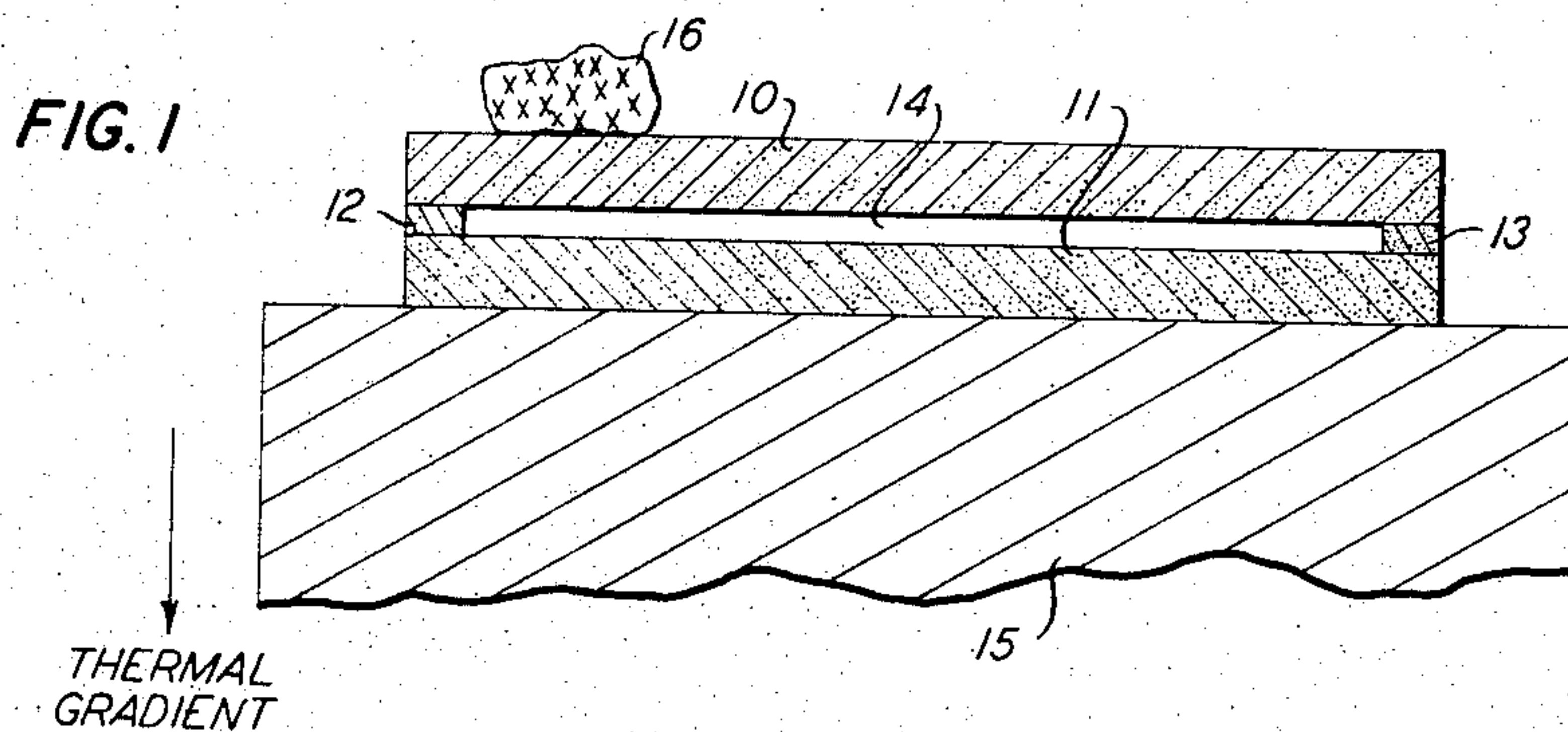


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TEMPERATURE GRADIENT ZONE MELTING AND
GROWING OF SEMICONDUCTOR MATERIAL
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TEMPERATURE GRADIENT ZONE MELTING AND GROWING OF SEMICONDUCTOR MATERIAL

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This invention relates to the growth of semiconductor crystals by a variation of the temperature gradient zone melting technique.

Growth of high purity semiconductor crystals is often achieved using the temperature gradient zone melting process described and claimed in United States Patent 2,813,048 issued Nov. 12, 1957. This process has particular advantages when applied to the regrowth of refractory materials since the solvent zone can be melted even where it may be impractical to melt the bulk material. For the purposes of this description a refractory semiconductor is considered to be one which melts at a temperature above 1800° C. Of particular interest in this category of semiconductors is silicon carbide which sublimates at 2200° C. and melts above 2700° C. At such temperatures ordinary zone melting techniques are difficult and expensive to maintain. The process is equally applicable to lower melting semiconductors particularly the III-V semiconductors such as gallium arsenide.

Temperature gradient zone melting has been applied to the growth of semiconductors with varying degrees of success. One of the principal difficulties has been the problem of obtaining effective wetting of both interfaces with the molten solvent. Added difficulty is encountered in maintaining a clean zone interface. When the solvent material is melted the impurities present characteristically collect at the surface. Then when the substrate is placed in contact with the molten solvent the substrate surface is contaminated, since it is usually the surface region of the molten material which first contacts the substrate surface.

This invention is directed to a variation in the temperature gradient zone melting technique which is particularly effective in obtaining effective wetting of the dissolving and regrowth interfaces and is capable of producing high purity crystals of exceptional uniformity and quality. It is essentially a method for introducing the solvent zone into the bulk material while maintaining a clean interface and insuring complete wetting of the growth surface.

According to the invention the solvent material, in solid form, is placed on the top surface of a sandwich comprising two flat blocks or wafers of the semiconductor being grown. The regrowth surface is a single crystal.

The two wafers are spaced apart using shims preferably composed of the material being grown. The sandwich carrying the solid solvent is heated to a temperature above the melting point of the solvent. As the solvent melts it dissolves through the upper wafer and enters the zone space. The impurities which characteristically inhabit the surface of the molten solvent are left behind and never enter the growth region. The elimination of contaminants through this technique assures proper wetting of the growth surface.

These and other aspects of the invention will perhaps be more fully appreciated in the light of the following detailed description. In the drawing:

FIG. 1 is a schematic representation of the crystal growth process at the initial stage;

FIG. 2 is a schematic representation similar to that of FIG. 1 showing the growth process at an intermediate stage; and

FIG. 3 is a representation similar to that of FIGS. 1 and 2 showing a completed crystal growth process.

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The essence of the invention is illustrated in FIGS. 1 through 3. The molten zone is introduced into the growth region by melting through a wafer of the substrate material. FIG. 1 represents the initial arrangement of the various elements necessary to the growth process. The substrate 10 is a p-type single crystal wafer of silicon carbide. The solute material 11 is a flat wafer of n-type silicon carbide which may or may not be a single crystal. The substrate wafer 10 is supported a spaced distance from the solute wafer 11 by shims 12 and 13. The shims are composed of a noncontaminating material which in this case is conveniently silicon carbide. The thickness of the zone region 14 is typically of the order of 1 to 5 mils although this parameter is not critical as long as growth can be promoted at the desired location. If the zone becomes too thick the crystal nucleates in the molten region and the single crystal habit is more difficult to obtain. There may be instances where this is desired and the spacing may be adjusted accordingly.

The wafers are supported on a noncontaminating carbon block 15 which, when heated, establishes the thermal gradient indicated by the arrow. The zone travels in a direction opposite to the heat flow. The size of the thermal gradient is not critical as long as it is adequate to maintain a manageable zone. The thermal gradient will determine the size of the molten zone and may be empirically determined according to the heat transfer properties of the material being processed and the nature of the particular apparatus being used so as to give a zone having dimensions appropriate for the purposes described here. In the specific example presented the difference between the average temperature of the substrate wafer 10 and the solute body 11 was approximately 50° C.

The solvent material is introduced into the growth region 14 in the following novel way. A solid piece of the solvent composition 16 is placed on the upper surface of the substrate wafer 10. The solvent in this case is chromium and the piece 16 is simply high purity chromium although a silicon-chromium alloy can be used. Alternative solvents are platinum and nickel.

The wafers are heated to 1500° C. in an argon atmosphere. This is a preliminary heat treatment to allow the wafer surfaces and the solvent surface to become pre-cleaned by the volatilization of adhered surface impurities. The duration is not important; fifteen minutes was found to be adequate. The SiC surfaces are not in direct contact with a solid solvent as in the case described by other investigators. (See article entitled, "Crystal Growth of GaAs from Ga by a Traveling Solvent Method," by A. I. Mlavsky and M. Weinstein, Journal of Applied Physics, vol. 34, No. 9, pp. 2885-2892, September 1963.) The fact that these surfaces are separated allows volatile contaminants to be carried off by the passing ambient prior to the introduction of the molten zone.

The temperature is then raised to about 1750° C. This temperature exceeds the melting point of the SiC-Cr eutectic which forms at ~1600° C. Referring now to FIG. 2 the chromium in contact with the silicon carbide locally attacks the silicon carbide forming a SiC-Cr eutectic and ultimately dissolves through the wafer. The chromium solvent, which dissolves silicon carbide as the hole 20 is formed, enters and fills the space 14 between the wafers. The solvent at this stage is already partially saturated with silicon carbide so that a dynamic equilibrium is established quite quickly. This reduces the tendency of the solvent to dissolve material away from the substrate wafer as may be encountered in the prior art technique where pure solvent is introduced directly into the region 14. This factor can be important where impurities in the substrate may interfere with the purpose for which the process is intended as in the case of the growth of p-n

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junctions. The volume of solvent in the piece 16 is preferably chosen to exceed the liquid volume accommodated by the space 14. If this is done, surface tension will terminate the flow of liquid alloy through the hole 20 while some of the solvent material remains behind in the hole or on the surface of the substrate wafer 10.

This method of introducing solvent into the growth region 14 has several advantages. The contaminants which form on the surface of the solvent piece 16 due to handling or oxidation and other impurities such as gaseous occlusions or less dense matter which gravitates to the surface during melting are actually left behind as the solvent flows through the hole 20 into the zone 14. This behavior is illustrated in FIGS. 1 through 3 by the small x's, which represent impurities, appearing initially distributed over the whole of the solvent body 16 in FIG. 1 but left behind as a surface "slag" in FIGS. 2 and 3. As a consequence, effective wetting of the surfaces of both the substrate wafer 10 and the solute wafer 11 is obtained. The advantages of effective wetting in promoting uniform growth are obvious. The introduction of partially saturated solvent into the growth region is advantageous also, as previously pointed out.

As the growth proceeds the liquid phase 14 advances through the solute wafer 11 with silicon carbide crystallizing on the cooler upper surface and dissolving at the hotter lower surface. The process in an advanced or completed stage is illustrated in FIG. 3. The solvent zone 14 has progressed in the direction of the thermal gradient producing the regrown crystal 21. The rate of growth is approximately 20 mils/hour. Since the solute wafer in this example is n-type the interface between the original p-type substrate 10 and the regrown crystal 21 forms a p-n junction. The quality and uniformity of the regrown material 21 is very high and the uniformity of the interface is evidence of the completeness of the initial wetting of the substrate 10 by the solvent material.

Various additional modifications and extensions of this invention will become apparent to those skilled in the art. All such variations and deviations which basically rely on the teachings through which this invention has advanced the art are properly considered within the spirit and scope of this invention.

What is claimed is:

1. A process for the growth of semiconductor crystals which comprises the steps of mounting a flat, semiconductor substrate wafer in spaced parallel relation overlying a flat semiconductor solute wafer each of said wafers comprising the semiconductor material being grown, placing a solid body of a solvent material which has a melting

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point below that of the said semiconductor material, and in which the semiconductor material has a substantial solubility on the top surface of said substrate wafer, said solid body having a volume when molten which substantially exceeds the volume of the space between the wafers, heating the wafers to a temperature above the melting point of the solvent material whereby the solvent material dissolves through the substrate wafer and flows into the space between the wafers, heating the wafers in a manner so as to establish a thermal gradient diminishing from the substrate wafer to the solute wafer which is sufficient to maintain the solvent material molten and maintaining a dynamic equilibrium for a period sufficient to recrystallize semiconductor material from the solute wafer onto the substrate wafer.

2. A process for the growth of semiconductor crystals which comprises the steps of mounting a flat semiconductor substrate wafer in spaced parallel relation overlying a flat semiconductor solute wafer each of said wafers comprising the semiconductor material being grown, the space between the said wafers being of the order of 1 to 5 mils, placing a solid body of a solvent material which together with the aforementioned semiconductor material forms a eutectic composition, said solid body having a volume when molten which substantially exceeds the volume of the space between the wafers, heating the wafers to a temperature above the melting point of the aforementioned eutectic composition whereby the solvent material dissolves through the substrate wafer and flow into the space between the wafers, heating the wafers in a manner so as to establish a thermal gradient between the substrate wafer and the solvent wafer which is sufficient to maintain the solvent material molten and maintaining a dynamic equilibrium for a period sufficient to recrystallize semiconductor material from the solute wafer onto the substrate wafer.

3. The process of claim 2 wherein the semiconductor is silicon carbide.

4. The process of claim 2 wherein the solvent material is chromium.

5. The process of claim 2 wherein the substrate wafer and the solute wafer have different conductivity types.

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HYLAND BIZOT, *Primary Examiner*.