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STORED CHARGE DIODE MATRIX SELECTION ARRANGEMENT

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FIG. 1

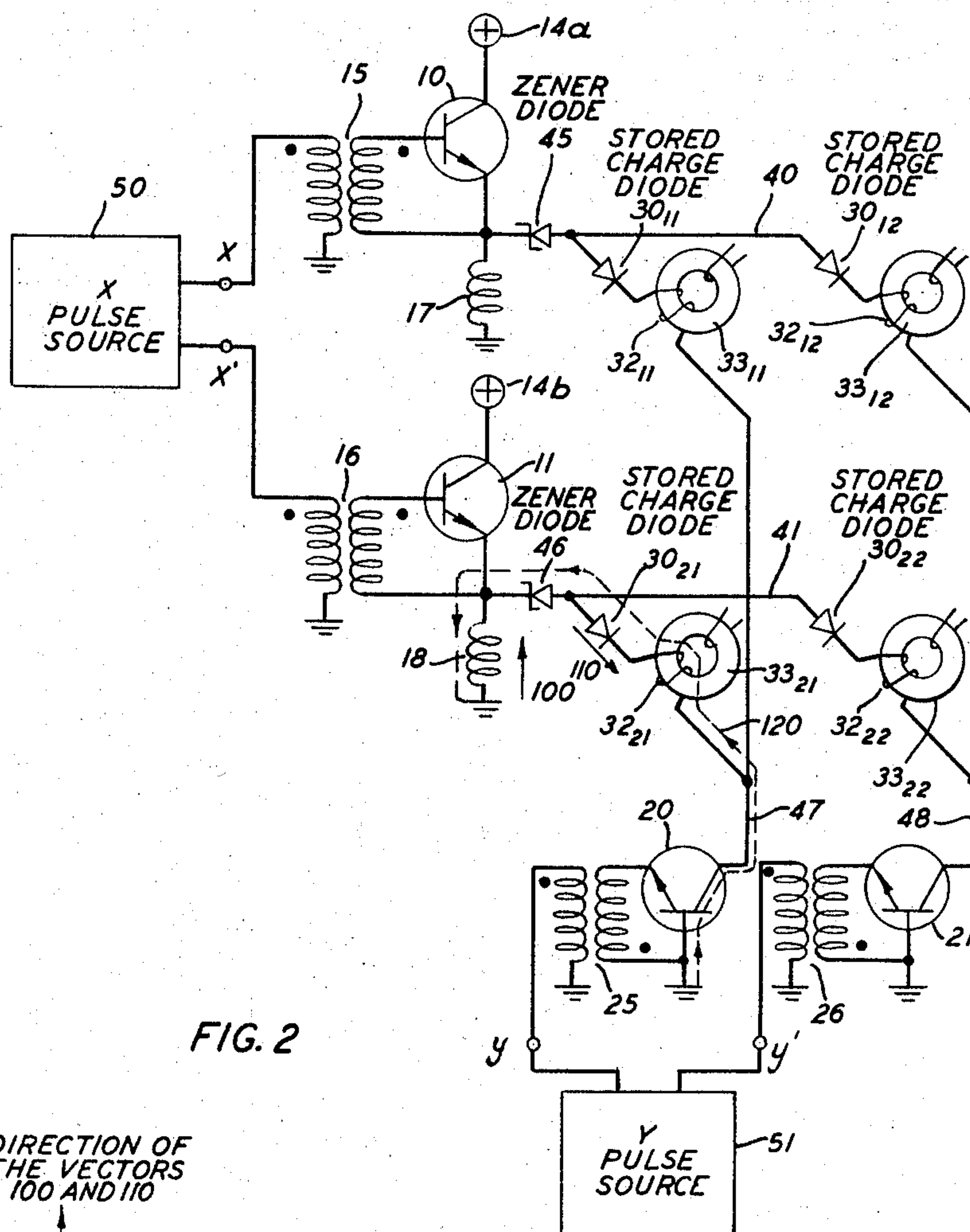
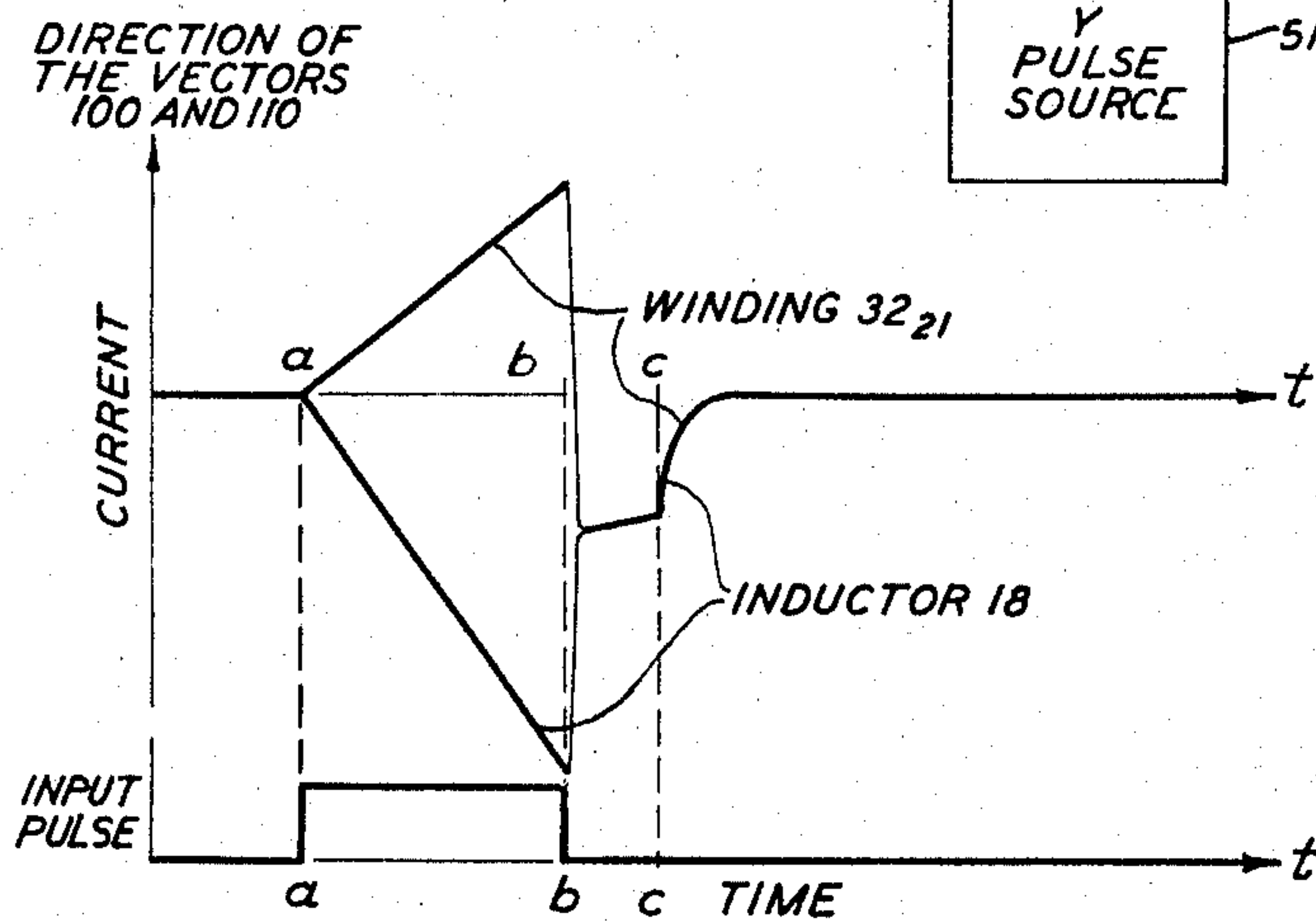


FIG. 2



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1

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STORED CHARGE DIODE MATRIX SELECTION ARRANGEMENT

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This invention relates to electronic selection circuits and, more specifically, to a matrix array for supplying a bi-polar current to a selected matrix crosspoint load.

Dual-axis matrix arrangements have been widely employed in the digital art to select a desired one of a plurality of load elements which may comprise, for example, square-loop ferromagnetic cores. One typical arrangement, which functions as a biased-core dual-axis switch, employs a plurality of magnetic cores each coupled to an output winding, a bias winding, and two selection windings respectively included in two selection axes.

When one winding in each selection axis is energized, the appropriate core coupled to both of the activated windings reverses its maximum remanent state in response thereto, thereby inducing a signal in the output winding coupled to the core. As the selection windings are de-energized, the selected core is reset to its original magnetic condition under the action of the bias winding, which supplies a magnetizing force to the core in a polarity opposite to that of the selection windings.

A similar type of circuit functioning occurs where the cores included in the above-described arrangement are employed to store binary information. Each of the binary characters may be represented, for example, by one of the two distinct maximum remanent hysteresis polarities, and one binary digit may be stored for each element employed. However, in all such prior art arrangements, a bias or reset winding is required to supply a magnetizing force to each magnetic element in a direction opposite to the flux established by the energized selection windings.

It is therefore an object of the present invention to provide an improved selection arrangement.

More specifically, an object of the present invention is the provision of a matrix selection circuit which supplies a bi-polar current signal to a selected matrix cross-point load.

Another object of the present invention is the provision of a matrix selection arrangement which may be operated at a relatively high repetition rate, and which may advantageously supply current pulses of a relatively short time duration.

A further object of the present invention is the provision of a matrix selection arrangement which is highly reliable, and relatively simple and inexpensively constructed.

These and other objects of the present invention are realized in a specific, illustrative matrix selection arrangement which supplies a bi-polar current signal to a selected one of a plurality of matrix cross-points. Each of the matrix cross-points comprises a stored charge diode serially connected to a winding which is coupled to at least one square-loop ferromagnetic storage element. The stored charge diode is characterized by a low impedance in its forward conduction direction, and by the capacity to conduct a current in its back-biased, high-impedance direction for a limited period of time.

A so-called Zener or reverse breakdown diode connects each conductor included in one selection axis to a different one of a first group of current switching transistors. Each conductor included in the other axis is connected to the collector of a different grounded-base trans-

2

istor included in a second group of transistor switches.

When an input signal is supplied to one transistor from each group, each ferromagnetic element included at the selected cross-point is driven to a like maximum remanent condition. When the input drive is removed, the circuit current reverses direction through the stored charge diode and its associated winding, thereby resetting each selected magnetic element to its original magnetic condition.

It is thus a feature of the present invention that a dual-axis matrix selection arrangement include a first and second plurality of selection conductors, a plurality of stored charge diodes respectively connecting each of the first with each of the second selection conductors, and a plurality of reverse breakdown diodes each serially connected to a different conductor included in the first selection axis.

It is another feature of the present invention that a matrix selection arrangement include a current switch which selectively conducts current in each of two directions comprising a grounded base transistor and circuitry connected to the collector of the transistor for supplying thereto a voltage which is both positive and negative in value.

It is still another feature of the present invention that a matrix selection arrangement include a first and second plurality of selection conductors, a plurality of stored charge diodes respectively connecting each of the first with each of the second selection conductors, a plurality of reverse breakdown diodes each serially connected to a different one of the first selection windings, and a plurality of current switches each connected to a different one of the first selection conductors, each switch including a transistor and an inductor connected to the emitter terminal thereof.

A complete understanding of the present invention and of the above and other features, advantages and variations thereof may be gained from a consideration of the following detailed description of an illustrative embodiment thereof presented hereinbelow in conjunction with the accompanying drawing, in which:

FIG. 1 is a diagram of a specific, illustrative matrix selection arrangement which embodies the principles of the present invention; and

FIG. 2 is a timing diagram illustrating the wave shapes of the currents which flow through selected circuit elements illustrated in FIG. 1.

Referring now to FIG. 1, there is shown a two-by-two selection matrix employing two horizontal selection conductors 40 and 41 each connected by a Zener diode 45 or 46, respectively, to the emitter of a transistor 10 or 11. Two inductors 17 and 18 connect the emitter terminals of the transistors 10 and 11, respectively, to a common ground terminal, and two transformers 15 and 16 couple the base-emitter circuits of the transistors to the x and x' output terminals of an X voltage pulse source 50. The collector terminals of the transistors 10 and 11 are connected to positive direct-current voltage sources 14a and 14b, respectively.

The selection matrix also includes two vertical selection conductors 47 and 48 each connected to the collector terminal of a grounded-base transistor 20 or 21, respectively. The base-emitter junction of the transistor 20 is coupled by a transformer 25 to the y output terminal of a Y pulse source 51. Similarly, a transformer 26 couples the y' output terminal of the source 51 to the base-emitter circuit of the grounded-base transistor 21. It is noted that the energization signals respectively supplied by the sources 50 and 51 are constrained to occur in time coincidence.

The two horizontal selection conductors 40 and 41, and the two vertical selection conductors 47 and 48 are

3

arranged to have four intersections, or cross-points. Each of the matrix intersections includes a cross-point load which connects one of the horizontal with one of the vertical selection conductors. The load comprises a stored charge diode 30 serially connected to a winding 32 which is coupled to at least one square-loop ferromagnetic core 33. As described above, the stored charge diode is characterized by a low impedance in its forward conduction direction and by the capacity to conduct a current in its back-biased, normally high impedance direction for a limited period of time. Stored charge diodes are well known in the art and are described, for example, in an article entitled, "P-N Junction Charge-Storage Diodes," by J. L. Moll et al. appearing on pages 43-53 of the January 1962 issue of the Proceedings of the I.R.E.

The elements included in each of the cross-point embodiments are further denoted with two subscripts which, in order, identify the row and column where the corresponding element may be found. For example, the numeral 30₂₁ denotes the stored charge diode 30 which is included in the second row and the first column of the selection matrix. It is noted at this point that the number of cores included in each cross-point, and also the nature and number of any additional windings coupled thereto, is dependent upon the desired functioning of the cores. For example, if it is desired that the FIG. 1 arrangement function as an access switch of the type described hereinabove, each cross-point would include only one ferromagnetic core, with one output winding coupled thereto. It is also noted that no reset winding need be coupled to each core as the corresponding winding 32 coupled thereto will perform the reset operation.

With the above organization in mind, an illustrative sequence of circuit operation for the FIG. 1 selection arrangement will now be described. Assume, for example, that it is desired to supply a bi-polar current to the winding 32₂₁ to initially switch the maximum remanent state of the ferromagnetic core 33₂₁ coupled thereto, and then reset the core. To select this cross-point load included in the second row and first column of the matrix, the pulse source 50 supplies a voltage pulse to the output terminal x' and, coincident therewith, the source 51 supplies a pulse to the output terminal y. The lower graph included in FIG. 2 shows an input pulse with its leading edge occurring at time a, which pulse represents the energization signal supplied by each of the sources 50 and 51.

The pulse supplied to the output terminal x' is coupled by the transformer 16 to the base terminal of the switching transistor 11. In response thereto, the transistor 11 is driven into a saturated condition, and as a result approximately the full voltage of the source 14b appears at the emitter terminal of the transistor. Similarly, the pulse supplied by the source 51 saturates the transistor 20, and effectively imposes ground potential on the conductor 47 through conventional transistor action. As the transistors 10 and 21 are not energized under these conditions, neither of the selection conductors 40 and 48 is at this time included in any complete, series-conduction path.

The positive step of voltage appearing at the emitter of the transistor 11 subsequent to time a generates a ramp of current flowing through the inductor 18 in a direction opposite to the vector 100 shown alongside the inductor 18 in FIG. 1. The waveshape of this current is shown in the appropriate curve of the upper diagram of FIG. 2.

Examine now the current flowing through the diode 30₂₁ and the series-connected winding 32₂₁, which winding may be considered to be in effect an inductor. The voltage impressed across the winding 32₂₁ is effectively the voltage of the source 14b less the breakdown voltage of the Zener diode 46 which is at this time conducting, and also minus the small, negligible conduction drop of the stored charge diode 30₂₁ and the series circuit resistance losses. This voltage, which is thus less than the voltage impressed across the inductor 18 by approximately the value of the Zener diode breakdown potential, gen-

4

erates a linear, monotonically increasing ramp of current which flows through the winding 32₂₁ in the direction of the vector 110, as shown in the upper diagram in FIG. 2.

At the time b, shown in FIG. 2, the voltage pulse supplied by each of the pulse sources 50 and 51 terminates, and each of the transistors 11 and 20 becomes an essentially infinite impedance with respect to conduction through the collector-emitter circuit thereof. Examining the transistor 20, however, note that if the collector terminal thereof has a negative potential applied thereto, the transistor will present a low impedance path from ground to the conductor 47 through the base-collector junction which will, under these conditions, be equivalent to a forward-biased rectifying diode. As will become apparent from the following discussion, a negative potential is in fact present at the collector of the transistor 20 for an interval following time b in FIG. 2.

Upon the termination of the input pulses at time b, there is formed a complete, counter-clocking series-conduction path, shown by the dashed line 120 in FIG. 1. This path includes the inductor 18, the base-collector junction of the transistor 20, the winding 32₂₁, the stored charge diode 30₂₁, which as noted above will conduct for a limited period of time in the reverse direction, and the Zener diode 46. Writing the differential equation for this series path in the counter-clockwise polarity, which is the forward conduction direction for the Zener diode, we have:

$$L_1 \frac{di(t)}{dt} + Ri(t) + L_2 \frac{di(t)}{dt} = 1 \quad (1)$$

where L_1 is the inductance of the inductor 18, L_2 is the effective inductance of the winding 32₂₁ coupled to the core 33₂₁, R is the series resistance of the included portions of the conductors 41 and 47, along with the resistance of the diode elements 46 and 30₂₁, and the current $i(t)$ is the transient current flowing through the above-defined series path. Taking the Laplace transform of the above equation, and transforming to the complex s-plane:

$$L_1(sI(s) - I(o)_1) + RI(s) + L_2(sI(s) - I(o)_2) = 0 \quad (2)$$

where $I(s)$ is the transform of the current $i(t)$, and $I(o)_1$ and $I(o)_2$ are the initial currents flowing through the elements 18 and 32₂₁, respectively, in the counter-clockwise direction shortly after the pulses supplied to the current switching transistors 11 and 20 are terminated. Factoring Equation 2 results in:

$$I(s)(s(L_1 + L_2) + R) = L_1 I(o)_1 + L_2 I(o)_2 \quad (3)$$

which may be rewritten

$$I(s) = \frac{L_1 I(o)_1 + L_2 I(o)_2}{L_1 + L_2} \cdot \frac{1}{s + \frac{R}{L_1 + L_2}} \quad (4)$$

Taking the inverse Laplace transform to return to the time domain, we find that the current $i(t)$ flowing through the above-described series circuit is

$$i(t) = \left(\frac{L_1 I(o)_1 + L_2 I(o)_2}{L_1 + L_2} \right) \cdot e^{-\frac{R}{L_1 + L_2} t} \quad (5)$$

In other words, the current flowing through the series circuit including the inductor 18 and the winding 32₂₁ has the form of a decaying exponential with an initial value of

$$\frac{L_1 I(o)_1 + L_2 I(o)_2}{L_1 + L_2} \quad (6)$$

It has been experimentally determined that the initial current value at the time b is relatively accurately predicted by employing for $I(o)_1$ and $I(o)_2$, respectively, in Equations 5 and 6 the maximum values of the current ramps which flow in the counter-clockwise direction through the inductor 18 and the winding 32₂₁ at the time b shown in FIG. 2. Employing this substitution, it may

5

be observed that the resulting current given by Equation 5 is a decaying exponential with an initial value intermediate the peak currents initially flowing through the inductor 18 and the winding 32₂₁. This current flows in a counterclockwise direction opposite to both of the vectors 100 and 110 for the interval between times *b* and *c* illustrated therein.

It may now be shown that the negative potential assumed above to be present at the collector of the transistor 20 during the time interval from *b* to *c* does in fact occur. The current through each of the inductive elements 18 and 32₂₁ flows in a counter-clockwise direction, and is decreasing in magnitude, as noted above. Hence, a voltage will appear across each of these elements in a direction which will attempt to sustain the current flow therethrough and such voltages are, of course, orientated with their positive terminals in the counter-clockwise direction. Hence, the voltage across each of the elements 18 and 32₂₁, and thereby also their sum, are of the proper polarity to impress a negative potential at the collector of the transistor 20, as was assumed in the above discussion.

The stored charge diode 30₂₁ conducts in the reverse direction for the interval between times *b* and *c* shown in FIG. 2. At time *c*, all the charge stored therein during the forward conduction portion of the cycle of operation between times *a* and *b* has been swept out, and the diode becomes an essentially open circuit in the reverse, or back-biased direction. Hence, for the period following time *c*, illustrated in FIG. 2, the current flowing through the winding 32₂₁ decreases rapidly, limited only by the charging time of the junction and stray capacity associated with the diode 30₂₁.

Hence, it has been shown that when a desired cross-point is selected by coincident pulses supplied by the X pulse source 50 and the Y source 51, first a positive current pulse and immediately thereafter a negative pulse are supplied to the selected cross-point load.

Examining the FIG. 2 graph illustrative of a typical current which flows through a selected cross-point winding 32, it is apparent that the core 33 coupled thereto would be switched in one direction during the time interval from *a* to *b* and then reset to its original polarity during the following interval from *b* to *c*. Note that the resetting operation occurs without any additional, energized reset winding being coupled to the switched core. Also note that the gradually rising, positive ramp of current supplied to the winding 32 has the practical effect of minimizing noise and spurious signals induced in any windings which may be coupled to the core 33 as the core is switched. Such spurious signals are, of course, produced by any marked discontinuities that exist in the switching drive signal.

It is to be observed that while Zener diodes were included to connect the horizontal selection conductors to the appropriate current switches, resistors might well have been employed to produce the equivalent effect of the Zener diodes, viz., impressing a smaller potential across the selected cross-point winding 32 than was supplied to the inductor connected to the emitter of the corresponding switching transistor.

Summarizing, an illustrative matrix selection arrangement made in accordance with the principles of the present invention supplies a bi-polar current signal to a selected one of a plurality of matrix cross-points. Each of the matrix cross-points comprises a stored charge diode serially connected to a winding which is coupled to at least one square-loop ferromagnetic element. The stored charge diode is characterized by a low impedance in its forward conduction direction, and by the capacity to conduct a current in its back-biased, high-impedance direction for a limited period of time.

A Zener diode connects each conductor included in one selection axis to a different one of a first group of current

6

switching transistors. Each conductor included in the other axis is connected to the collector of a different grounded-base transistor included in a second group of transistor switches.

When an input signal is supplied to one transistor from each group, each ferromagnetic element included at the selected cross-point is driven to a like maximum remanent condition. When the input drive is removed, the circuit current reverses direction through the stored charge diode and its associated winding, thereby resetting each selected magnetic element to its original magnetic condition.

It is to be understood that the above-described arrangements are only illustrative of the applications of the principles of the present invention. Numerous other arrangements may be devised by those skilled in the art without departing from the spirit and scope of this invention. For example, while a two-by-two selection matrix was illustrated for the purposes of clarity, any number of rows and columns might well be employed.

Also, note that the sole function of the storage diode 30 is to terminate the reverse current flowing therethrough abruptly at the time *c* shown in FIG. 2. The stored charge diode 30 may thus simply be replaced by a conductor, in which case the exponential current flowing through the winding 32 after time *b* will continue to decay rather than ending abruptly, thereby prolonging the period required for each cycle of operation.

What is claimed is:

1. In combination, a first and second plurality of selection conductors, a plurality of cross-point circuits respectively connecting each of said first plurality of selection conductors to each of said second selection conductors, each of said cross-point circuits comprising a stored charge diode, and a plurality of Zener diodes each serially connected to a different conductor included in said first conductor plurality.

2. A combination as in claim 1, further comprising a plurality of first current switches each characterized by a selective bi-directional conduction capability and connected to a different one of said second selection conductors.

3. A combination as in claim 2, wherein each of said first current switches comprises a transistor including a base and collector terminal, a common ground terminal connected to said base terminal, and said collector terminal being connected to the corresponding selection conductor.

4. A combination as in claim 3, further comprising a plurality of inductors, a plurality of second current switches each comprising a transistor including an emitter terminal which is connected to a different one of said inductors and further connected to a different one of said first selection conductors.

5. A combination as in claim 4, further comprising a plurality of windings each serially connected to a different one of said stored charge diodes, and at least one square-loop ferromagnetic element coupled to each of said windings.

6. In combination, a first and second plurality of selection conductors, a plurality of cross-point circuits respectively connecting each of said first plurality of selection conductors to each of said second selection conductors, each of said cross-point circuits comprising a stored charge diode and a winding serially connected thereto, a plurality of first current switches each comprising a transistor including an emitter terminal and an inductor connected to said emitter terminal, a plurality of Zener diodes each connecting one of said first selection conductors to a different one of said first current switching transistor emitter terminals, and a plurality of second current switches each characterized by a selective bi-directional conduction capability and connected to a different one of said second selection conductors.

7

7. A combination as in claim 6, wherein each of said first transistor current switching transistors includes a base terminal, a plurality of transformers each connected to the base and emitter terminals of a different transistor included in said first plurality of current switches, and a pulse source for energizing a selected one of said transformers coupled to said first plurality of current switching transistors.

8. A combination as in claim 6 wherein each of said second current switches comprises a transistor operated in the grounded base mode.

9. In combination, a first and second plurality of selection conductors, a plurality of load means respectively connecting each of said first plurality of selection conductors to a different one of said second plurality of selection conductors, a source of potential including a point of reference potential for said combination, a plurality of first switching means each connecting said potential source to a different one of said first plurality of selection conductors, a node point intermediate each of said first switching means and its associated first selection conductor, and a plurality of inductors respectively connected between said node points and said point of reference potential for supplying an automatic reverse-direction reset signal to any selected load means that was energized by the application thereto from said source of a forward-direction energization signal, said reverse-direction reset

8

signal being automatically applied to the selected load means in a time interval immediately following the termination of said forward-direction energization signal.

10. A combination as in claim 9 further comprising a plurality of Zener diodes each serially connected between a different one of said node points and its associated first selection conductor.

11. A combination as in claim 10 further comprising a plurality of second switching means each including a transistor operated in the grounded base mode, and means connecting the collector electrode of each of said transistors to a different one of said second selection conductors.

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