

April 11, 1967

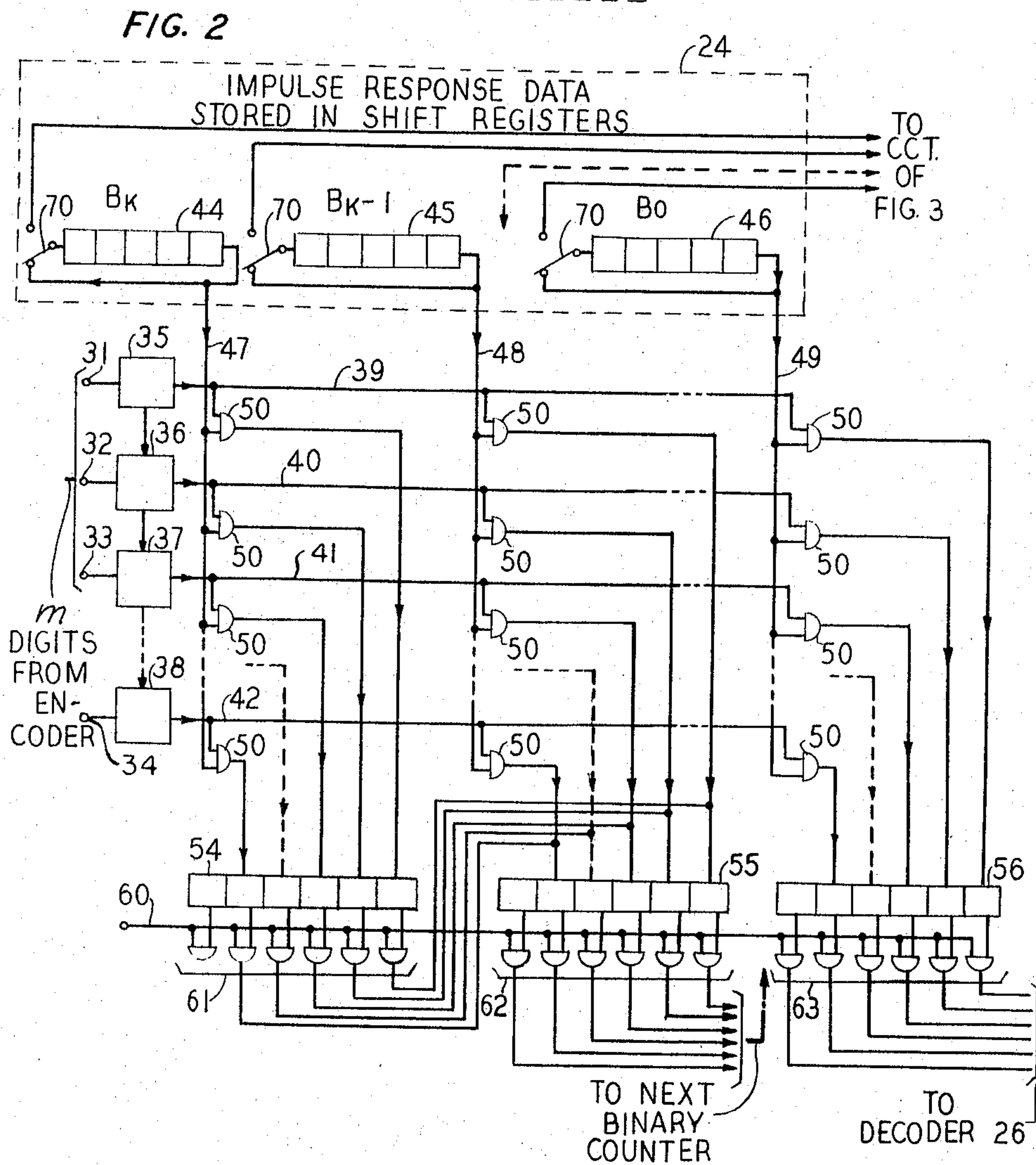
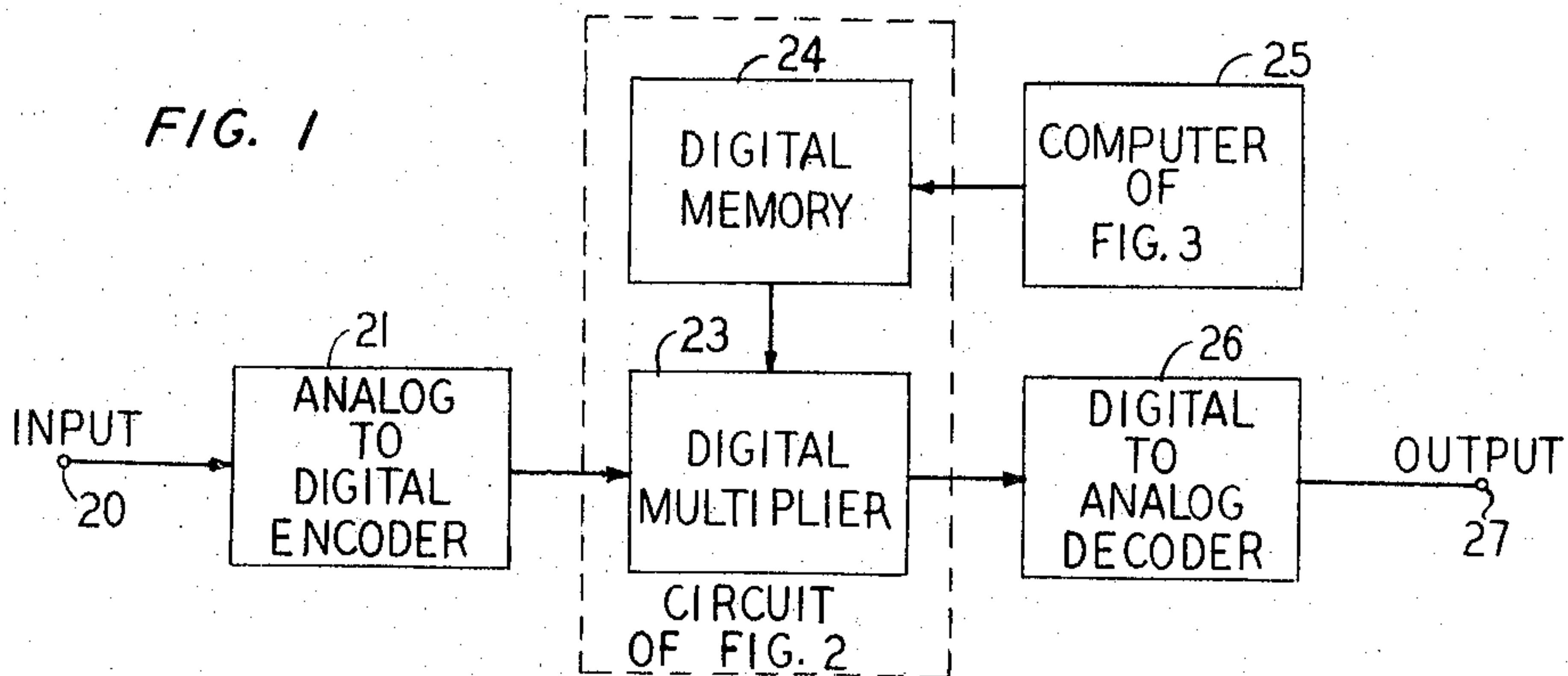
C. F. SIMONE

3,314,015

DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

Filed Sept. 16, 1963

5 Sheets-Sheet 1



INVENTOR  
**C. F. SIMONE**  
 BY *Ray M. Porter Jr.*  
 ATTORNEY



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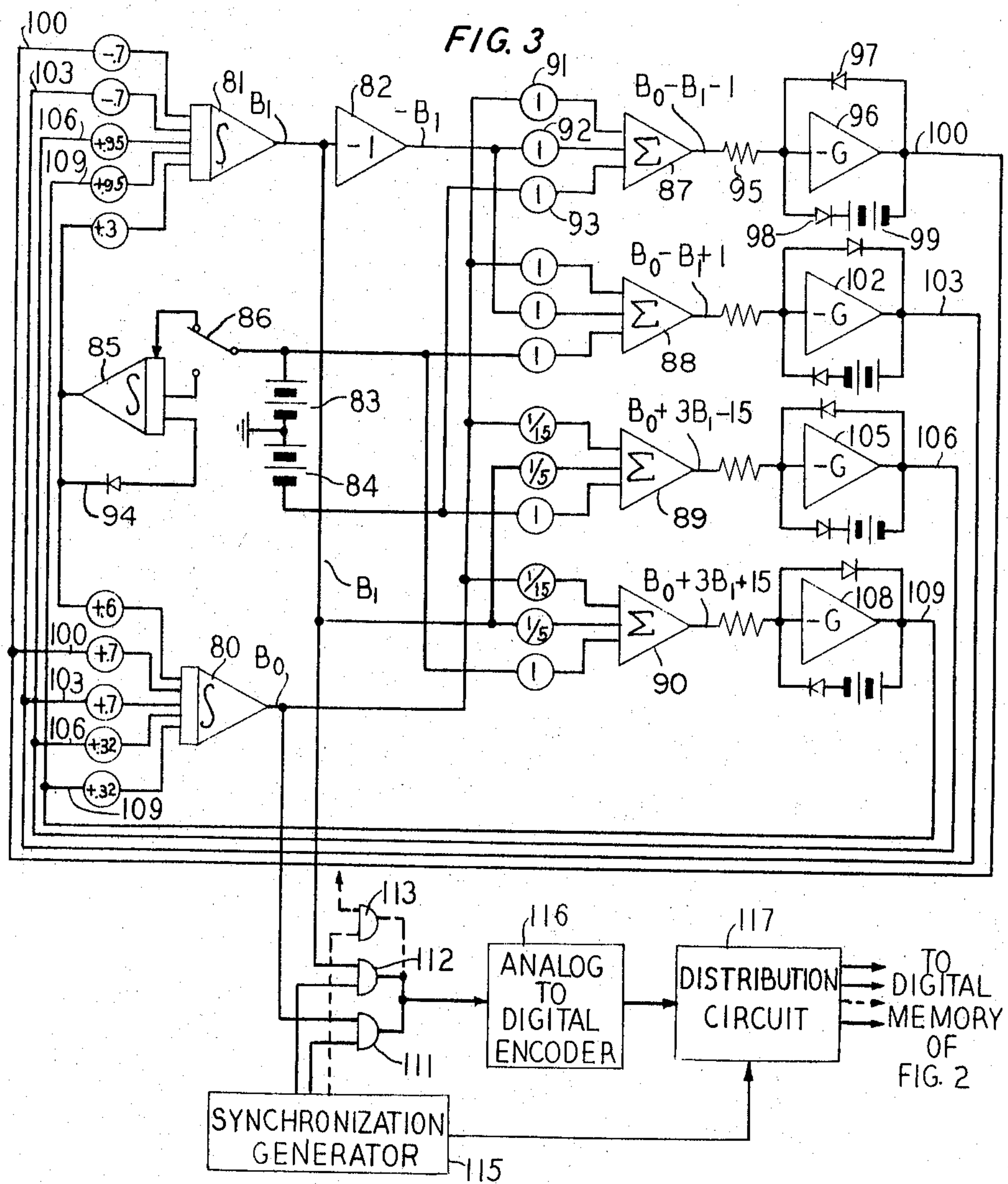
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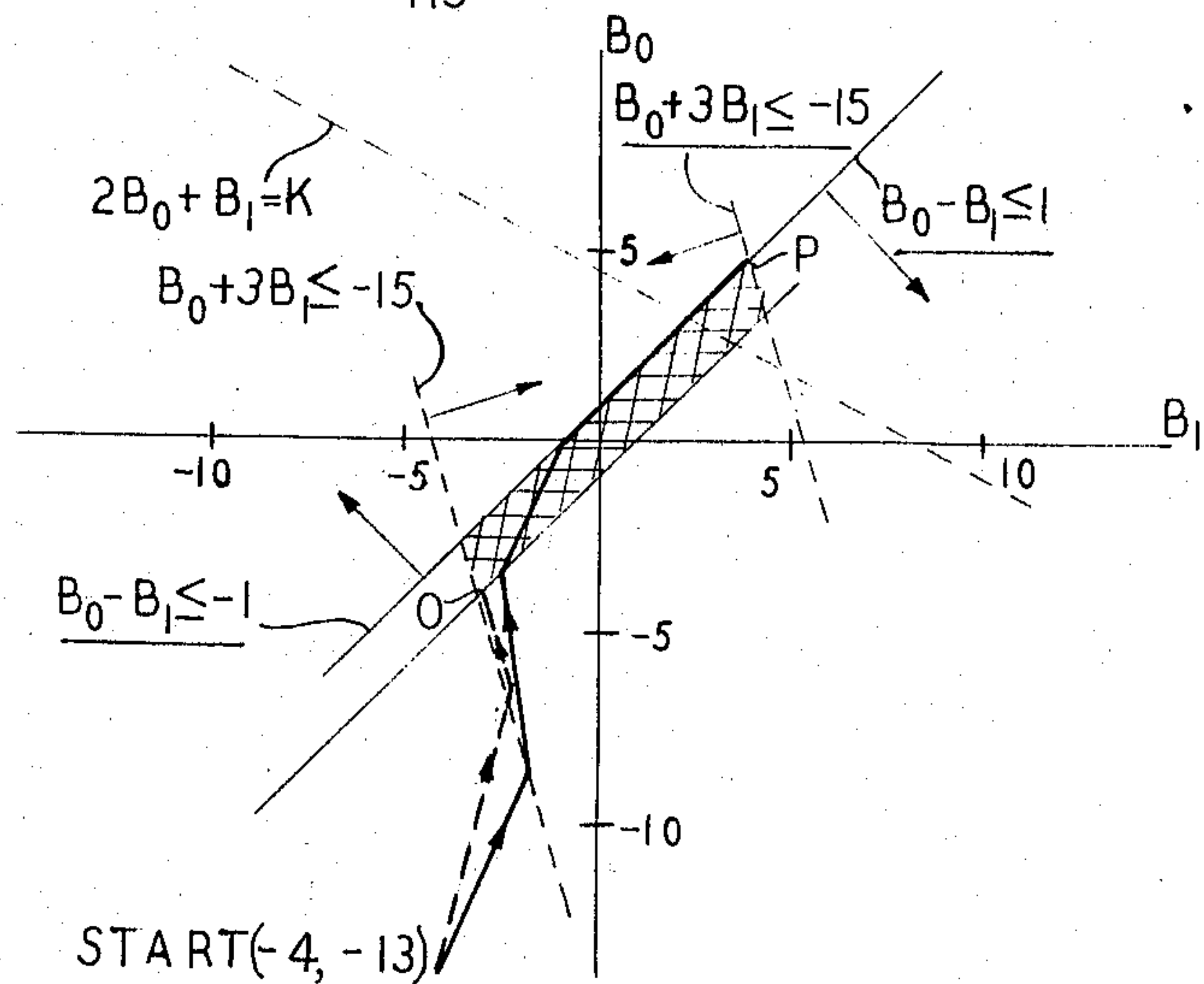
DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

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**FIG. 4**





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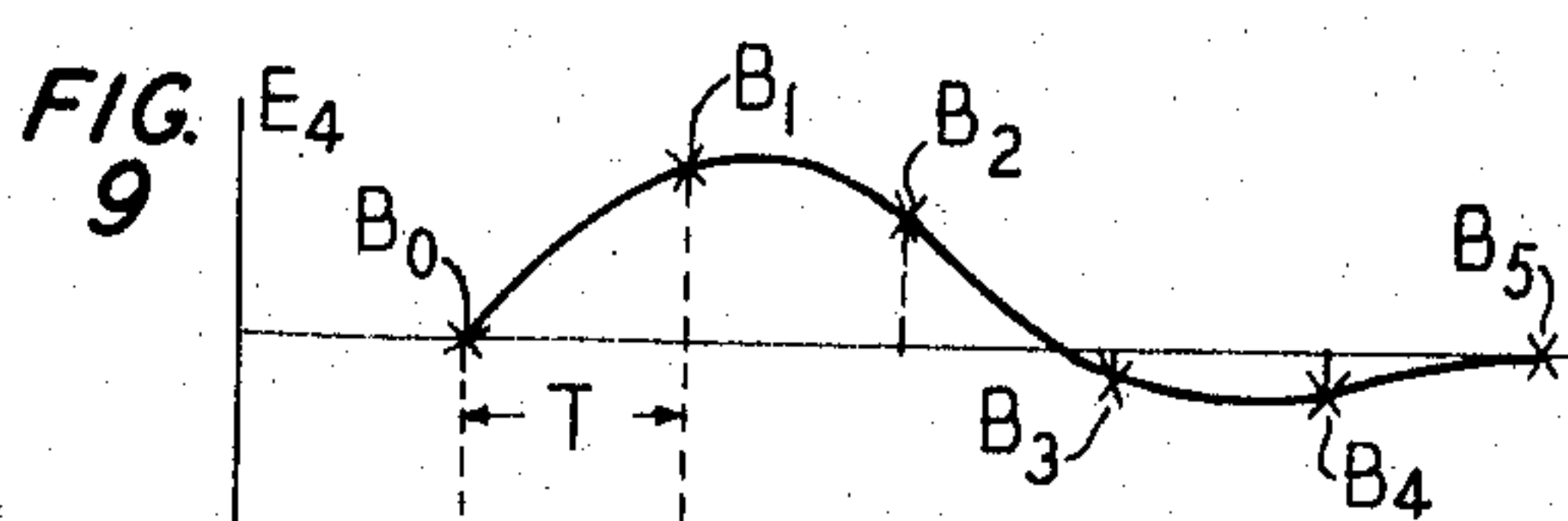
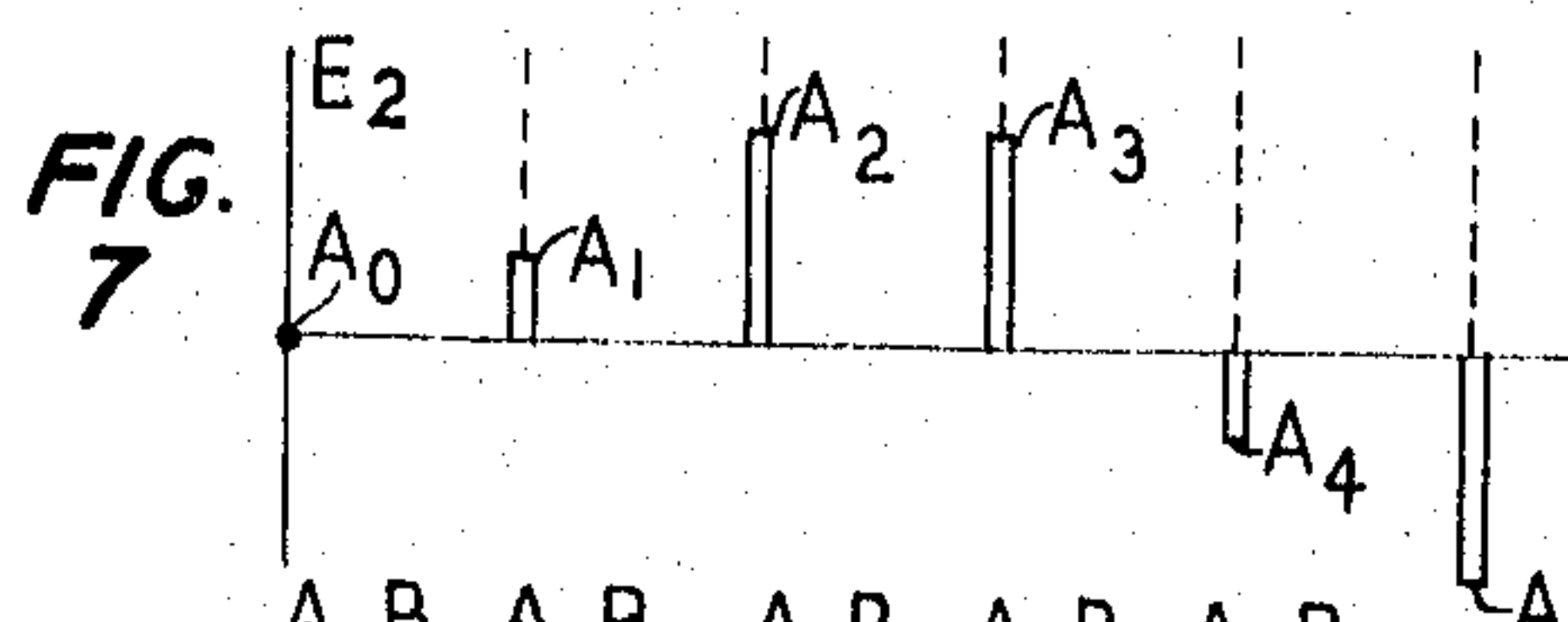
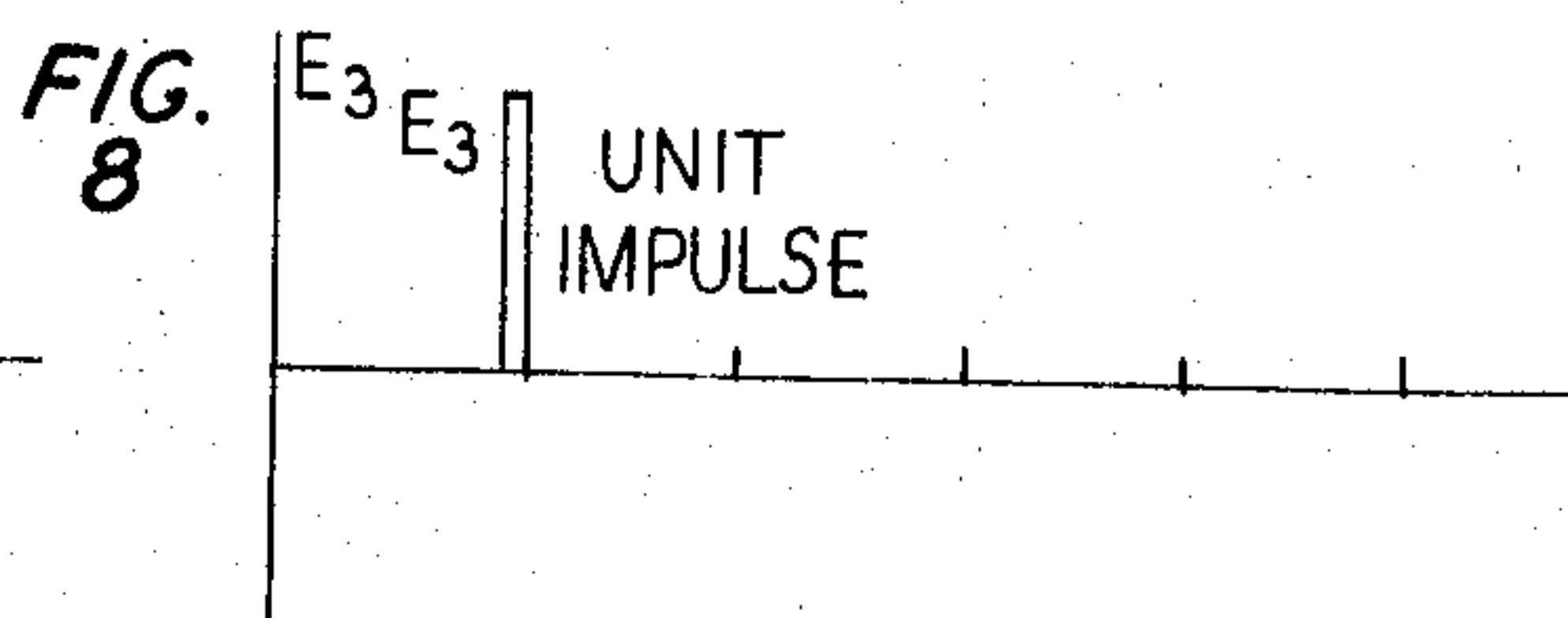
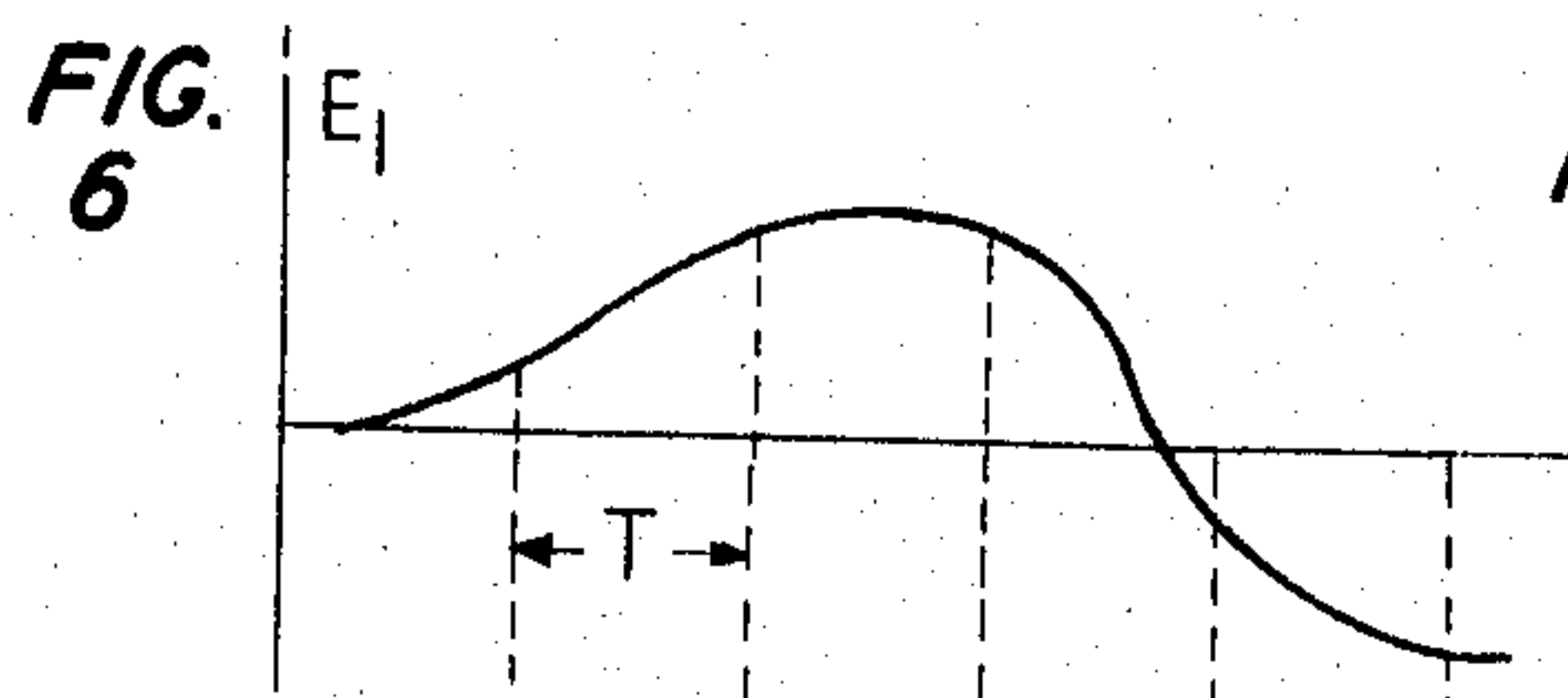
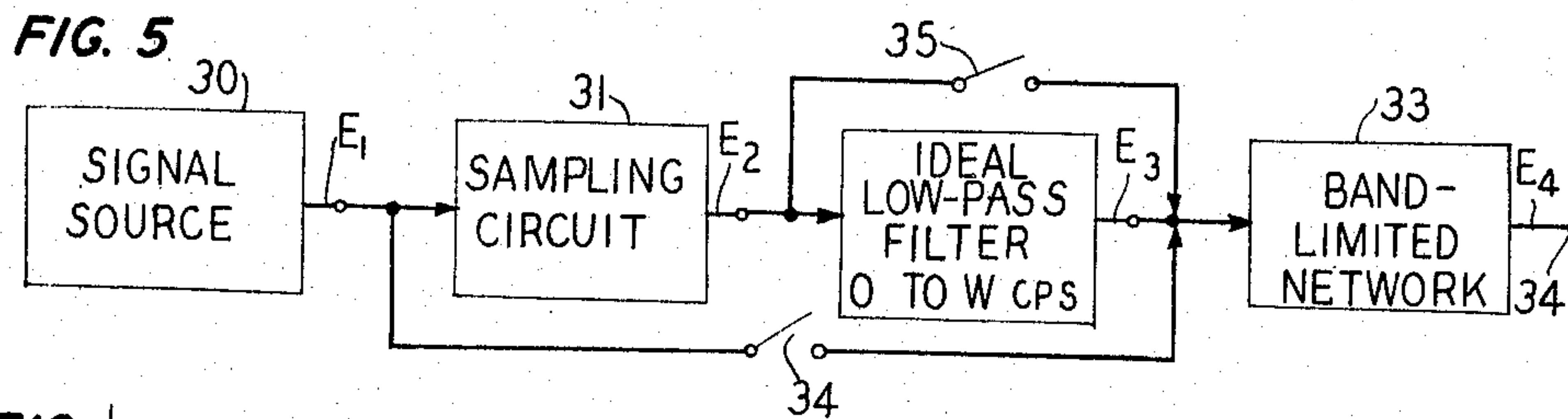
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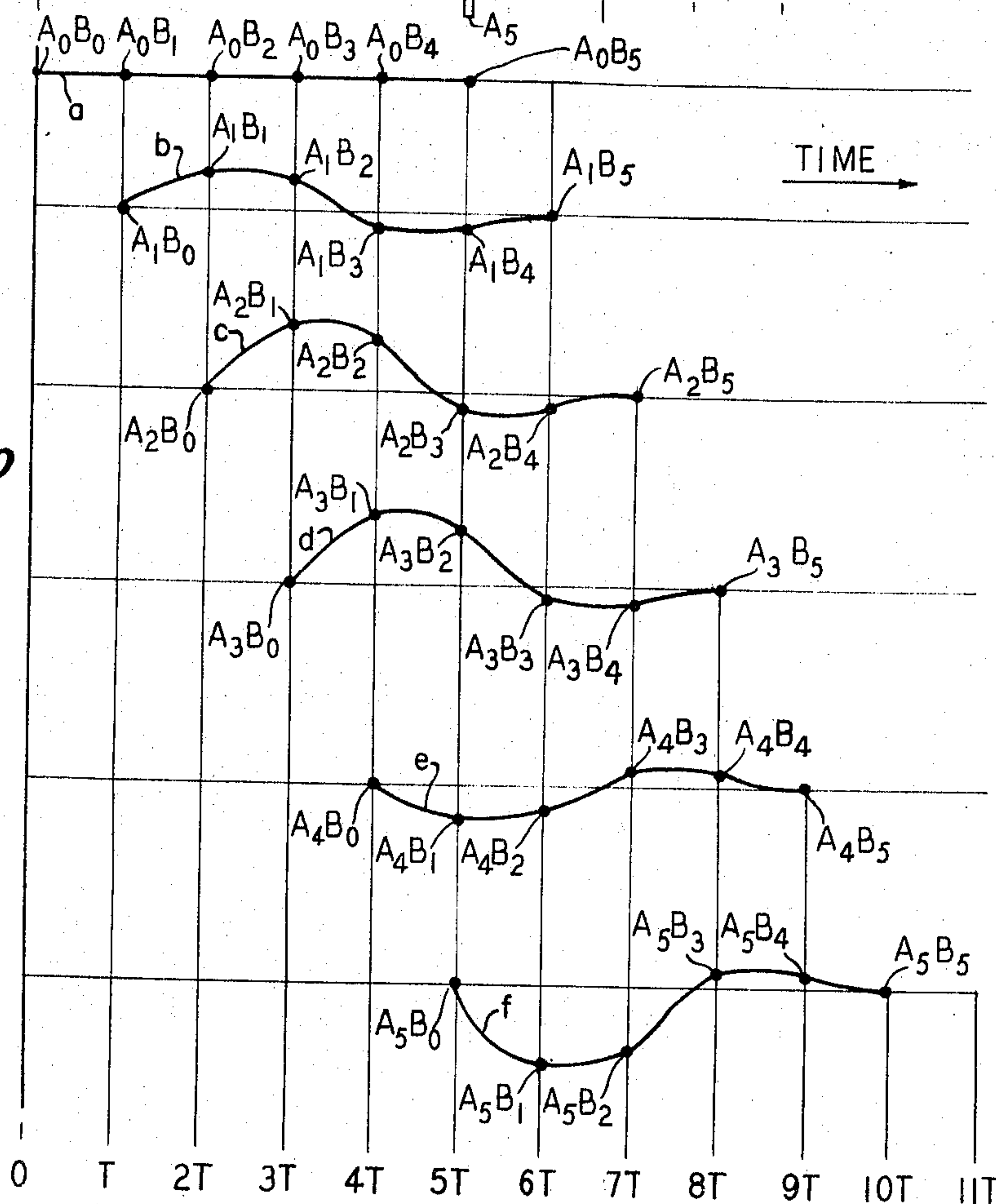
DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

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**FIG. 10**





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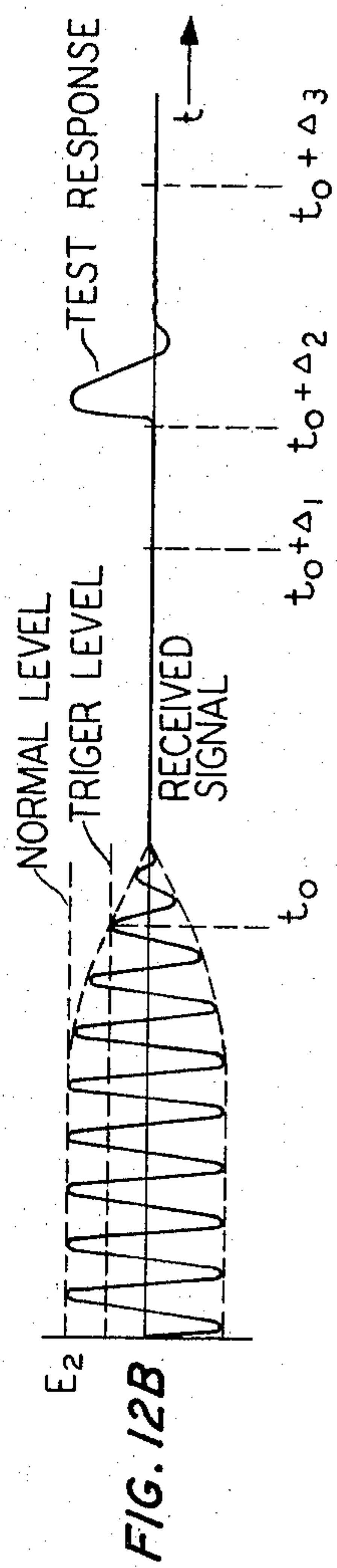
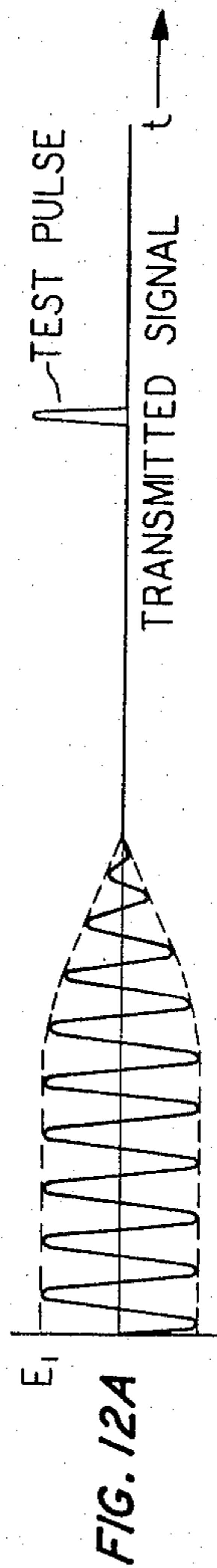
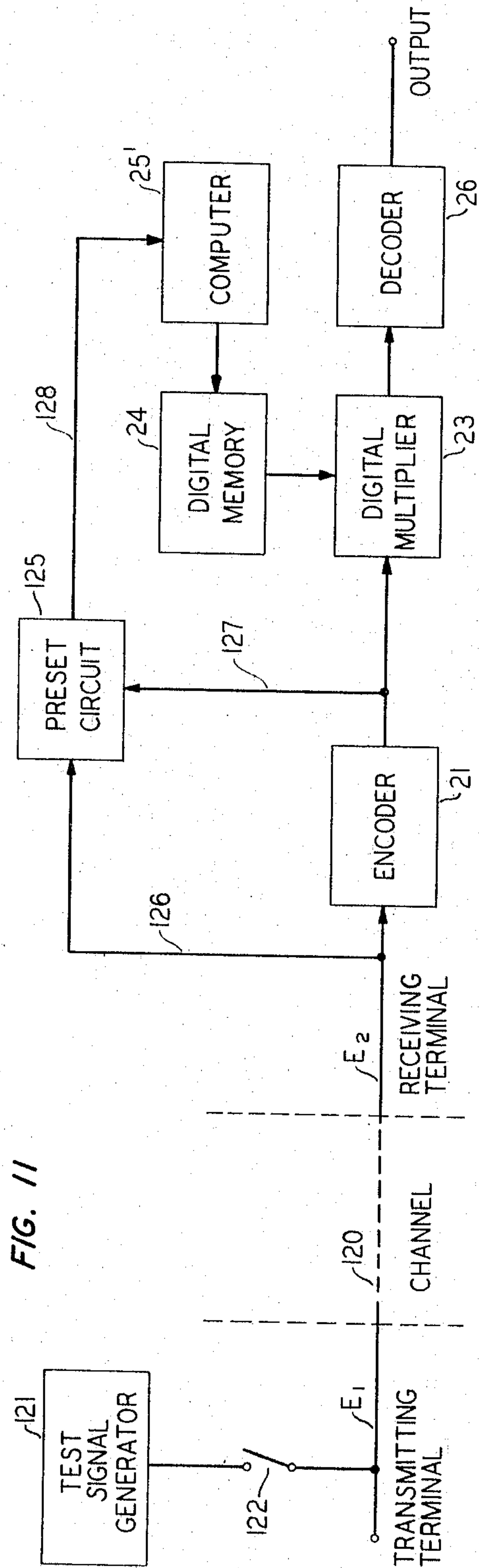
C. F. SIMONE

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DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

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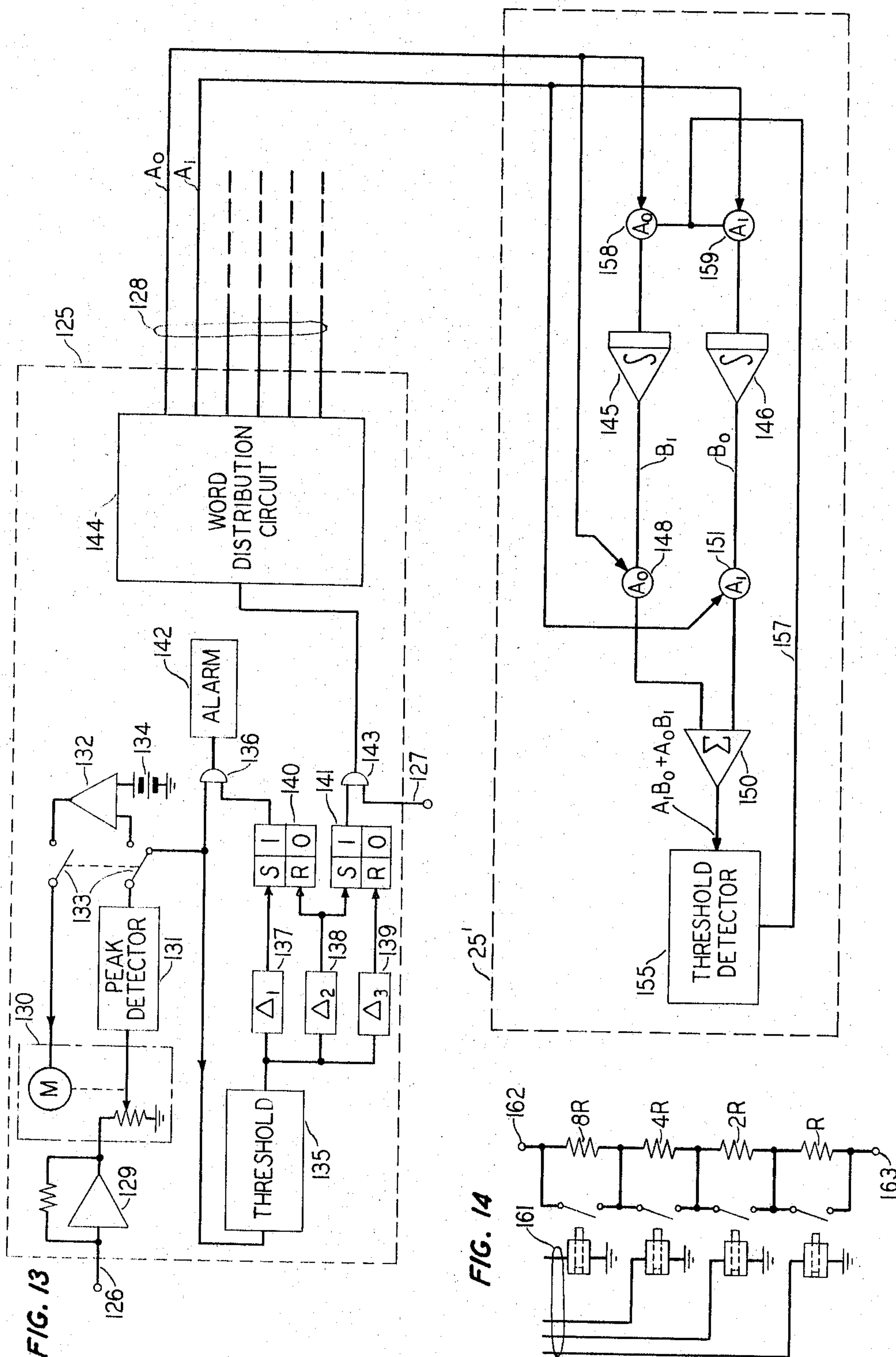
C. F. SIMONE

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# DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

Filed Sept. 16, 1963

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3,314,015

## DIGITALLY SYNTHESIZED ARTIFICIAL TRANSFER NETWORKS

Carl F. Simone, Florham Park, N.J., assignor to Bell Telephone Laboratories, Incorporated, New York, N.Y., a corporation of New York

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5 Claims. (Cl. 328-165)

This invention relates to digital and analog information handling systems and, more particularly, to means for and a method of synthesizing a network having a desired transfer characteristic.

From the standpoint of the signals involved, the basic problem in designing electrical transfer networks may be stated simply. An input waveform of known shape is to be applied to the network and, in response, the network should deliver a desired output waveform. Unfortunately, finding a combination of conventional circuit components which will in fact achieve such a waveform transformation is often quite difficult and, in some cases, impossible.

Consider, for example, the difficulties involved in designing an extremely steep-skirted low-pass filter having a cut-off frequency of  $W$  c.p.s. The problem may be presented in the time-domain, waveform context by determining the "impulse-response" of such a network. By means of known methods of analysis, it may readily be shown that if a unit impulse is applied to an "ideal" low-pass filter, the output waveform,  $E_o$ , has a shape given by the following relation:

$$E_o = k \frac{\sin \pi W t}{\pi W t}$$

where  $t$  is time and  $t=0$  is the time at which the input impulse is applied. It will be noted that  $E_o$  is not zero-valued when  $t$  is less than zero, leading to the conclusion that the network must begin delivering an output even before an input is applied. Clearly such a network is not physically realizable, although its response could be imitated if an arbitrarily long delay were permissible between the occurrence of the input signal and the beginning of the response.

Still other situations arise where the transfer response to be synthesized, while physically realizable in theory, is so complex as to make synthesis by conventional techniques impractical. The design of transmission path equalizers exemplifies the difficult problems often encountered. If a single data pulse is applied at the transmitting end of an unequalized telephone transmission line, for example, an oddly shaped waveform which is quite dissimilar from the transmitted pulse is received at the other end. This distorted waveshape is then applied to the equalization network from which, ideally, emerges a single pulse shaped like the transmitted pulse. As will be readily appreciated, the design of such an equalization network is often so complicated that a detailed analysis and synthesis by known methods is not economically worthwhile. Consequently, only approximate equalization is normally attempted.

Complex network synthesis problems arise in many other fields, including control systems, closed-loop servomechanisms, electronic simulating systems, and so on. In all of these areas, it is desirable that the desired transfer response be developed quickly, accurately, and automatically.

Accordingly, it is a principal object of the present invention to synthesize a network having a desired transfer response through the use of high speed digital and analog information handling techniques.

In a principal aspect, the present invention takes the

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form of an artificial transfer network which may be made to accurately approximate a desired response. In accordance with the invention, the input signal to the network is first sampled and encoded to form a polynomial series of binary numbers, the terms of which represent the amplitude of the input signal taken at intervals. By means of a novel multiplying circuit, this input polynomial is then multiplied by another binary polynomial stored in a digital memory. In accordance with a principal feature of the invention, this stored polynomial is representative of the impulse response desired and is composed of a fixed number of terms, each of which is optimized by a coacting, special-purpose network in response to automatically programmed input information. The decoded product of the input polynomial and the stored polynomial forms the desired output waveform.

According to a further feature of the invention, the "artificial transfer network" may be advantageously adapted to automatically equalize a transmission facility. As contemplated by the invention, means may be included at the transmission end of the facility for generating a short duration testing signal having a finite frequency content throughout the selected band of interest. This testing signal is then transmitted over the facility, sampled at the receiving end, and the resultant samples passed to the optimizing network which automatically develops a polynomial series of numbers which most nearly approximates the inverse of the test response sample series. This inverse series is then stored in the digital memory to affect equalization of both phase and amplitude of the incoming signals.

These and other objects, features and advantages of the invention will be more clearly understood following a consideration of the following detailed description and drawings of a specific embodiment of the invention. In the drawings:

FIG. 1 is a simplified block diagram of the artificial network contemplated by the invention;

FIG. 2 is a detailed drawing of memory and multiplier circuits which may be employed to instrument the present invention;

FIG. 3 shows a special-purpose analog computing arrangement which may be employed in the invention;

FIG. 4 illustrates the operation of the circuit of FIG. 3;

FIG. 5 shows a circuit, the consideration of which is useful in understanding certain principles underlying the invention;

FIGS. 6 through 10 are waveforms which are useful in describing the principles of the invention;

FIG. 11 illustrates a transmission path equalizing system as contemplated by the present invention;

FIGS. 12A and 12B show a pair of waveforms of the type transmitted and received during the process of equalizing a transmission path by means of the scheme shown in FIG. 11;

FIG. 13 shows in more detail the preset and computer circuit of FIG. 11; and

FIG. 14 illustrates a simple digitally-operated potentiometer which may be used to instrument the computer shown in FIG. 13.

## GENERAL DESCRIPTION

FIG. 1 of the drawings shows an artificial network of the type contemplated by the present invention. Input terminal 20 of the analog-to-digital encoder 21 constitutes the input to the artificial network. The binary output signal from encoder 21 is fed to a first input of digital multiplier 23. The other input to digital multiplier 23 is connected to the output of a digital memory 24. The portion of the artificial transfer network which includes multiplier 23 and memory 24 is enclosed in dotted



lines and is shown in detail in FIG. 2 of the drawings. The digital memory 24 is connected to receive binary information from the computer 25. Circuit details of a typical computer used to instrument the invention are shown in FIG. 3 of the drawings. The output of the digital multiplier 23 is connected to the input of a digital-to-analog decoder 26, the output of which forms the output for the artificial network.

In accordance with the invention, the input signal which is to be passed through the artificial network is applied to input terminal 20 and hence to the input of the analog-to-digital encoder 21. Encoder 21 samples the input waveform at intervals and encodes the amplitude of each sample into a binary "word" composed of several digits. Each of these binary words is a binary number representative of the amplitude of a particular sample. The multiplier 23 forms the polynomial product of the series of binary numbers from encoder 21 and another series of binary numbers from the memory 24. According to the invention, the polynomial number series stored in memory 24 is representative of the impulse response desired and is composed of a fixed number of terms, each of which is developed and optimized by the computer 25. The signal appearing at the output of multiplier 23 is also a polynomial series of binary numbers which is translated by the decoder 26 into a continuous output waveform which appears at output 27.

### BACKGROUND

In order to obtain a more complete understanding of the present invention, it will be necessary to consider several basic principles which underlies its operation. With this in view, attention is directed to the illustrative circuit shown in FIG. 5 of the drawings. In FIG. 5, a signal source 30 is shown which delivers an output signal,  $E_1$ , to the input of a sampling circuit 31. The output signal  $E_2$ , from sampling circuit 31 is fed to the input of an ideal low-pass filter 32 having a cut-off frequency of  $W$  cycles per second. The "ideal" low-pass filter 32, not being physically realizable, is used in a theoretical sense only. As will be seen, the ideal filter 32 may be eliminated. The filter 32 delivers an output signal,  $E_3$ , to the input of an arbitrary band-limited network 33. The output terminal 34 receives an output signal,  $E_4$ , from the network 33.

The signal from source 30 is characterized in that it possesses no frequency components higher than  $W$  cycles per second. FIG. 6 of the drawings illustrates a typical waveform for signal  $E_1$ . The circuit 31 samples the signal  $E_1$  and delivers a series of pulses,  $E_2$ , the amplitude of each pulse being scaled to represent the amplitude of  $E_1$  taken at intervals. With the waveform as shown in FIG. 6, circuit 31 would deliver a series of sample pulses as shown in FIG. 7 of the drawings. The signal from the sampling circuit 31 may be expressed functionally by the following relation:

$$\sum_n A_n G(t - nT)$$

where  $A_n G(t - nT)$  is the  $n$ th sample pulse and  $T$ , the spacing between pulses, is less than  $1/2W$  seconds.

As is well known from the Nyquist sampling theorem, the sample signal  $E_2$ , if passed through the ideal low-pass filter 32, would be converted back into the original waveform  $E_1$ . Thus it may be seen that closing the switch 34 does not affect the shape of the waveform  $E_3$ . Furthermore, if it is assumed that the band-limited network 33 will pass no frequency components higher than  $W$  cycles per second, the low-pass filter 32 performs no useful function (it does not affect any of those signals which pass through network 33). Thus the switch 35 may also be closed without altering the form of the signal which is delivered to output terminal 34. Since switch 35 can be closed without changing the output waveform  $E_4$ , it is apparent that it makes no difference whether the signal  $E_1$

as shown in FIG. 6 or the sample pulses  $E_2$  as shown in FIG. 7 are applied to the network 33—the shape of the output waveform  $E_4$  is unaffected.

To determine the nature of the output signal  $E_4$ , consideration need therefore only be given to the response of the network to a series of sample pulses such as the series shown in FIG. 7. It will be convenient to start with an investigation of the network's response to a single input pulse of unit amplitude as shown in FIG. 8 of the drawings.

When a single impulse is applied to the network 33 shown in FIG. 5, an output waveform of the type illustrated by FIG. 9 is delivered to terminal 34. This output waveform is termed the "impulse response" of the network. It will be remembered that network 33 passes no frequency components higher than  $W$  cycles per second. Consequently, the impulse response may also be represented by a series of sample values,  $B_0$  through  $B_5$ , taken at intervals  $T = 1/2W$  as shown in FIG. 9.

The network 33, in addition to being band-limited, will also be assumed to be both linear and time-invariant. By "linear" is meant that the shape of the impulse response is not in part dependent upon the magnitude of the input impulse applied. By "time-invariant" is meant that if an input to the network,  $X(t)$ , resulting in an output  $Y(t)$ , then an input  $X(t+T)$  will cause an output  $Y(t+T)$ . By making use of the superposition principle for linear, time-invariant systems, the output from network 33 due to a series of input pulses may be considered to be made up of the responses due to each previous pulse taken singly.

By way of example, consider the response of network 33 to the series of pulses shown in FIG. 7 of the drawings. The first pulse, having an amplitude  $A_0=0$ , delivers no output at all as shown in curve  $a$  of FIG. 10. The second pulse, having an amplitude  $A_1$ , delivers an output waveshape as shown in curve  $b$  of FIG. 10. The amplitude of the response from this second pulse is merely  $A_1$  times the amplitude of the response due to the unit impulse. Curves  $c$  through  $f$  show the response of network 33 to the third through sixth pulses respectively. Notice in curves  $c$  and  $f$  that the response is negative-going since the fifth and sixth pulses shown in FIG. 7 were negative-going. In accordance with the superposition principle mentioned earlier, determination of the output from network 33 is merely a matter of adding the responses of the various pulses. Thus at  $t=0$ , the output from network 33 would have an amplitude  $A_0B_0$ , at  $t=T$ ,  $E_4=A_0B_1+A_1B_0$ , and so on.

It may now be noted that the sample series of the output signal from network 33 is analogous to the product of two polynomials. This is illustrated by the multiplication shown below:

$$\begin{array}{r} A_0 + A_1X + A_2X^2 + \dots + A_nX^n \\ B_0 + B_1X + B_2X^2 + \dots + B_kX^k \\ \hline C_0 + C_1X + C_2X^2 + \dots + C_{n+k-1}X^{n+k-1} \end{array}$$

where:

$$\begin{array}{l} C_0 = A_0B_0 \\ C_1 = A_1B_0 + A_0B_1 \\ C_2 = A_2B_0 + A_1B_1 + A_0B_2 \\ C_3 = A_3B_0 + A_2B_1 + A_1B_2 + A_0B_3 \end{array}$$

and so on.

Note that the coefficients,  $C_0$  through  $C_{(n+k-1)}$ , of the product polynomial are the same as the sample amplitudes of the output signal from the network. Thus it is seen that, to calculate the output of a network in response to an input waveform, the polynomial representing the network's impulse response would be multiplied by the polynomial sample series of the input waveform. The resulting polynomial would be a representation of the output waveform.

In accordance with one aspect of the present invention, a desired transfer network may be synthesized by actu-



ally performing this polynomial multiplication. The input signal to the network is sampled and encoded to form a first polynomial series of binary numbers. This first polynomial is then multiplied times a second binary polynomial stored in a digital memory. This second polynomial which is stored in the memory is representative of the impulse response desired. According to a further feature of the invention, the stored polynomial may be limited to a predetermined maximum number of terms, each of which may be optimized by a coating, special-purpose analog computer. The decoded product of the first and second polynomials forms the desired output waveform.

As shown in FIG. 1 of the drawings, the input signal is first applied to the analog-to-digital encoder 21. Encoder 21 may comprise any one of many well-known encoders, such as those used in PCM systems. An encoder which may be advantageously used in conjunction with the present invention is described in U.S. application, Ser. No. 227,271, filed Oct. 1, 1962, by F. D. Waldhauer, now Patent No. 3,161,868. The Waldhauer encoder delivers an  $m$ -digit binary word which is representative of the instantaneous amplitude of the input signal. The  $m$ -digits of each word are delivered in parallel; that is, each digit is delivered on its own output conductor.

#### DETAILED DESCRIPTION—MULTIPLIER AND MEMORY

FIG. 2 of the drawings illustrates a novel memory and multiplier circuit which may be advantageously employed to instrument the present invention. The  $m$  digits from the encoder 21 are applied in parallel to the  $m$  multiplier input conductors 31 through 33. Conductors 31 through 34 comprise the information inputs to the input shift register which consists of  $(m+n-1)$  register stages 35 through 38. (Where  $n$  is the number of digits in each word stored in memory 24.) The outputs of stages 35 through 38 are connected to row conductors 39 through 42, respectively. It will, of course, be understood that  $(m+n-1)$ , the total number of input shift register stages and row conductors, is dependent both on the number of digits in the encoded word from the encoder 21 and the number of digits in each word stored in memory 24.

In the memory circuit 24 shown in detail in FIG. 2, digital information is stored in a series of shift registers 44 through 46. Each register stores a digital word comprising  $n$  digits and has as many stages as digits in the word stored. The output from shift register 44 is fed into the multiplier 23 by means of a column conductor 47. Similarly, the output from register 45 is connected to column conductor 48 and the output from register 46 is connected to column conductor 49. The total number of memory shift registers and associated column conductors,  $k$  is equivalent to the total number of impulse response samples to be stored in the memory 24.

With the  $m$  row conductors 39 through 42 and the  $k$  column conductors 47 through 49 are connected  $mk$  AND gates 50. Each of the AND gates 50 is provided with two inputs, one of which is connected to a row conductor and the other connected to a column conductor. For example, the column conductor 47 is connected to an input of  $m$  AND gates 50, the other input of these AND gates being connected to respective ones of the  $m$  row conductors 39 through 42.

Each of the AND gates 50 is provided with an output conductor which is connected to the input of a summing binary counter. The output of each AND gates 50 associated with column conductor 47 delivers an output signal to an "accumulator set" of binary counters 54. In like manner, the AND gates associated with column conductor 48 deliver output signals to an accumulator set 55 and those AND gates 50 connected to column conductor 49 deliver output pulses to an accumulator set of counters 56. Each accumulator set 54 through 56 is provided with an output circuit comprising a set of AND gates, one

input of each gate being connected to a gating conductor 60 and the other input of each being connected to one of the counters in an accumulator. Each of the binary counters in the set 54 has an output connected to an input of one of the AND gates 61. Similarly, the set of counters 55 is connected to a set of AND gates 62 and the set of counters 56 is connected to a set of AND gates 63. The output of each AND gate 61 is connected to the input of one of the binary counters in set 55. The outputs from AND gate 62 are then connected to the input to the next set of counters (not shown) and so on. The output from the AND gates 63 is delivered to the decoder 26 and forms the output from the multiplier.

To initiate the operation of the artificial network, the encoder 21 shown in FIG. 1 delivers to the multiplier 23 a binary word representing the amplitude of the first sample of the input signal. This  $m$ -digit binary number,  $A_0$ , is delivered to the input shift register stages 35 through 37. The least significant binary digit of this word is applied to the stage 35, and so on, with the most significant digit being applied to register stage 37.

Before operation is commenced, the shift registers 44, 45 and 46 are filled with appropriate information from computer 26 by moving the switches 70 to their upper positions while digits are shifted into the associated register. Each switch 70 is then returned to its normal position to allow the digits to circulate through each register.

Each shift register in the memory 24 holds a binary word representative of the amplitude of a single impulse response sample. Thus, the  $k$ th sample having an amplitude  $B_k$  is stored in register 44, with the least significant digit being the first to appear on column conductor 47. Similarly, the register 45 holds a binary word representative of the amplitude of the next to the last impulse response sample,  $B_{k-1}$ . The amplitude of the first sample,  $B_0$ , is stored in binary form in the last register 46. All of the impulse response sample words are stored in the registers such that the least significant digit appears at the output of the register and is delivered to the connected column conductor first.

At the first instant in which multiplication is commenced, all of the digits in the first sample  $A_0$  are multiplied by the least significant digit of each of the impulse response samples  $B_0$  through  $B_k$ . The AND gates 50 perform the digit-by-digit multiplication and the respective products are stored in the proper binary counter accumulator sets 54 through 56. During the next portion of the multiplication operation, the input register shifts the sample  $A_0$  downward, the least significant digit moving from stage 35 to stage 36. Also, the digits in the memory registers 44 through 46 are shifted one stage to the right. Multiplication of the next-to-least significant digit of the stored words times the newly aligned input word is then accomplished. The binary counters in the accumulator sets 54 through 56 are provided with a "carry" mechanism such that whenever one counter changes state twice the next counter to the left is caused to change state. Each time the input word is shifted in the input register, the memory registers 44 through 46 also shift to deliver a new digit to the multiplying matrix. Finally, when the initial input word is shifted entirely out of the input register, the accumulator sets 54 through 56 hold the product of the initial sample  $A_0$  times respective ones of the stored samples  $B_0$  through  $B_n$ . At that time, gating conductor 60 is energized thereby passing the contents of each accumulator set 54 through 56 to the next accumulator set to the right. This shifting between the accumulator sets of counters provides the necessary alignment of sub-products that must be summed. Note that the accumulator sets 55 and 56 are provided with an additional counter on the left for registering the possible extra carry digit.

As may be appreciated from a consideration of the arrangement shown in FIG. 2, the output from the AND gates 63 represents a series of binary words each being a part of the product of the input sample series and the



stored sample series. This output sample series is passed in binary form to the decoder 26 as shown in FIG. 1 of the drawings. Decoder 26 may well comprise a parallel binary input-analog output decoder of the type described in U.S. Patent 3,145,377 which issued Aug. 18, 1964 to F. A. Saal.

#### DETAILED DESCRIPTION—ANALOG COMPUTER

As explained above, the output of a network in response to a given input signal may be simulated by multiplying the polynomial series representing the input waveform times the polynomial representing the network's impulse response. The resulting polynomial series, when decoded, forms the desired output waveform.

One method of impulse response determination which is applicable to the transmission path equalization problem involves determining the impulse response of the path to be equalized and then storing, in time reversed order, the samples of this response. Although such a scheme corrects for phase distortion only, it has proven to be quite useful. U.S. Patent 2,908,874 which issued to J. R. Pierce on Oct. 13, 1959 describes a method of forming, on an analog basis, the product of the incoming signal and the time-reversed impulse response of the path to be corrected. In U.S. Patent 3,071,739 issued to J. P. Runyon on Jan. 1, 1963, a phase distortion equalizer which forms the product of the input signal and the time-reversed impulse response of the transmission link by digital means is described. Unlike the present invention, these prior equalization schemes are inherently unable to correct amplitude distortion and accordingly, additional equalizers must also be employed. As will be explained below, however, the present arrangement employs optimized impulse response data such that an equalizer according to the invention is capable of correcting for both phase and amplitude distortion.

In some applications, the artificial network may be "programmed" directly. In situations where the desired impulse response is already known or readily ascertained, the necessary information may be developed and stored in the memory by straightforward techniques. Likewise, where the input waveshape is known and the desired output waveshape is also known, the impulse response required may, in some cases, be found by dividing the desired output polynomial by the input polynomial. Often, however, direct division will yield an unbounded, nonconvergent series requiring special analytical algorithms or other techniques for solution.

In the usual case, furthermore, the total number of terms in the "perfect" impulse response series (even if it could be conveniently derived) will exceed the capacity of the memory. Unfortunately, the best approximation using a fixed number of stored terms is not obtained by merely filling the memory to capacity with the first terms appearing in the perfect response and then disregarding the remaining terms of the series. Instead of "truncating" the impulse response series in this fashion, great improvement may be realized in accordance with the present invention by optimizing the magnitude of each term individually. A high-speed analog computer may be employed to provide this optimization function. The use of the optimizing computer increases the versatility of the artificial network and provides the best possible performance with a memory and multiplier of predetermined capacity.

The optimization problem solved by the computer may be best illustrated by referring once again to the polynomial multiplication shown below.

$$\begin{array}{r} A_0 + A_1X + A_2X^2 + \dots + A_nX^n \\ B_0 + B_1X + B_2X^2 + \dots + B_kX^k \\ \hline C_0 + C_1X + C_2X^2 + \dots + C_{(n+k-1)}X^{(n+k-1)} \end{array}$$

From which may be obtained the following  $(n+k)$  equations:

$$C_0 = A_0B_0$$

$$C_1 = A_1B_0 + A_0B_1$$

$$C_2 = A_2B_0 + A_1B_1 + A_0B_2$$

$$C_3 = A_3B_0 + A_2B_1 + A_1B_2 + A_0B_3$$

and so on—up to the last equations:

$$C_{(n+k-2)} = A_nB_{k-1} + A_{n-1}B_k$$

$$C_{(n+k-1)} = A_nB_k$$

If the input signal series of coefficients,  $A_0$  through  $A_n$ , is known, the problem is to find the series of impulse response coefficients,  $B_0$  through  $B_k$ , which will produce a series of product coefficients most similar to the desired output series. It should also be remembered that the total number of terms in the impulse response is limited by the capacity of the memory—that is,  $k$  is a fixed, finite number. It may be seen that the problem is "over-determined," there being  $k$  unknowns and  $(n+k-1)$  equations.

The optimum solution for such an overdetermined system of equations may be found through the use of "linear programming." Since all of the equations cannot be satisfied exactly, the approach begins with the criterion that none should depart from exact equality by more than an arbitrary error,  $r$ . Thus, the following  $2(n+k-1)$  inequalities may be written:

$$\begin{cases} A_0B_0 - C_0 \leq r \\ A_0B_0 - C_0 \geq -r \\ A_1B_0 + A_0B_1 - C_1 \leq r \\ A_1B_0 + A_0B_1 - C_1 \geq -r \end{cases}$$

and so on—up to the last inequalities:

$$\begin{cases} A_nB_k - C_{(n+k-1)} \leq r \\ A_nB_k - C_{(n+k-1)} \geq -r \end{cases}$$

In accordance with the linear programming scheme, a maximum or minimum value of a linear function of many variables is sought while, at the same time, these variables are constrained to satisfy a set of linear conditions. The inequalities shown above thus form the conditions and an equation representing the total error forms an equation to be minimized.

The linear programming method of impulse response optimization may be more clearly understood by referring to a specific example. For this purpose, the method of optimizing the terms of an impulse response for equalizing a telephone transmission facility will be described. Assume that a single impulse is transmitted through the telephone facility such that it emerges at the receiving end as an oddly shaped waveform. It is desired to apply this distorted waveshape to the input of the digital equalization network such that a single pulse of the type transmitted emerges from the equalizer. Hence, the distorted input waveshape and its samples,  $A_0$  through  $A_n$  are known. The desired output waveshape, being a single pulse, is also known. Stated in terms of polynomials, it is desired to select an impulse response series,  $B_0$  through  $B_k$ , which will deliver an output series,  $C_0$  through  $C_{n+k}$ , all terms of which except one,  $C_j$  (indicating the pulse), are as close to zero as possible. The inequalities for all of the "C" terms except  $C_j$  may then be written as below:

$$\begin{cases} A_0B_0 \leq r \\ A_0B_0 \geq -r \\ A_1B_0 + A_0B_1 \leq r \\ A_1B_0 + A_0B_1 \geq -r \end{cases}$$

and so on—up to the last inequalities:

$$\begin{cases} A_nB_k \leq r \\ A_nB_k \geq -r \end{cases}$$

The equation to be maximized is then merely the equation for the selected output coefficient,  $C_j$ , which is to be representative of the position of the output pulse. This equation, determined from the polynomial multiplication, may be written, in general form, as follows:

$$C_j = f(B_0, B_1, B_2, \dots, B_k)$$



FIG. 3 of the drawings shows a special purpose analog computing arrangement which may be employed in accordance with the present invention. FIG. 4 of the drawings illustrates the operation of the computer shown in FIG. 3. In order to simplify the discussion of the method and apparatus for developing optimum values, for the stored impulse response, a problem having only two variables,  $B_0$  and  $B_1$ , will be considered. Thus assume that the following set of linear inequations in two variables is given:

$$\begin{aligned} B_0 - B_1 &\leq 1 \\ B_0 - B_1 &\geq -1 \\ B_0 + 3B_1 &\leq 15 \\ B_0 + cB_1 &\geq -15 \end{aligned}$$

In addition, assume that it is desired to maximize the function:

$$C_j = 2B_0 + B_1$$

FIG. 4 of the drawings shows graphically the statement of the problem. The shaded area indicates the region where all four constraining inequations are satisfied; hence, only values of  $B_0$  and  $B_1$  in this region are valid solutions. The dashed line shows the locus of all points for which  $C_j$ , the function to be maximized, has the value 8. Since some of these points lie in the valid region, they would be permissible solutions to the problem if there were not "better" points, also in the valid region, producing a value of  $(2B_0 + B_1)$  greater than 8. These "better" points lie on lines parallel to the dashed line at distance farther from the origin. In fact, the line passing through a vertex P will yield the maximum value for  $C_j = (2B_0 + B_1)$ . Hence, the solution will be  $B_0 = 4.5$ ,  $B_1 = 3.5$ , and  $C_j = 12.5$ .

Of course, for problems of more than two variables, the optimum solution is no longer pictorially evident because of its higher dimensionality. However, in these cases the problem is similarly solved by searching for a vertex of the valid region (which would then be a convex polyhedron in a multidimensional Euclidian space) through which the locus of points satisfying the function to be optimized may be passed to produce the optimum values for the impulse response variables.

An analog computation for solving such a linear programming problem in its simplest form involves investigating each constraining inequation for satisfaction, starting with some arbitrarily selected set of values for the variables. For those inequalities which are satisfied no correction is made on the existing values of the variables; for those which are not satisfied a correction is made which changes the variables toward decreasing the non-satisfaction. Eventually, all constraints will be satisfied but the values of the variables at this time would generally not be optimum. For this reason, changes are also included in the variables which tend to force them in a direction toward optimizing the desired function, at the same time forcing them toward satisfying all constraints.

Assume a poor first guess,  $B_0 = -13$ ,  $B_1 = -4$ , as shown in FIG. 4 of the drawings. The following two constraints are not satisfied:

$$\begin{aligned} B_0 - B_1 &\geq -1 \\ B_0 + 3B_1 &\geq -15 \end{aligned}$$

If equal importance is attached to satisfying all constraints, changes are made in a direction to improve the nonsatisfaction of each of the above two constraints by changing them at the same rate. FIG. 4 shows the path (broken line) which is taken in order to reach the region where all constraints are satisfied. Once point "O" is reached, no further change takes place. If at the same time maximization of  $(2B_0 + B_1)$  is considered, then the path shown as a solid line is taken until point P is reached. If it is considered more important to satisfy particular constraints or to reach the valid region as soon as possible, the appropriate rates of change can be weighted for these purposes.

FIG. 3 of the drawings shows an analog computing arrangement using conventional components which may be used to instrument the problem illustrated by FIG. 4. Electrical signals representing the variables  $B_0$  and  $B_1$  appear at the outputs of summing integrators 80 and 81 respectively. The signal appearing at the output of integrator 81 is also passed through an inverting amplifier 82 which delivers a signal representative of  $-B_1$ . A battery 83 provides a source of a positive unit reference voltage and battery 84 constitutes a source of a negative unit reference voltage.

The combination of an integrator 85, switch 86, and diode 94, form a source of a decreasing, maximizing potential. Initially, switch 86 is in the upper position to apply a reference potential to the integrator 85, thereby establishing an initial condition. When switch 86 is moved to the lower position, the potential from battery 84 causes the output voltage from integrator 85 to decrease until it is finally clamped at zero by diode 94.

The computer shown in FIG. 3 includes four summing amplifiers, 87, 88, 89 and 90, each of which handles one of the constraining inequalities. Summing amplifier 87, like the other four amplifiers, is provided with three input conductors. A first one of these inputs is connected to the output of integrator 80 by means of a multiplying network 91. The second input to summing amplifier 87 is connected to the output of the inverting amplifier 82 by means of the multiplying network 92. The third input to summing amplifier 87 is connected to the source of the negative unit reference potential 84 through multiplying network 93. All three of the multiplying networks 91, 92 and 93 are adjusted such that they present equal signal attenuations relative to one another. Accordingly, a signal appears at the output of the summing amplifier 87 which is representative of the quantity  $(B_0 - B_1 - 1)$ .

The output of summing amplifier 87 is connected through a resistance 95 to the input of a high gain, inverting amplifier 96. A diode 97 is connected between the input and output of amplifier 96 and is poled in a direction to allow positive current flow from the output to the input of amplifier 96. A second feedback path around amplifier 96 comprises a diode 98 connected in series with source 99. The diode 98 is poled to allow positive current flow from the input to the output of amplifier 96. The combination of the amplifier 96 and its two associated feedback paths form a switching arrangement of the type commonly used in analog computing systems. Whenever a negative input is applied to the input of amplifier 96, a zero voltage is delivered to its output conductor 100. When a positive voltage is applied, the diode 98 is forward biased and a negative potential equal to the potential delivered by source 99 is delivered to conductor 100. Consequently, conductor 100 receives a negative voltage only when the quantity  $(B_0 - B_1 - 1)$  is greater than zero. Accordingly, it may be seen that conductor 100 receives a negative potential whenever the following inequation is not satisfied:

$$B_0 - B_1 \leq 1$$

The three inputs to each of the remaining summing amplifiers 88, 89, and 90 are "programmed" by the same method used for summing amplifier 87. The amplifier 88 is connected to deliver an output representative of the quantity

$$(B_0 - B_1 + 1)$$

The output of amplifier 88 is then connected to a switching arrangement which includes the high gain, inverting amplifier 102 to whose output is connected to conductor 103. The conductor 103 accordingly receives a positive voltage whenever the variables  $B_0$  and  $B_1$  fail to satisfy the following relation:

$$B_0 - B_1 \geq -1$$



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The inputs to the summing amplifier 89 are programmed such that a voltage representing the quantity

$$(B_0 + 3B_1 - 15)$$

appears at the output of amplifier 89. A switching arrangement including amplifier 105 is connected to the output of the summing amplifier 89 such that conductor 106 receives a negative potential whenever nonsatisfaction exists for the following inequality:

$$B_0 + 3B_1 \leq 15$$

The inputs to the summing amplifier 90 are connected such that a potential representing the quantity

$$(B_0 + 3B_1 + 15)$$

appears at its output. The switching arrangement which includes the high gain, inverting amplifier 108 delivers a positive voltage to conductor 109 when, and only when, the following inequation is not satisfied.

$$B_0 + 3B_1 \geq -15$$

As discussed previously, for those inequations which are satisfied no correction is to be made on the existing values of the variables; however, for those which are not satisfied a correction is made which changes the variables toward decreasing the nonsatisfaction. Thus, when the inequality,  $(B_0 - B_1) \leq 1$ , is not satisfied, the variables  $B_0$  and  $B_1$  should be decreased and increased respectively at the same rate. Thus, the minus voltage appearing on conductor 100 when this equality is not satisfied is applied through a multiplying network having a relative coefficient attenuation of  $+0.7$  to the input of the integrator 80. This negative voltage on conductor 100 is also applied to the input of the integrator 81 through a coefficient multiplying network having a value  $-0.7$  (so that the net positive voltage is applied). Similarly, the voltages on conductors 103, 106 and 109 are connected to the inputs of the two integrators 80 and 81 to provide appropriate changes in the variables whenever selected ones of the remaining three inequations are nonsatisfied.

Provision is also made for including changes in the variables which tend to force them in a direction toward optimizing a desired function. Since, in the example given, it is desired to maximize the quantity  $(2B_0 + B_1)$ , the variable  $B_1$  is made to increase at a rate equal to half the rate of increase for  $B_0$  when all of the inequations have been satisfied. In order to insure stability, the variables' propensity for maximizing the desired function should not be allowed to outweigh the forces which tend to satisfy the inequations. Otherwise, the changes toward maximization might pull the variables outside the range of satisfaction and thus yield an incorrect solution. To insure stability, therefore, means are provided for steadily decreasing the maximizing potentials over a period which is long in comparison to the expected solution time. The output of the integrator 85 provides this source of decreasing potential. Before solution is started, the switch 86 is held in the upper position to establish an initial output condition from the integrator 85. When the switch 86 is moved to the lower position, the output voltage from integrator 85 decreases in a linear fashion until zero output potential is reached. At this time, the clamping diode 94 becomes forward-biased thereby arresting any further decrease in output potential.

The two variables are made to change at their proper respective rates by connecting the output of integrator 85 to the inputs of the integrators through appropriately adjusted potentiometers. Since variable  $B_0$ , to achieve maximization, should increase at twice the rate of variable  $B_1$ , the maximizing input to integrator 81 is connected to the output of integrator 85 through a multiplying network having a coefficient of  $+0.3$  while integrator 80 is connected through a multiplier having a  $+0.6$  coefficient.

The computational scheme described above is, of

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course, subject to a variety of design modifications which will be apparent to those skilled in the art. A description of further design techniques is contained in the article, "Linear Programming on an Electronic Analogy Computer," by I. B. Payne appearing in volume 75, Part I, Transactions of the A.I.E.E., Communications and Electronics, pp. 139-143 (1956).

As discussed previously with regard to FIG. 4 of the drawings, the computer shown in FIG. 3 will eventually find those values of  $B_0$  and  $B_1$  for which all of the constraining inequations are satisfied and for which the maximum permissible value for the function to be optimized exists. When this solution is achieved it then becomes possible to encode each of the variables into digital form and to distribute the digital words representing the solutions to the problem into the digital memory of FIG. 2 of the drawings. For this purpose, as shown in FIG. 3, the output of the integrating amplifier 80 is connected to one input of a transmission gate 111 while the output from integrating amplifier 81 is connected to one input of a transmission gate 112. Other variables whose values would be computed in an enlarged computer would be delivered in a similar manner to the inputs of other transmission gates as illustrated by the broken-line AND gate 113. The other input to each of these AND gates is connected to a synchronization generator 115 which delivers the variable in their analog form one after another to an analog-to-digital encoder 116. The encoder 116 converts the analog signals representing the solutions to the variables into digital form and delivers these digital signals to the distribution circuit 117. Distribution circuit 117 then distributes each encoded word to the proper one of the shift registers in the digital memory 24 as shown in FIG. 2 of the drawings.

During the period when digital information from the distribution circuit 117 is being stored in the registers 44, 45, and 46, the switches 70 shown in FIG. 2 are in their upper position as previously discussed. The information from the computer having been fed into the digital memory 24, the artificial network is then ready to begin operation as contemplated by the invention. Thus it is seen that the use of the optimizing computer in combination with the digital memory and digital multipliers provides an extremely versatile artificial network capable of optimum performance with minimum component expense.

#### Automatic transmission path equalization

As described earlier, the "artificial transfer network" according to the invention is particularly well adapted for use in equalizing transmission channels. In accordance with another feature of the invention, the optimizing computer may be automatically programmed in response to a test signal sent over the path to be equalized. FIG. 11 of the drawings illustrates such an automatic transmission path equalizing system in block diagram form.

FIG. 11 shows a transmission channel 120 having a transmitting terminal and a receiving terminal. A test signal generator 121 is connected to the transmitting terminal of channel 120 by means of a switch 122. The equipment at the receiving terminal of channel 120 includes an analog-to-digital encoder 21, a digital multiplier 23, a digital memory 24, a computer 25', and a decoder 26. These components are connected and perform in the same manner as discussed earlier with regard to FIG. 1 of the drawings. The computer 25', however, is a modification of the computer 25 shown in FIG. 1 and may be automatically programmed.

Also shown in FIG. 11 is a preset circuit 125. It is the function of the preset circuit 125 to provide appropriate digital data to the computer 25' so that it may be automatically programmed in accordance with the response of the transmission channel 120 to a test signal generated by the signal generator 121. One input conductor 126 of preset circuit 125 is connected to the



transmission path 120 while a second input conductor 127 connects preset circuit 125 to the output of encoder 21. Path 128 connects the preset circuit 125 to the computer 25'. The details and operation of the preset circuit 125 will be discussed below with regard to FIG. 13 of the drawings.

FIG. 12A illustrates the waveform produced by the test signal generator 121. This waveform comprises an initial single frequency test tone useful for synchronizing the preset circuitry 125 followed by a single test pulse. The test pulse is separated from the preliminary timing tone by a sufficient time interval to insure that the effects produced by the tone have completely died away by the time the test pulse appears. FIG. 12B of the drawings shows a waveform typical of the type which might appear at the receiving terminal of the channel in response to the application of the generated testing signal. The response to the test pulse, since it is isolated in time from the synchronizing tone, indicates the response of the transmission facility to the single test pulse only. Although no particular shape of test pulse is required, it is important that the testing pulse generated has at least a finite frequency content throughout the band of interest. To equalize pulse-type data transmission facilities, the test pulse may well take the form of one of those pulse signals ordinarily transmitted over the channel to be equalized.

As will be remembered from the previous description, it is desirable to equalize the channel 120 in a manner such that the test response signal received is translated by the equalizer back into the form of the test produced by the generator 121. In terms of polynomials, the sample series of the test response, when multiplied times the polynomial stored in the memory 24, should produce an output polynomial representative of the sample values of the original test signal. As will be seen, the digital sample values of the test response may be employed to automatically preset the weighting potentiometers in the computer 25'.

FIG. 13 of the drawings illustrates the preset circuit 125 in more detail and also shows the manner in which preset circuit 125 is interconnected with the computer 25'. The initial, single frequency test tone which appears at the receiving terminal of transmission line 120 (as shown in FIG. 12B) is applied through input conductor 126 to the input of an amplifier 129. The frequency of the test tone is not critical, the only requirement being that it is transmittable over the unequalized facility. The output of amplifier 129 is applied across a "servo-operated" potentiometer 130. The output signal from potentiometer 130 is, in turn, fed to the input of a peak detector 131. One input of a differential amplifier 132 is connected to the output of peak detector 131 through one pole of double pole switch 133, the other input to the amplifier 132 being connected to reference voltage source 134. As shown in FIG. 13, the output of amplifier 132 is connected through the other pole of switch 133 to control the servomechanism of potentiometer 130.

The double-pole switch 133 is arranged such that when the connection between peak detector 131 and amplifier 132 is broken, the connection between amplifier 132 and the servomechanism of the potentiometer 132 is also broken. At the same time, connection of the output of peak detector 131 is transferred to the input of a threshold circuit 135 and to one input of AND gate 136. Signals appearing at the output of the threshold circuit 135 are applied to the inputs of three delay circuits 137, 138 and 139. The output of delay circuit 137 is connected to the "set" input of a flip-flop circuit 140 while the "reset" input of flip-flop 140 is connected to the output of delay circuit 138. The output signals from delay circuit 138 are also applied to the "set" input of another flip-flop 141, the "reset" input to flip-flop 141 being connected to the output of delay circuit 139. Output signals from

the flip-flop 140 are applied to the second input of AND gate 136 and an alarm device 142 is connected to the output of AND gate 136. The conductor 127, which supplies coded sample signals from the encoder 21 as shown in FIG. 11, is connected through a transmission gate 143 to the word distribution circuit 144, the gate 143 being controlled by signals from flip-flop 141.

The preset circuit 125 distributes the digital sample values of the test response so that each sample value may be used to preset the appropriate weighting potentiometers in the computer 25'. To accomplish this function, it is necessary to provide means capable of indicating the time at which the test response signal will appear at the receiving terminal of the transmission path. The preset circuit 125, operating in response to the preliminary single frequency test tone which is received as shown in FIG. 12B, provides the necessary time marking signal.

The preset circuit 125 first determines the normal level of the preliminary test tone envelope and then generates a time mark signal at the time  $t_0$  when the test tone envelope falls below a predetermined trigger level. As shown in FIG. 12B, the trigger level may conveniently be set at half the amplitude of the normal level. The test signal generator 121 shown in FIG. 11 produces a test tone which, at a time preceding the test pulse by a predetermined duration, drops in amplitude at a sufficiently slow rate that the test tone envelope suffers no significant distortion during transmission over the still unequalized transmission facility.

The preliminary test tone as received is applied through conductor 126 to the input of amplifier 129. Amplifier 129 may include a tuned circuit resonant at the test tone frequency in order to reduce noise signals. However, such a tuned circuit should be of sufficiently low "Q" to pass the tone envelope without distortion. The amplified test tone from amplifier 129 is then applied across the servo-operated potentiometer 130. Peak detector 131 develops a rectified signal having a waveshape like that of the tone envelope and delivers this signal to one input of differential amplifier 132. Amplifier 132 produces an output signal representative of the difference between the amplitude of the test tone envelope and the reference amplitude from source 134 and delivers the difference signal to change the position of the movable tap on potentiometer 130 such that, regardless of the amplitude attenuation suffered by the tone during transmission, the tone amplitude as it appears at the output of the automatic potentiometer 130 is always the same. It should be noted that the automatic gain control device just described is only an example of one of the many ways for referencing the received signal which are known to the art.

After the appropriate level has been found by the servomechanism associated with potentiometer 130, the switch 133 is moved to its lower position, disabling the potentiometer from further movement and applying the now referenced test tone to threshold device 135. If desired, the switch 133 may be actuated in response to a zero signal from differential amplifier 132. When the test tone envelope falls below the trigger level as shown in FIG. 12B, the threshold circuit 135 generates a time marking pulse and applies this pulse to the inputs of the three delay networks 137, 138 and 139.

Delay circuit 137 has the shortest delay time,  $\Delta_1$ , seconds, so that the pulse appears again first at the "set" input of flip-flop 140, causing it to deliver an output signal at the time  $(t_0 + \Delta_1)$  as shown in FIG. 12B. At this time, at least one input to AND gate 136 is energized. Should the other input to gate 136 be energized (by a noise burst occurring on the transmission line, for example), the gate 136 will actuate the alarm 142 to notify the testing personnel that a trouble condition exists. In this manner, the transmission line continues to be monitored for spurious signals until the test response is about to begin at time  $(t_0 + \Delta_2)$  as shown in FIG. 12B. At that moment,



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the time marking pulse appears at the output of delay network 138, resetting the flip-flop 140 and turning ON the flip-flop 141. The signal from flip-flop 141 energizes transmission gate 143, allowing the coded signals from encoder 21 to be gated into the word distribution circuit 144. At time  $(t_0 + \Delta_3)$ , when the test response signal has passed, the marking pulse appears at the output of delay network 139, resetting flip-flop 141.

The encoder 21 shown in FIG. 11 continuously samples and encodes the incoming signal, thereby producing a binary series of numbers which represent the sample values of the incoming pulse train. Transmission gate 143 allows the appropriate sample values of the test response to be delivered to the word distribution circuit 144. The distribution circuit 144 separates the encoded signal on a word-by-word basis, delivering each word (or sample) to a separate output conductor in the set of conductors 128. Thus, the first sample of the test response,  $A_0$ , is delivered in digital form to the uppermost output conductor. The second sample,  $A_1$ , in a similar manner, is delivered to the second output conductor, and so on.

It will, of course, be remembered that encoder 21 may well be adapted to deliver the output sample words in parallel; that is, each digit appearing on a separate conductor from the encoder. Thus, the output conductors in the set 128 in practice may each comprise a plurality of conductors where it is desired to continue to handle these sample words on a parallel basis.

FIG. 13 shows only a portion of the computer 25' in order to illustrate the manner in which the impulse response data may be used to automatically preset the interconnected weighting potentiometers. For illustrative purposes therefore, there is shown only the apparatus for handling the following single inequation:

$$A_1 B_0 + A_0 B_1 \leq r$$

the remaining inequations are automatically programmed in the same manner. The apparatus shown in FIG. 13 includes a pair of integrators 145 and 146 (analogous to integrators 80 and 81 as shown in the more detailed FIG. 3) which deliver signals representative of the variables  $B_1$  and  $B_0$ , respectively. The output of integrator 145 is connected through the weighting potentiometer 148 to one input of the summing amplifier 150 (similar to amplifier 87 of FIG. 3, for example). Similarly, the output of integrator 146 is connected through a weighting potentiometer 151 to another input of the summing amplifier 150. The output of summing amplifier 150 is directly connected to a threshold detector 155 which is like the threshold device 102 of FIG. 3. Threshold detector 155 delivers a signal to conductor 157 whenever the inequation  $A_1 B_0 + A_0 B_1 \leq r$  is unsatisfied; that is, whenever the sum of the signals applied to the inputs of amplifier 150 is greater than the arbitrarily selected reference quantity " $r$ ." The signal from conductor 157 is applied to the input of integrator 145 through weighting potentiometer 158 and to the input of integrator 146 through the weighting potentiometer 159.

For the reasons discussed in regard to FIGS. 3 and 4 of the drawings, the weighting potentiometers 148 and 158 should be set to a value representative of the amplitude quantity  $A_0$ . This quantity represents the amplitude of the first sample and appears in digital form on the uppermost output conductor 128 from the distribution circuit 144. Similarly, the potentiometers 159 and 151 are to be set in accordance with the value  $A_1$  which appears in digital form on output conductor second from the top in set 128. Many schemes are known to the art for providing a setting on a potentiometer in accordance with coded signals. Typical among these digital potentiometers is that shown by W. W. Fisher et al. in their U.S. Patent 2,782,408, issued Feb. 19, 1957. Another scheme is shown in FIG. 14 of the drawings. As shown, four logarithmically related resistors are connected in series and each may be shunted whenever the

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associated electromagnetic relay is actuated. Thus, digital signals applied to the conductors 161 may be converted into a value of resistance between terminals 162 and 163 which is representative of the value of the digital "word." Such a scheme may be used to instrument potentiometers 148, 151, 158, and 159 shown in FIG. 13.

It will be apparent from the description above that the preset circuitry 125 and the computer 25' may be disconnected from the remaining portion of the circuit once the appropriate information has been stored in the digital memory 24. Accordingly, it will be possible for the computer and preset circuitry to be employed in equalizing a large number of transmission channels leaving the memory, multiplier, coding and decoding circuits to do the work once the information storage has been accomplished.

It is to be understood that the arrangements which have been described are illustrative of the application of the principles of the invention. Numerous other arrangements may be devised by those skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. Apparatus for synthesizing a network having a desired impulse response which comprises, in combination with a source of a time varying input signal, means for sampling and encoding said signal to form a first series of binarily expressed numbers, a digital memory, means for storing in said memory a second series of binarily expressed numbers, said second series being composed of a fixed number of terms representative of the sample values of an impulse response which approximates said desired impulse response, means for multiplying together said first and said second series to form the polynomial product thereof, and means for translating said product into an output signal.

2. An artificial network having input and output terminals and having an actual transfer characteristic which closely approximates a desired transfer characteristic, said desired transfer characteristic being defined as the relationship between a selected known input waveform and a desired output waveform, said artificial network comprising, in combination with a source of a time varying signal connected to said input terminal, means for sampling said signal and encoding each sample to form a first series of binarily expressed numbers, a digital memory for storing a second series of binarily expressed numbers, said second series of numbers being composed of a limited number of terms the value of each of which is selected such that when said second series of numbers is multiplied times the sample values of said known input waveform a polynomial product is produced which most nearly approximates the sample values of said desired output waveform, means for multiplying said first series from said sampling and encoding means times said second series from said memory to form a third series of binarily expressed numbers, and means for translating said third series into an analog output signal.

3. Apparatus as set forth in claim 2 wherein said means for multiplying together said first and second series comprises, in combination, means for storing a first binarily expressed number from said first series in a first shift register, a series of memory units each of which stores a binarily expressed number in said second series, an AND-gate multiplying matrix for cross-connecting each stage of said first shift register with the output of each of said memory units, accumulator means connected to said matrix for simultaneously storing the first series of subproducts formed by multiplying said first number times each of the numbers in said second series, means for storing a second number from said first series in said first register, and means for shifting said first series of subproducts within said accumulator means and adding said first series of subproducts to a second series of subproducts formed by said second number.

4. Apparatus for equalizing an electrical transmission



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path which comprises, in combination, means at the transmitting end of said path for generating a short duration testing signal having a frequency spectrum of finite value throughout a selected band of interest, means for passing said testing signal over said transmission path, means for sampling and encoding said signal as distorted by said path to form a first polynomial series of binary numbers, means for developing a second polynomial series of numbers which most nearly approximates the inverse of said first series, a binary memory, means for storing said second series in binary form in said memory, means for multiplying said second series of numbers stored in said memory times the sample values of incoming signals as they are received from said path to form a product series, and means for decoding said product series.

5. Apparatus as set forth in claim 4 wherein said means for developing said second series of numbers comprises, in combination, an analog computer adapted to automatically converge to an optimal solution for a prob-

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lem having  $k$  variables and a greater number of restrictions, said restrictions being electrically defined within said computer by means of settings on a plurality of potentiometers, means for adjusting the settings on said potentiometers in accordance with the values of said numbers in said first series, and means responsive to said computer for generating said second series of numbers wherein each term is representative of the optimal solution of respective ones of said  $k$  variables.

#### References Cited by the Examiner

##### UNITED STATES PATENTS

|           |        |                     |           |
|-----------|--------|---------------------|-----------|
| 2,763,721 | 9/1956 | Hansell et al. .... | 328—163 X |
| 3,242,462 | 3/1966 | Funk et al. ....    | 340—146.1 |
| 3,252,099 | 5/1966 | Dodd .....          | 328—164 X |

ARTHUR GAUSS, *Primary Examiner*.

J. JORDAN, *Assistant Examiner*.