

Sept. 20, 1966

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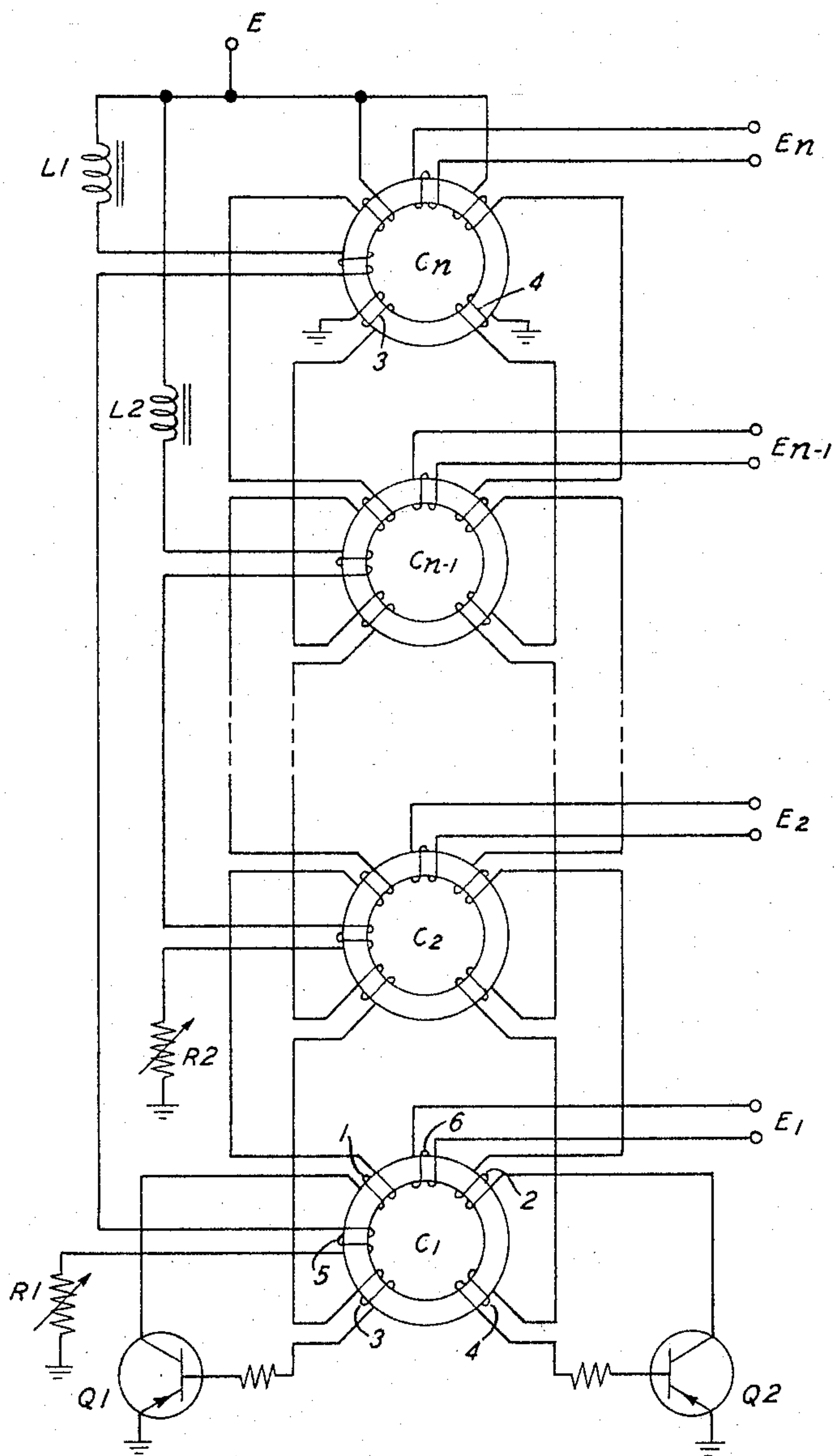
3,274,396

MULTI-WAVEFORM GENERATOR

Filed May 16, 1962

3 Sheets-Sheet 1

FIG. 1



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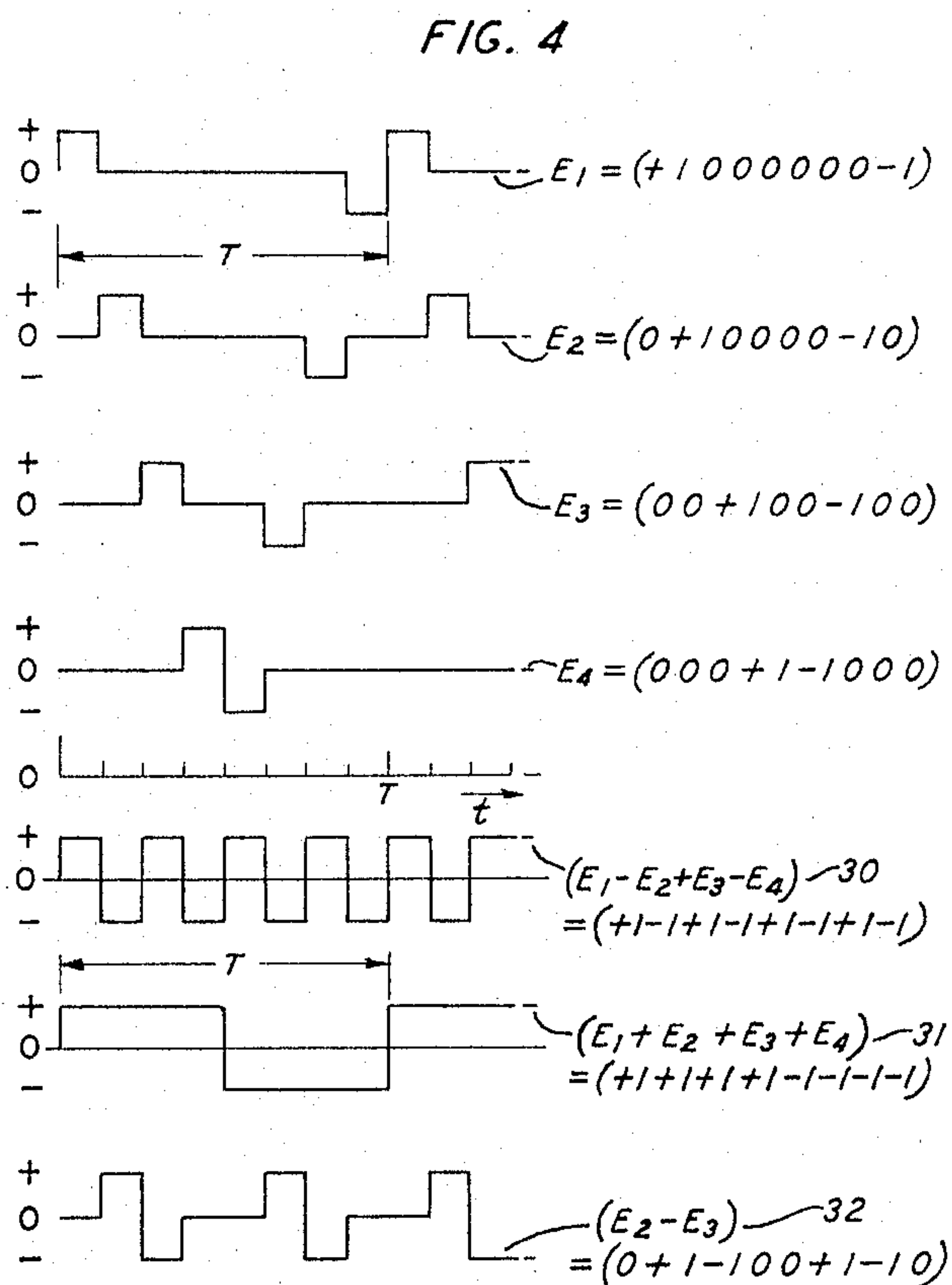
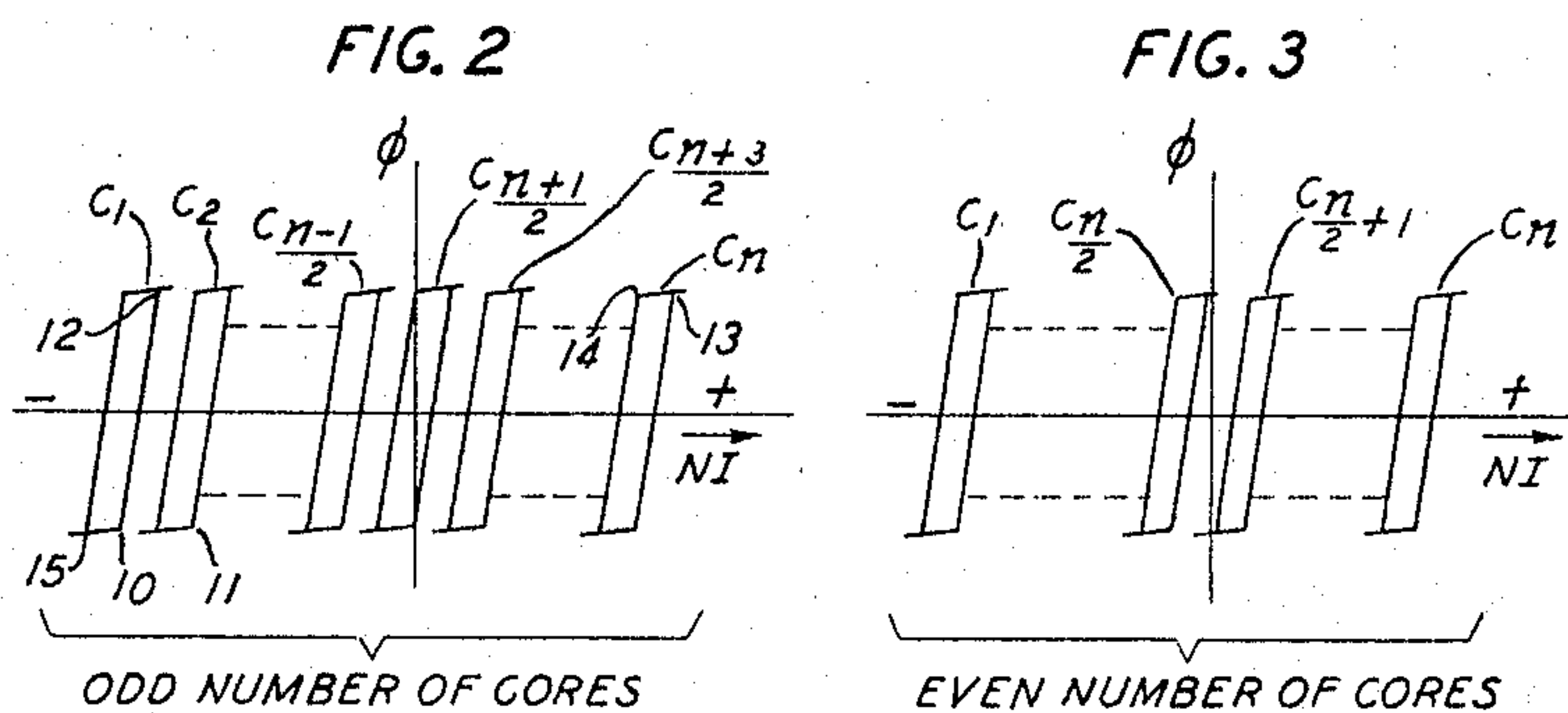
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FIG. 5

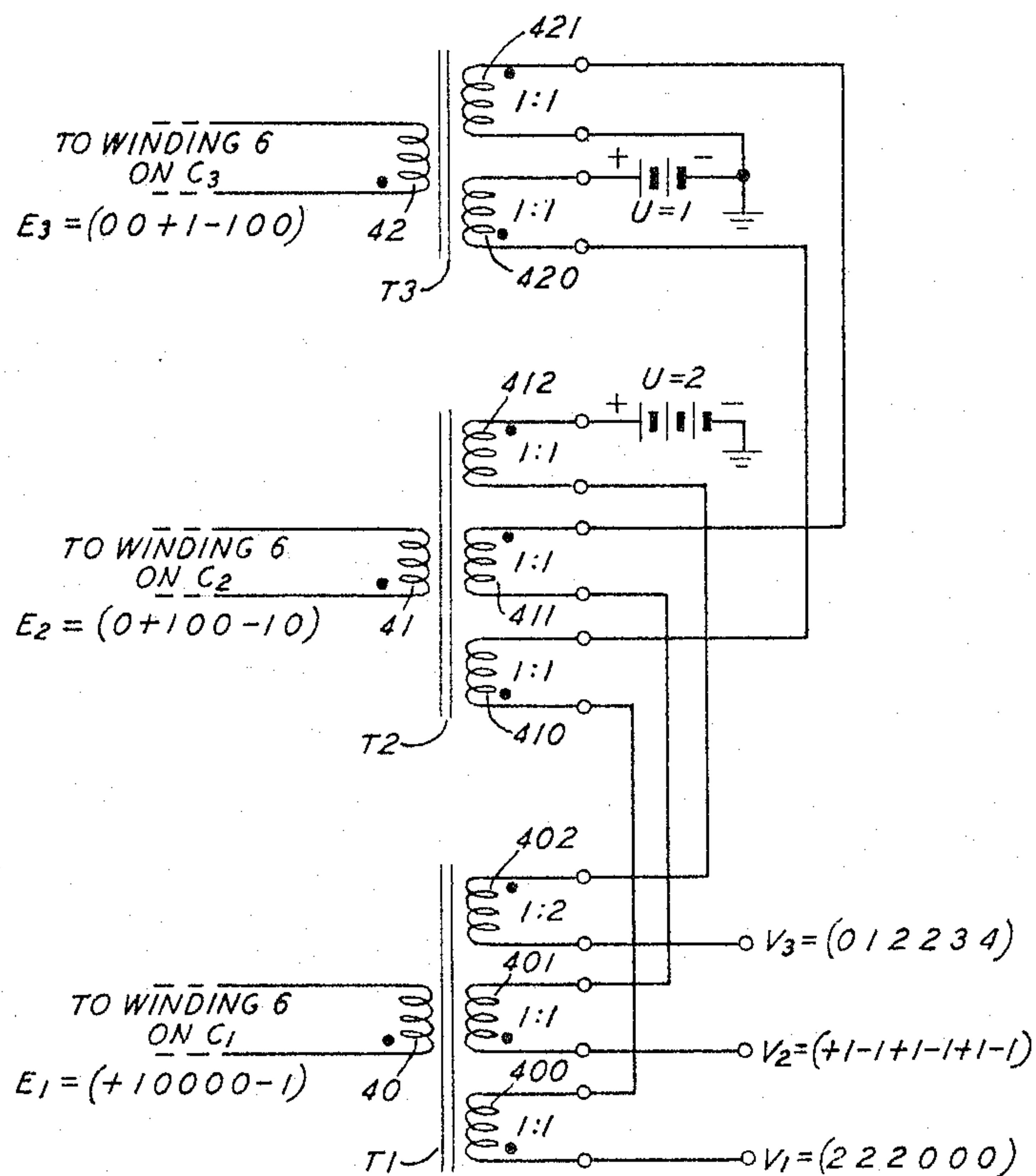
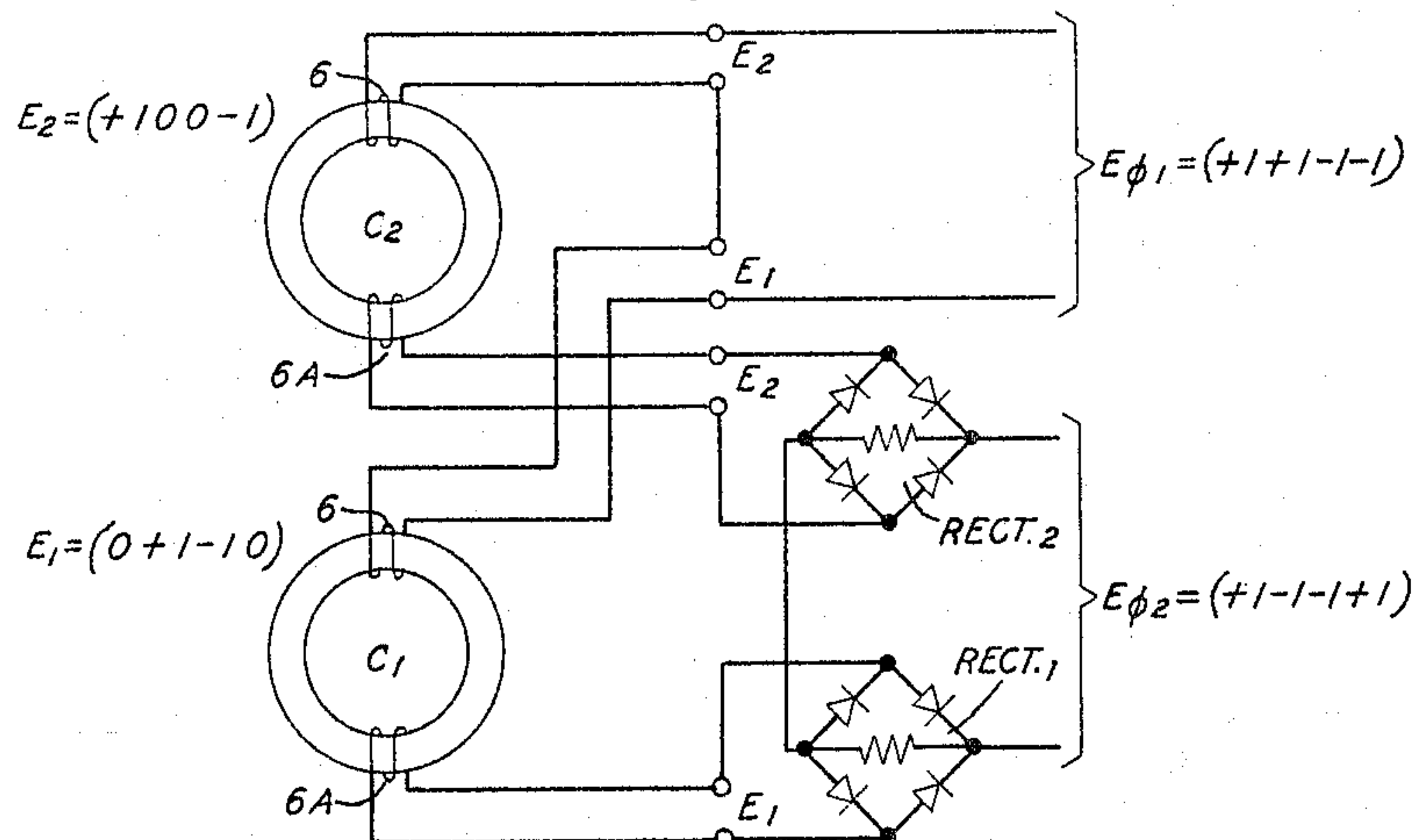


FIG. 6



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MULTI-WAVEFORM GENERATOR

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This invention relates to waveform generators and more particularly to a multi-waveform generator capable of simultaneously producing a plurality of independent waveforms.

Many different types of relaxation oscillators have been known in the prior art and these produce a variety of different waveforms which are useful for many different purposes. Few of these oscillators are capable of simultaneously producing more than a very limited number of waveforms and in most cases only a single waveform. Therefore, each of these oscillators is of a specialized type. It is desirable that a single generator be capable of producing a great variety of waveforms and such a generator may be termed a multi-waveform generator. By this term is meant a generator which is capable of producing a large number of waveform types such as the square, rectangular and the staircase waveforms.

It is an object of this invention to simultaneously generate a plurality of independent waveforms in fixed time relationship with respect to each other.

The foregoing object is achieved by this invention which comprises a multi-waveform generator of the relaxation oscillator type in which is included a plurality of saturable magnetic cores each of which is initially biased to a different degree of saturation. As the generator alternately conducts current in each of its two current branches, the increasing current in one branch successively switches the cores from one of their saturable states to their other one. This is immediately followed by an increasing current in the other branch to successively switch the cores back again. Output windings on these cores develop voltage pulses each time the core switches. As these pulses create waves of different form but related in time they may be used either individually or combined to form various single-phase and poly-phase waveforms.

The term "saturable magnetic core" as used in this specification and in the claims has the usual connotation in that it refers to a core material, usually an alloy of nickel and iron, which has a substantially rectangular hysteresis loop of small area so that it can be readily driven from one of its two saturable states to the other by a very small change in magnetizing force.

The invention may be better understood by reference to the accompanying drawings, in which:

FIG. 1 illustrates the circuits of a preferred embodiment of this invention;

FIGS. 2 and 3 show how the several cores may be differently biased to produce hysteresis loops displaced along the exciting current axis;

FIG. 4 shows the basic waveforms produced by a generator of the type shown in FIG. 1 having four cores and some typical waveforms which may be derived therefrom;

FIG. 5 illustrates how some typical waveforms may be derived from a three-core generator; and

FIG. 6 is illustrative of connections for obtaining a two-phase output.

Referring now to FIG. 1, it will be noted that the circuit embodies an oscillator of the relaxation type similar to that disclosed in FIG. 9 of an article by Johnson and Rauch, entitled "Decicycle Magnetic Amplifier System for Servos," appearing in Communications and Elec-

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tronics for Nov. 1955, p. 670. FIG. 1 differs, however, in that a plurality of cores are disclosed with a means for biasing them to different degrees of saturation and each core has its own output windings. Windings 1 and 2 of core C_1 comprise the exciting windings, windings 3 and 4 are the feedback windings, winding 5 is the bias winding and winding 6 is the output winding. The unnumbered windings of the remaining cores, similarly situated about their cores, have the same functions. It will be noted that the bias winding for cores C_1 and C_n are connected in series to a source of direct potential E through a reactor L_1 and a variable resistor R_1 , the latter providing a means for adjusting the degree of bias applied to these two cores. The directions of these bias windings are to be such that these two cores are biased to equal degrees of saturation but in opposite sense. Similarly, cores C_2 and C_{n-1} are oppositely biased to substantially equal degrees through a reactor L_2 and variable resistor R_2 . Cores which may be inserted between cores C_2 and C_{n-1} are similarly biased in opposite sense through separate inductors and variable resistors. If the generator contains an odd number of cores the centrally located core will be unbiased. The manner in which these biases are adjusted will be more particularly described in connection with FIGS. 2 and 3.

Two transistors Q_1 and Q_2 , schematically illustrated as of the PNP type, are shown with their emitters grounded. NPN type transistors may be used by merely reversing the polarity of the voltage source E . The collectors of these transistors are respectively connected in series with the exciting windings 1 and 2 of all cores and finally connected to the power source E . The base of each transistor is connected through a resistor to its feedback winding 3 or 4 and the similarly located feedback windings on the other cores and finally returned to ground as shown for core C_n in FIG. 1. FIG. 1 discloses only a single output winding 6 for core C_1 and a similar winding for each of the other cores. Actually, a plurality of such windings may be provided and they may have equal or different numbers of turns. Moreover, one or more of the windings may be tapped for selection of different voltages. These conventional alternatives have not been shown in FIG. 1 for clarity.

Before describing the operation of FIG. 1 reference may first be made to FIGS. 2 and 3 disclosing the manner of biasing the cores to different degrees of saturation. FIG. 2 discloses the manner of biasing the cores when an odd number of cores are employed. In this case, the central core $C_{(n+1)/2}$ is shown unbiased as is the case whenever an odd number of cores is used. The subscript designation for this core, namely, $(n+1)/2$ designates the number of the core where n is the number of cores used in the generator. The other designations shown for the adjacent cores will now have an obvious significance. The cores shown to the right of the central core in FIG. 2 are biased positively and those to the left are biased negatively. The vertical axis represents the flux in the cores while the horizontal axis represents the ampere-turns magnetizing force in the exciting windings of the core. Therefore, the bias applied to the cores as shown in this figure, as well as in FIG. 3, is with reference to the magnetizing force provided in the exciting windings.

FIG. 3 is similar to FIG. 2 except that it discloses the biasing arrangement for a generator having an even number of cores. In this case there is no central core so half of the cores are biased in one sense and half in the other. Here again, those cores whose loops are shown to the right of the vertical axis are positively biased while those to the left of the vertical axis are negatively biased.

The operation of this generator may now be described with FIGS. 1, 2 and 3 in mind. Assuming that the gen-

erator contains an odd number of cores, the biasing situation represented by FIG. 2 would apply. Also assume that the generator is in a state of oscillation and that transistor Q_2 has just ceased conducting after having driven the cores into negative saturation, that is to say, the negative magnetizing force provided by the collector current of transistor Q_2 has exceeded point 15 shown in FIG. 2. The action of the oscillator is now such as to cause Q_1 to start conduction so that current very rapidly increases until the magnetizing force has reached point 10 at the heel of the hysteresis curve of core C_1 . Core C_1 now suddenly becomes unsaturated and the rate of current increase is substantially linear with time as the magnetizing force increases from a value corresponding with point 10 to a value corresponding to point 12 at the knee of the curve. This results in a change in flux in core C_1 from negative saturation to positive saturation. Since core C_1 is now saturated, the flux change suddenly becomes very low in this core and consequently the current in the exciting winding increases very rapidly. In this connection it should be remembered that the inductance of saturated cores is exceedingly low while the inductance of unsaturated cores is relatively very high. The reason for the rapid increase in current when core C_1 saturates at the knee of its curve, point 12, is that the entire exciting circuit now has a very low inductance. As this current increases, it very rapidly produces a magnetizing force which corresponds to point 11 of core C_2 . The current then again increases linearly with time to switch core C_2 in the same manner just described for core C_1 . This operation continues in successive order until the magnetizing force is such as to cause the last core C_n to reach saturation at point 13. Once again, the total inductance in the circuit becomes very low and the current starts to increase rapidly. Since there is no further core in the chain to switch, core C_n is driven farther into saturation and the induced current in its feedback winding to the base of transistor Q_1 very rapidly lowers. This rapidly reduces the collector to emitter current through transistor Q_1 to bring the magnetizing force back toward point 14 of the hysteresis loop for core C_n . It will be observed that this is in such a direction as to cause a slight decrease in the total flux in the core, thereby reversing the polarities of the induced voltages in the two feedback windings 3 and 4 of core C_n . This produces two effects. First, it tends to drive Q_1 into non-conduction and secondly, it starts Q_2 toward conduction so that current now begins to flow through the emitter-collector path of transistor Q_2 and the exciting windings 2 of all the cores. This increasing current is of such a direction as to drive the magnetizing force in the negative direction with reference to FIG. 2 and consequently switch core C_n through a flux change from positive saturation to negative saturation down the left side of its hysteresis loop. The remaining cores are similarly switched in succession in the same manner previously described when the current was increasing in transistor Q_1 . The current in transistor Q_2 continues to increase until the magnetizing force it produces has finally switched core C_1 and thus restarts the cycle. It will be evident that the operation is precisely the same for a generator containing an even number of cores.

FIG. 4 is illustrative of the types of waveforms which are obtainable from a generator of the type shown in FIG. 1 constructed with four cores. It will be remembered that as one transistor is conducting each of the cores is switched once from one of its extreme saturation states to its opposite saturation state and that as the other transistor is conducting they are switched back again. Where the generator embodies four cores, this represents eight switch intervals so that a complete cycle of period T is represented by eight discrete time intervals, each of time $T/8$. In this figure, the waveforms represented by E_1 , E_2 , E_3 and E_4 are, respectively produced by cores C_1 , C_2 , C_3 and C_4 . The time axis shown directly below

the waveform E_4 shows the eight discrete time intervals for the period T . Referring now to the waveform E_1 (which is generated by core C_1) it will be noted that as transistor Q_1 starts to conduct, thereby switching cores C_1 from negative saturation to positive saturation, a voltage pulse in the positive direction is developed. This voltage pulse will be of substantially rectangular waveform and is thus shown in idealized form in FIG. 4. As core C_1 does not again switch until the eighth time interval, the output voltage E_1 will be zero for the second through the seventh intervals. During the eighth time interval it will develop a voltage in the opposite direction since the flux is now reversing in the core. Similar considerations will disclose the reasons for the waveforms shown for the remaining cores. Normalizing these voltage pulses, they may be represented by the series of eight digits shown in parentheses to the right of the four basic waveforms in FIG. 4. For the waveform of voltage E_4 , the output from core C_4 , the figures in the parentheses show the output to be zero for the first three time intervals, then +1, then -1, and finally zero for the remaining three time intervals, thereby completing the cycle. It should be understood that the actual voltages of these pulses may be of any value and that these figures represent only a normalized output.

By connecting the output terminals of the several cores shown in FIG. 1 in series, various waveforms may be derived. For example, the waveform 30 shown in FIG. 4 is obtained by connecting the four output circuits in series with the terminals for cores C_2 and C_4 reversed, i.e., connected in opposite phase. This produces a waveform having a frequency four times that of the basic oscillator frequency of the generator. The waveforms 31 and 32 are similarly obtained. However, in the case of waveform 32 the outputs of only two of the cores are used. In this case the output from cores C_2 and C_3 are connected in series with the terminals from core C_3 reversed in phase. These waveforms, drivable from the basic four waveforms of the generator, are only illustrative of some of the waveforms which may be derived.

The "staircase" waveform is particularly useful and is very difficult to derive by other means. It is readily obtainable, however, from the generator of this invention. A simple case will be described using the principles already described with reference to FIG. 4. Assuming that it is desirable to derive a staircase voltage having the waveform represented by the designation $(0 +1 +2 +3)$ for a complete cycle, the designation in the parentheses having the same significance as previously described with reference to FIG. 4. The output voltages from a two-core generator may be designated as $(+1 0 0 -1)$ and $(0 +1 -1 0)$. Here again, the voltage designations have the same significance as previously described for FIG. 4. By selecting an output voltage from the first core equal to one and one-half times the normalized value, an output from the second core equal to one-half its normalized value, adding these in series and then reversing the phase will result in a series of voltages represented by $(-1.5 -0.5 +0.5 +1.5)$. Now, by simply connecting this series circuit in series with a source of direct voltage equal to one and one-half times the normalized voltage, the desired waveform $(0 +1 +2 +3)$ is obtained.

Various methods may be employed for obtaining voltages differing from the normalized values described above. One of these methods is to simply put multi-tap output windings on the generator cores; another method is to put a plurality of windings with different numbers of turns on each core; a third method is to connect the single output winding of each core to a separate transformer to give different transformation ratios; and finally the output windings of the several cores may contain voltage dividers which may be adjusted to give the desired relative values. Such methods are conventional and require no detailed illustration. However, one of these will be specifically described with reference to FIG. 5.

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FIG. 5 discloses three transformers T_1 , T_2 and T_3 , the primary windings 40, 41 and 42 being respectively connected to the output windings 6 on cores C_1 , C_2 and C_3 of a three-core generator. Alternatively, the secondary windings for these three transformers may be made output windings on the three cores without use of the intervening transformers. The use of transformers increases the flexibility with which connections may be made. As described above, it will be evident that a three-core generator will produce voltage pulses at six discrete time intervals in one period of oscillation. The waveforms of the three output voltages from the generator are represented as voltages E_1 , E_2 and E_3 and designated by the values given in their respective parentheses. Transformers T_1 and T_2 are each shown with three secondaries and transformer T_3 with only two. This is not to be taken as in any way limiting the number of secondaries or their respective transformation ratios. The transformation ratios of all of these windings is 1:1 except for secondary 402 of transformer T_1 which steps up its primary voltage by a ratio of 1:2.

The arrangement shown in FIG. 5 is for the purpose of developing three output waveforms designated by voltages V_1 , V_2 and V_3 . Voltage V_1 , for example, is designated by (2 2 2 0 0 0). This is derivable from the output from secondary 400 of transformer T_1 , secondary 410 of transformer T_2 and secondary 420 of transformer T_3 , these secondaries all being connected in series and in like phase relative to each other. Since the transformation ratios for each of these secondaries is 1:1, the output voltage for V_1 is obtained from the generator voltages E_1 , E_2 and E_3 by simply algebraically adding these latter voltages and to this sum adding the unit voltage, $U=1$, obtained from the direct voltage source connected between the upper terminal of secondary 420 and ground. As previously described, these voltages are all normalized or unit voltages, and the actual voltages may differ considerably from the values shown. To further illustrate this addition, the three voltages from the secondaries are added to this constant voltage to derive the voltage V_1 as indicated below:

$$\begin{array}{r} E_1 = (+1 \quad 0 \quad 0 \quad 0 \quad 0 \quad -1) \\ E_2 = (\quad 0 \quad +1 \quad 0 \quad 0 \quad -1 \quad 0) \\ E_3 = (\quad 0 \quad 0 \quad +1 \quad -1 \quad 0 \quad 0) \\ U = (+1 \quad +1 \quad +1 \quad +1 \quad +1 \quad +1) \\ \hline V_1 = (+2 \quad +2 \quad +2 \quad 0 \quad 0 \quad 0) \end{array}$$

As indicated above, the desired output voltage V_1 is the algebraic sum of each time interval voltage pulse of the waveforms E_1 , E_2 , E_3 and the constant voltage U . The other two waveforms are similarly derived keeping in mind the relative polarities of the output windings as designated by the dots adjacent the secondary windings and their respective transformation ratios. In this connection it will be noted that voltage V_3 is derived from secondaries 402 and 412 each of which is connected in reverse phase with respect to the primary voltages, that the transformation ratio for core 402 is 1 to 2 and that a constant unit voltage of $U=2$ is connected in series with these two windings.

From the above description it will be quite evident that the waveform from the individual cores are each mutually independent of all others but precisely time related. By reason of this precise time relation, it is possible for the generator of this invention to develop, in addition to the single phase waveforms mentioned above, various polyphase waveforms. For example, a two-phase square wave output is derivable from a generator with two cores. One of the phases is obtained by simply connecting the output windings of the two cores in series to derive the waveform (+1 +1 -1 -1). The second phase must have a waveform 90 degrees displaced from this one so that it would be designated by (+1 -1 -1 +1), this latter waveform is again obtained from the

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outputs from the two cores but this time they must be rectified with a full wave rectifier before adding them together in series. This is illustrated in FIG. 6.

In FIG. 6, cores C_1 and C_2 are the two cores of the generator of this invention. In addition to windings 6, auxiliary output windings 6A are shown to provide isolation and to supply the input voltages for the two full wave rectifiers RECT₁ and RECT₂. The polarities of the diodes in these two rectifiers are as indicated by their symbols. It will be observed that the effect of these rectifiers is to place on the right hand output terminal of the rectifier a positive pulse with respect to the left hand terminal of the rectifier for each voltage pulse supplied by its winding 6A. By adding these rectifier pulses in the manner indicated, the desired waveform is obtained for the other phase. It will thus be noted that the direct addition of the two output windings yields the phase voltage $E_{\phi 1}$ while the waveform for the second phase $E_{\phi 2}$ is obtained from the outputs of the rectifiers RECT₁ and RECT₂.

The various waveforms shown in the several figures and described herein should be understood to be for illustrative purposes only as it will be quite apparent to those skilled in the art that a great variety of waveforms may be obtained by varying the number of cores and connecting one or more output windings in series in accordance with the principles described above. Also additional waveforms may be obtained by the addition of rectifiers and constant voltage sources, the latter being particularly described with reference to FIG. 5 as illustrative of this technique. The invention is therefore not limited to any particular manner by which these windings may be connected together to provide the various waveforms. It is also obvious that a special purpose generator can be constructed omitting output windings from those cores from which outputs are not to be taken. Where several successive cores have no output windings because of the aforesaid special purpose character of the generator, a single core can replace them by the simple expedient of increasing the number of its exciting winding turns, and hence its inductance, until the amount of time required to switch the core through its unsaturated state equals the total time required for the cores it replaces. Should it be desired to eliminate one of the two pulse polarities generated by any winding, it can be accomplished by a single diode in series with that winding, poled to pass the pulse of desired polarity and reject the undesired one.

What is claimed is:

1. A multi-waveform generator of the relaxation oscillator type comprising two circuit branches in which current repetitively flows first in one branch and then in the other one, a plurality of saturable cores each having a hysteresis characteristic such that it is capable of being switched to either of two opposite states of saturation through an unsaturated portion of said characteristic, means initially biasing a first group of said cores to different degrees of saturation in one of their two saturable states and a second group comprising an equal number of the remaining cores to different degrees of saturation in the other of their saturable states, means coupling all of said cores to said two circuit branches so that an increasing current in one of said branches successively switches all of said cores from a first one of their said states to the other one and an increasing current in the other branch successively switches all of them back again to said first state, and an output winding on at least one of said cores in which a voltage pulse is generated each time the core is switched from one saturable state to the other.

2. The combination of claim 1 in which at least one of said cores has a plurality of output windings which may have different numbers of turns to simultaneously generate different voltages.

3. The combination of claim 1 wherein said means coupling all of said cores comprises a winding on each of

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said cores connected in series with each other and one of said two circuit branches and another winding on each of said cores connected in series with each other and the other of said circuit branches.

4. The combination of claim 2 wherein said means coupling all of said cores comprises a winding on each of said cores connected in series with each other and one of said two circuit branches and another winding on each of said cores connected in series with each other and the other of said circuit branches.

5. A multi-waveform generator comprising a plurality of saturable magnetic cores, each having at least one output winding, a bias winding, a pair of exciting windings and a pair of feedback windings wound thereon, two current controlled switches each having a control circuit for alternately turning a switch on and off as the polarity of current supplied to its control circuit is reversed, means for passing a bias current through each of said bias windings to bias said cores to different degrees of saturation, circuits connecting one of the exciting windings of each core in series with each other and one of said switches and the other exciting winding of each core in series with each other and the other switch, and other circuits connecting one of the feedback windings of each core in

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series with each other and the control circuit of one switch and the other feedback winding of each core in series with each other and the control circuit of the other switch, the relative polarities of said exciting and feedback windings being such that an increase in current in the exciting windings connected to either one of said switches generates currents in the feedback windings to hold on the switch through which current is increasing and to hold off the other switch, whereby a voltage pulse is generated in the output windings of each core as it is driven through the unsaturated part of its hysteresis characteristic.

6. The combination of claim 5 wherein said current control switches are transistors.

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