

July 17, 1962

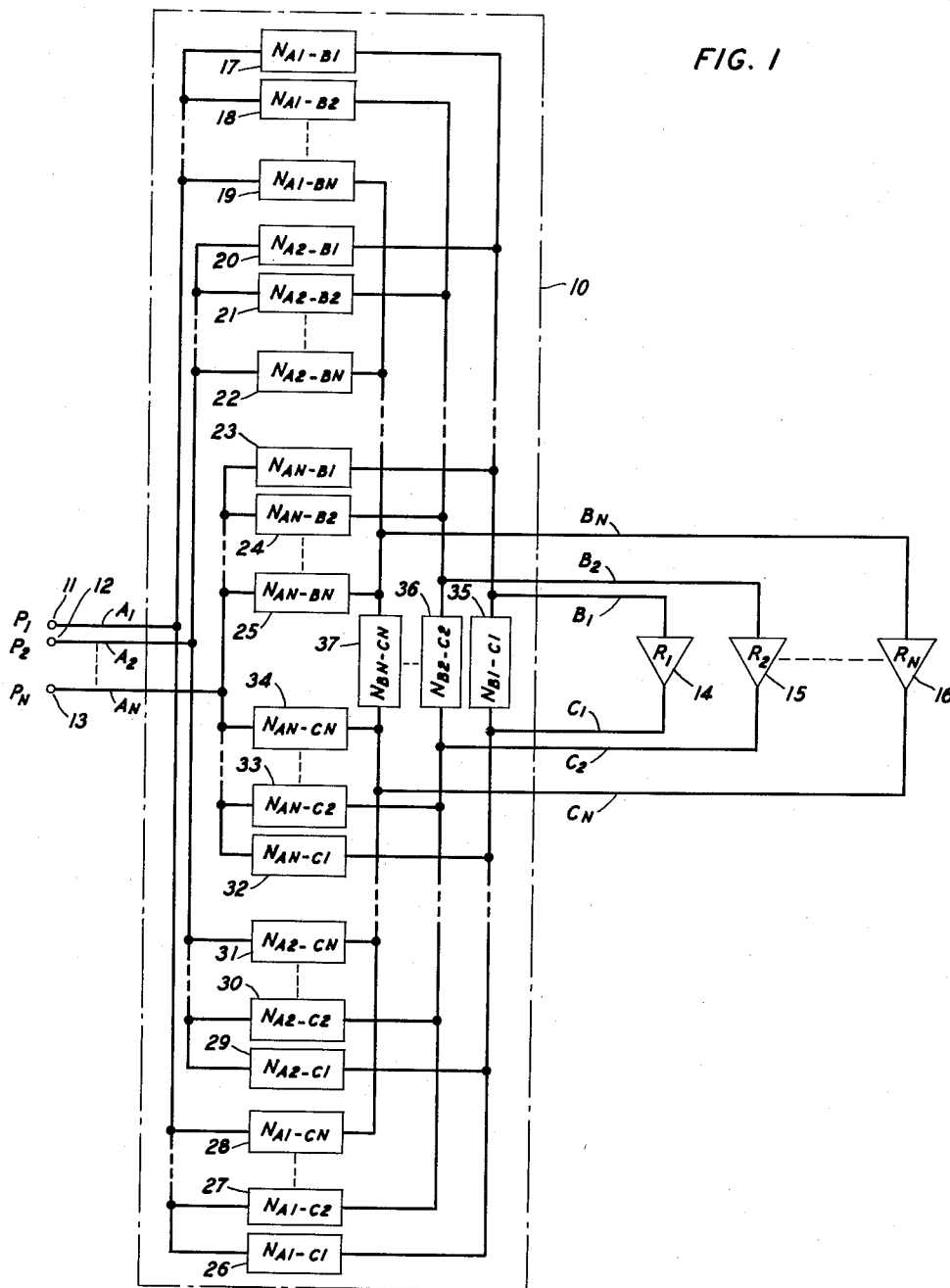
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3,045,194

ACTIVE MULTIPOINT NETWORKS

Filed Nov. 2, 1960

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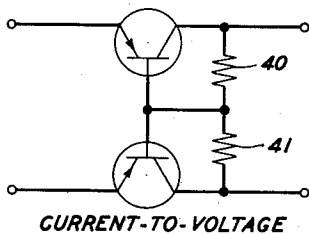
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ACTIVE MULTI-PORT NETWORKS

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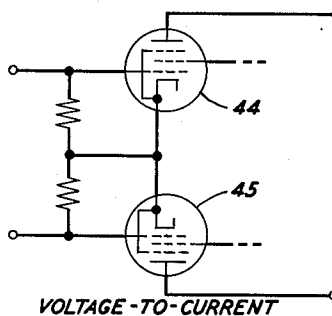
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FIG. 2A



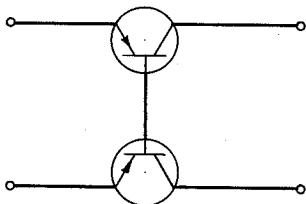
CURRENT-TO-VOLTAGE

FIG. 2B



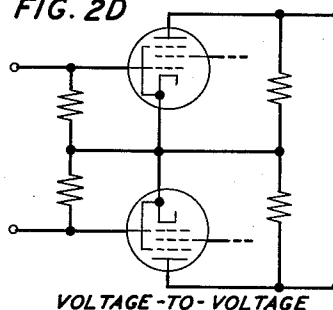
VOLTAGE-TO-CURRENT

FIG. 2C



CURRENT-TO-CURRENT

FIG. 2D



VOLTAGE-TO-VOLTAGE

FIG. 3

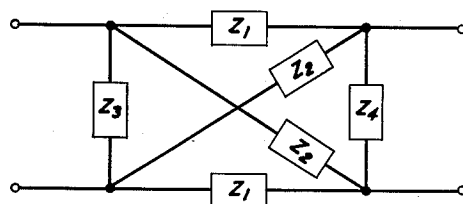


FIG. 4B

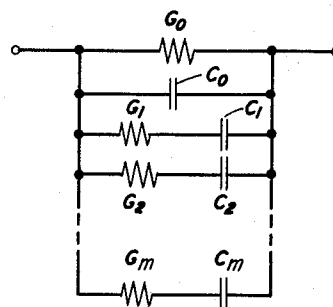
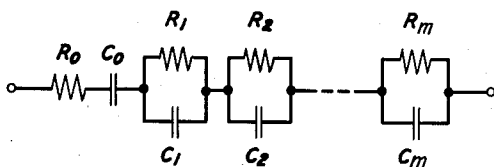


FIG. 4A



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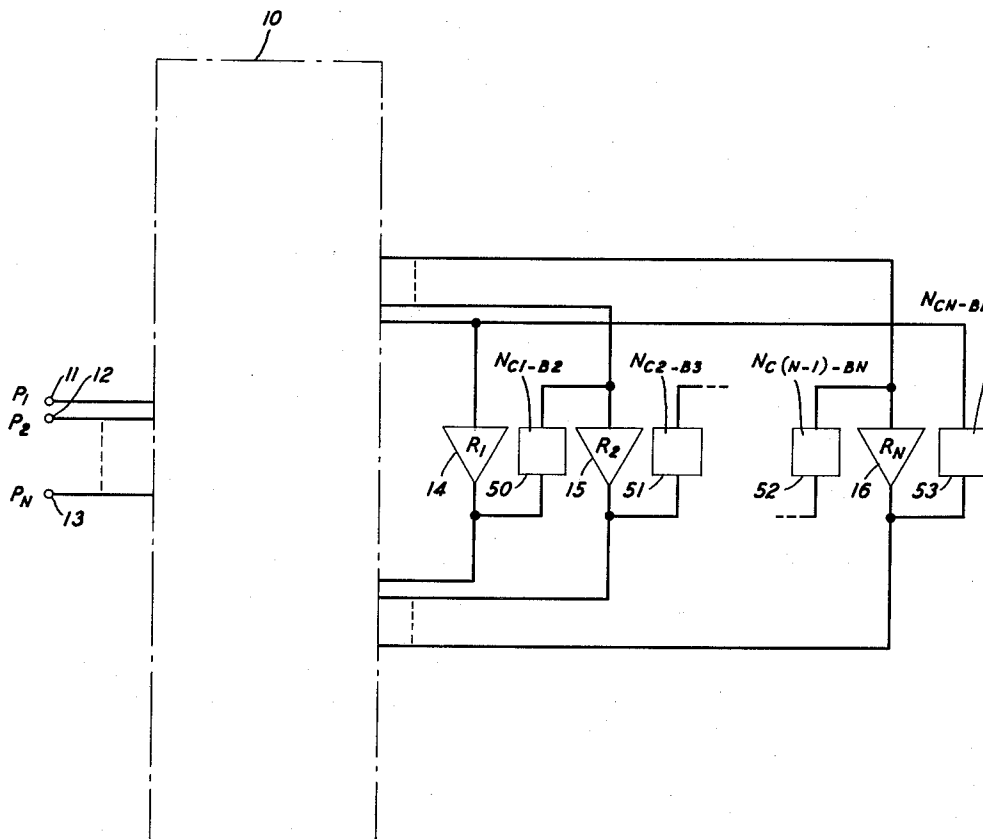
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FIG. 5



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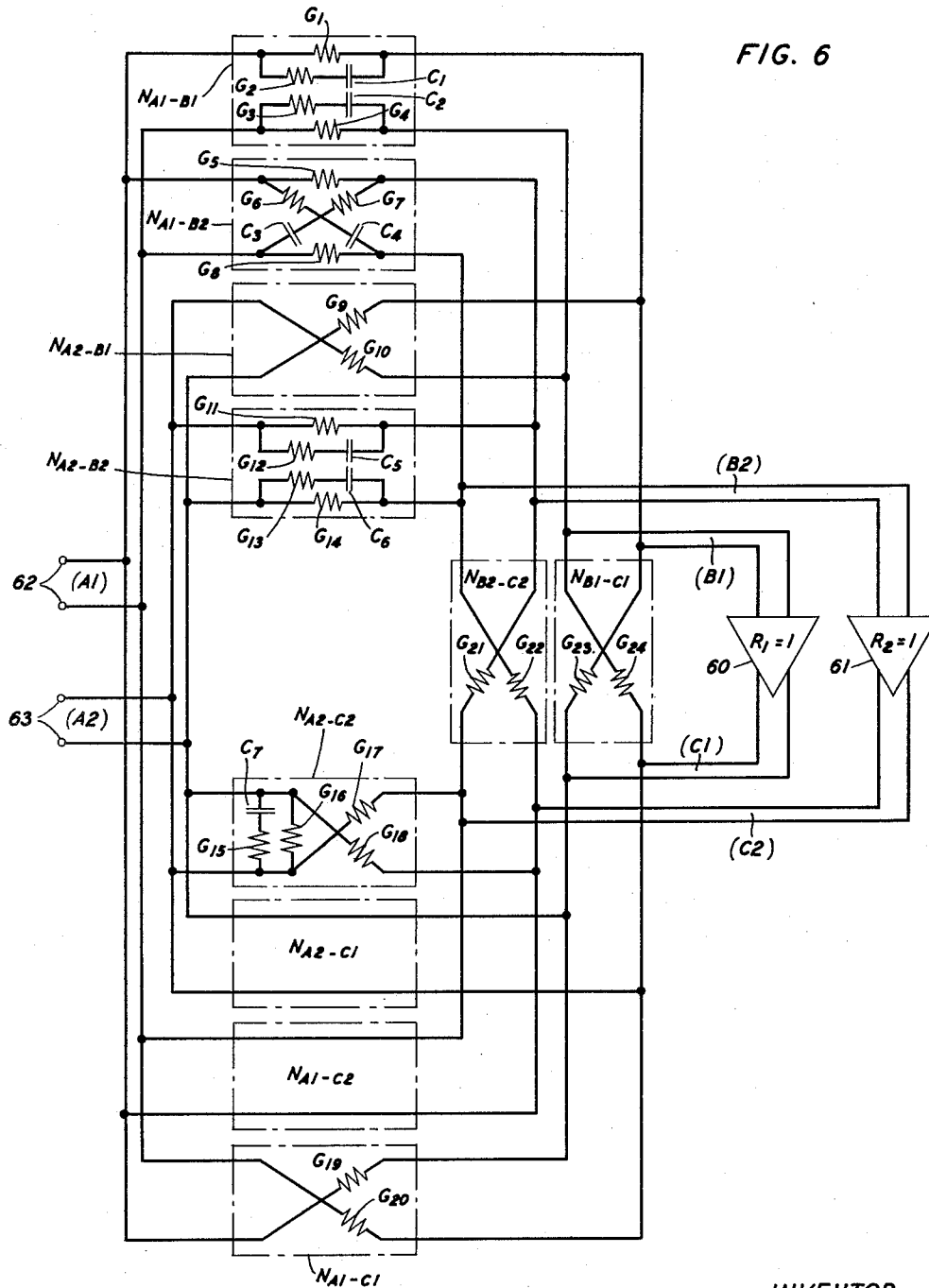


FIG. 6

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ACTIVE MULTI-PORT NETWORKS

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Filed Nov. 2, 1960, Ser. No. 66,755
16 Claims. (Cl. 333-80)

This invention relates to wave transmission networks and, more particularly, to active n -port networks without inductors in which all of the driving point and transfer parameters may be preselected without restriction.

In many signal transmission networks, it is often desirable to obtain certain driving-point and transmission parameters without the use of inductors, particularly at low frequencies. This arises from the fact that inductors at these frequencies are generally large, cumbersome, expensive, and are usually far from ideal components. Resistors and capacitors, on the other hand, are small, inexpensive, and much more nearly ideal components. A large amount of work has therefore been done in synthesizing networks having desirable parameters but having no inductors. J. G. Linvill, for example, in an article entitled "RC Active Filters," Proceedings of the Institute of Radio Engineers, volume 42, page 555, March 1954, suggests a technique for realizing one arbitrarily chosen parameter of the four parameters of an inductorless two-port active network. Similarly, in the copending application of J. M. Sipress, Serial No. 46,285, filed July 29, 1960, since matured into U.S. Patent 2,998,580, issued August 29, 1961, there is disclosed a structure for realizing any of certain specific groups of n of the n^2 short-circuit admittance parameters of an n -port network. The difficulties with such synthesizing techniques are, of course, the inability to realize an arbitrary group of n parameters and, even more important, the inability to control the remaining $n^2 - n$ parameters.

The object of the present invention is to synthesize n -port transmission networks for which all of the parameters may be arbitrarily chosen, and which includes no inductors.

In accordance with the present invention, a generalized multi-port transmission network is obtained, including only resistors, capacitors, and amplifiers, in which all of the parameters may be preselected without restriction. The network comprises at least n amplifiers and a $3n$ -port network, including only resistors and capacitors, interconnecting the n external ports to the n inputs of the amplifiers and the n outputs of the amplifiers. In the simplest case, this $3n$ -port network includes two-port networks, each including only resistors and capacitors, by means of which each of the n ports is connected to each amplifier input and each of the n ports is also connected to each amplifier output. The parameters of the individual resistance-capacitance networks are chosen according to the method to be described below so as to realize any arbitrarily chosen overall network parameters.

The advantage of the present invention over previously known circuit synthesis techniques is the ability to generate arbitrarily all of the parameters of an n -port network without restriction and without the use of inductors.

In the drawings:

FIG. 1 is a schematic block diagram of an n -port network in accordance with the present invention including only resistors, capacitors and amplifiers;

FIGS. 2A, 2B, 2C and 2D are circuit diagrams of four different types of amplifiers suitable for use in the network of FIG. 1;

FIG. 3 is a generalized block diagram of a two-port lattice type network suitable for all of the two-port networks of FIG. 1;

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FIGS. 4A and 4B are circuit diagrams of two forms of generalized two-terminal resistance-capacitance networks suitable for realizing each of the impedances of FIG. 3;

FIG. 5 is a schematic block diagram of one possible modification of the network of FIG. 1; and

FIG. 6 is a circuit diagram of one possible two-port network constructed in accordance with the present invention.

Referring more particularly to FIG. 1, there is shown a schematic block diagram of a generic n -port network in accordance with the present invention in which the parameters as seen from each of the n ports or sets of terminals may be chosen arbitrarily. It will be noted that FIG. 1 is a line drawing which, for convenience, represents each pair of conductors in an actual circuit as a single line. The ports 11, 12, . . . 13 therefore each represent a pair of terminals to which two-wire connections may be made. For simplicity, the term "port" will hereafter be used to denote such a pair of terminals.

The network of FIG. 1 comprises a subnetwork 10, within the dashed rectangle, which includes only resistive and capacitive elements. Subnetwork 10 has $3n$ ports, n of which comprise the n ports of the overall network. Thus ports 11, 12, . . . 13 in FIG. 1 comprise the ports of the overall network. Another n of the $3n$ ports of subnetwork 10 provides access to the input of n active circuit elements 14, 15, . . . 16, and the remaining n ports provide access to the outputs of the n active circuit elements 14, 15, . . . 16. Active elements 14, 15, . . . 16 may be characterized as controlled sources and, more specifically, amplifiers. Amplifiers 14, 15, . . . 16 may take the form of any one of four different types which can be termed current-to-voltage amplifiers, voltage-to-current amplifiers, current-to-current amplifiers and voltage-to-voltage amplifiers. These various types of amplifiers will be discussed more fully below in connection with FIGS. 2A, 2B, 2C and 2D.

Referring again to FIG. 1, it can be seen that, in accordance with the present invention, an n -port network may be synthesized with arbitrarily chosen parameters and including no inductances by interconnecting at least n active elements 14, 15, . . . 16 and the n ports 11, 12, . . . 13 with a subnetwork 10 including only resistors and capacitors. In the simplest case, subnetwork 10 includes $(2n^2 + n)$ two-port networks each of which includes only resistors and capacitors. These individual two-port networks are connected as follows: A two-port network is connected between each of the n ports 11, 12, . . . 13 and the input of each of active elements 14, 15, . . . 16. Thus two-port networks 17, 18, . . . 19 connect port 11(P_1) to the inputs of active elements 14, 15, . . . 16, respectively; two-port networks 20, 21, . . . 22 connect port 12(P_2) to the same respective active element inputs; and two-port networks 23, 24, . . . 25 connect port 13(P_n) to these same respective active element inputs.

Similarly, a two-port network is connected between each of the n ports 11, 12, . . . 13 and the output of each of active elements 14, 15, . . . 16. Thus two-port networks 26, 27, . . . 28 connect port 11(P_1) to the outputs of active elements 14, 15, . . . 16, respectively; two-port networks 29, 30, . . . 31 connect port 12(P_2) to the same respective active element outputs; and two-port networks 32, 33, . . . 34 connect port 13(P_n) to these same respective active element outputs.

Subnetwork 10 also includes n additional two-port networks 35, 36, . . . 37 which also include only resistors and capacitors and which operate as individual feedback networks for the active elements 14, 15, . . . 16, respectively.

In accordance with the present invention, a network of the form shown in FIG. 1 is realizable for synthesizing

ing any possible combination of parameters at the n ports 11, 12, . . . 13. Thus, for example, filter structures having different transfer functions for the opposite directions of transmission may be synthesized and, moreover, may be synthesized with any arbitrary input and output impedances. The present invention is therefore universally applicable for synthesizing network parameters without the use of inductors.

Referring then to FIG. 2, there are shown examples of the four possible active elements suitable for use in the network of FIG. 1. FIG. 2A, for example, shows one form of current-to-voltage amplifier which might be used in the block diagram of FIG. 1. The essential characteristics of this type of amplifier are a low input impedance (ideally zero) and a low output impedance (also ideally zero). Such an amplifier may be characterized by a constant gain factor which represents the ratio of output voltage to input current. In the example in FIG. 2A, this constant is nearly equal to the total resistance value of resistors 40 and 41. Transistors 42 and 43 may be of the junction type and hence present a low emitter-to-base input impedance over a useful portion of their operating ranges. Resistors 40 and 41, of course, are of low values in order to present a low output impedance.

FIG. 2B illustrates one form of voltage-to-current amplifier which might be used in the block diagram of FIG. 1. The essential characteristics of this type of amplifier are a high input impedance (ideally infinite) and a high output impedance (also ideally infinite). Tubes 44 and 45 are of the pentode type and hence have these properties. Again, this amplifier can be characterized by a constant gain factor relating the output current and input voltage.

FIGS. 2C and 2D each illustrate one form of a current-to-current amplifier and voltage-to-voltage amplifier, respectively, which might be used in FIG. 1. Each can be characterized by a constant gain factor. The current amplifier of FIG. 2C has low input and a high output impedance and the voltage amplifier of FIG. 2D has high input and a low output impedance.

It is to be understood that the electrodes of each of the amplifiers of FIGS. 2A through 2D must be energized from some source, omitted in the drawings for simplicity. These sources must, of course, be arranged so as not to destroy the necessary impedance levels noted above. The amplifiers shown are only illustrative and should not be taken as limiting inasmuch as many other amplifiers having the necessary properties will be obvious to those skilled in the art.

FIG. 3 is a generalized block diagram of a two-port (four terminal) network of the lattice type which is one form that is suitable for all of the two-port networks in subnetwork 10 in FIG. 1. Proper choice of the individual impedances Z_1 , Z_2 , Z_3 and Z_4 provides an overall two-port network with all of the required properties. More specifically, each of the two-terminal networks Z_1 , Z_2 , Z_3 and Z_4 may have the form shown in FIGS. 4A or 4B.

In FIG. 4A there is shown a two-terminal resistive-capacitive (RC) network which, with proper choices of resistances and capacitances, will generate any impedance possible with only resistances and capacitances. The network of FIG. 4A is the so-called "first Foster form" and comprises a series resistance, a series capacitance and n parallel resistance-capacitance sections connected in series.

FIG. 4B illustrates another two-terminal resistance-capacitance network which will generate any possible RC impedance. This network is the so-called "second Foster form" and comprises a resistor and capacitor in parallel with n resistive-capacitive sections. The networks of FIGS. 4A and 4B are more fully discussed and analyzed in the text "Synthesis of Passive Networks" by E. A. Guillemin, Wiley and Sons, 1957, and will not be discussed further here except to note that many other network forms could also be used for this purpose.

Returning to FIG. 1, it is possible to analyze this network mathematically most conveniently by means of matrix techniques. The 3n-port subnetwork 10 can be characterized in terms of its external behavior at the 3n ports, that is, in terms of the relationships between the 3n voltages and 3n currents at these ports. For this purpose, it is convenient to define an admittance matrix $\hat{Y}$ such that

$$I = \hat{Y}E \quad (1)$$

where I and E are the column vectors of currents and voltages respectively, at the 3n ports of subnetwork 10. The matrix $\hat{Y}$ is a 3n by 3n short-circuit admittance matrix relating I and E and having a total of $9n^2$ terms. Each of these terms may be written as a rational function of s , where s is the complex frequency variable ($s = j\omega$ where ω is the radian frequency variable).

Each diagonal term in the 3n x 3n admittance matrix $\hat{Y}$ is the short-circuit driving-point admittance at one of the 3n ports. Similarly, each off-diagonal term in the $\hat{Y}$ matrix is the short-circuit transfer admittance between two of these 3n ports. More specifically, the term in the i th row and the j th column of the matrix $\hat{Y}$ is the short-circuit transfer admittance between ports i and j . Hence the admittance matrix $\hat{Y}$ completely specifies subnetwork 10 and can be directly related to the individual two-port networks within subnetwork 10.

Thus, in FIG. 1, the first n of the 3n ports are labeled $A_1, A_2, \dots, A_n$ and comprise the external ports 11, 12, . . . 13; the second n of the 3n ports are labeled $B_1, B_2, \dots, B_n$ and comprise the inputs to amplifiers 14, 15, . . . 16 respectively; and the third n of the 3n ports are labeled $C_1, C_2, \dots, C_n$ and comprise the outputs of amplifiers 14, 15, . . . 16, respectively. Each of the two-port networks 17 through 37 is identified with two subscripts identifying the particular pair of the 3n ports between which it is connected. These two-port networks can therefore be directly identified with corresponding terms in the matrix $\hat{Y}$ and, indeed, can be designed to provide short-circuit transfer admittance expressed in the off-diagonal terms of $\hat{Y}$.

It is, furthermore, convenient to partition the $9n^2$ items of the matrix $\hat{Y}$ into nine n by n submatrices as follows:

$$\hat{Y} = \begin{bmatrix} Y_{AA} & Y_{AB} & Y_{AC} \\ Y_{BA} & Y_{BB} & Y_{BC} \\ Y_{CA} & Y_{CB} & Y_{CC} \end{bmatrix} \quad (2)$$

where each of the terms in the matrix is itself a matrix having n^2 terms. Y_{AA} , for example, contains the n^2 elements appearing in the first n columns and first n rows of $\hat{Y}$ and hence expresses all of the relations between the currents and voltages at ports $A_1, A_2, \dots, A_n$ when all other ports are short-circuited. Similarly, Y_{AB} also has n^2 terms and expresses all of the transfer relations between the currents and voltages at ports $A_1, A_2, \dots, A_n$ and $B_1, B_2, \dots, B_n$ when all other ports are short-circuited.

Returning to the overall network of FIG. 1, an admittance matrix Y representing the relationships of the currents and voltages at the n external ports 11, 12, . . . 13, and hence the desired overall properties of the network of FIG. 1, may be expressed as follows:

$$Y = Y_{AA} + Y_{AC}[U - RY_{BC}]^{-1}RY_{BA} \quad (3)$$

where Y_{AA} , Y_{AC} , Y_{BC} and Y_{BA} are defined in Equation 2, U is the identity matrix of order n , and R is the diagonal matrix of current-to-voltage amplifier gain constants $R_1, R_2, \dots, R_n$, corresponding to the n active elements 14, 15, . . . 16.

It will be noted that the matrix $\hat{Y}$ is symmetrical and hence the submatrices Y_{CA} , Y_{CB} and Y_{AB} are uniquely

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related to Y_{AC} , Y_{BC} and Y_{AB} appearing in Equation 3. That is, once Y_{AC} , Y_{BC} and Y_{AB} are determined, Y_{CA} , Y_{CB} and Y_{BA} may be obtained merely by interchanging respective rows and columns. The submatrices Y_{BB} and Y_{CC} do not appear in Equation 3 and hence may be freely chosen to assist in the synthesis procedure. In accordance with the present invention, each of these submatrices will be chosen to (1) realize any desired Y , and (2) to render $\hat{Y}$ realizable with only resistors and capacitors.

An admittance matrix of the form of $\hat{Y}$ may be expressed in the following partial fraction form:

$$\hat{Y} = sK_{\infty} + \sum_{m=0}^M K_m \left(\frac{s}{s+a_m} \right) \quad (4)$$

where s is the complex frequency variable, a_m in every term is a non-negative real number, and K_{∞} and K_m represent $3n \times 3n$ matrices of real constants. A sufficient criterion for the realizability of the $3n$ -port network characterized by $\hat{Y}$ with only resistors and capacitors is that each of the matrices K_{∞} and K_m satisfy the so-called "dominant-diagonal condition." That is, each diagonal term in each of these matrices must be no less than the sum of the magnitudes of all of the off-diagonal terms in the row in which the diagonal term appears. A general method for synthesizing resistance-capacitance networks that satisfy the dominant-diagonal condition is shown in detail in a paper by P. Slepian and L. Weinberg entitled "Synthesis Applications of Paramount and Dominant Matrices" appearing at pages 611-630 in the Proceedings of the National Electronics Conference, October 1958, and hence will not be discussed in detail here.

In order to synthesize $\hat{Y}$ with a network including only resistances and capacitances, it is therefore sufficient to satisfy Equation 3 with submatrices Y_{AA} , Y_{AC} , Y_{BC} and Y_{BA} such that each of the diagonal terms in $\hat{Y}$, when $\hat{Y}$ is expressed in the partial fraction form of Equation 4, satisfy the dominant-diagonal condition.

It is assumed, of course, that Y , the desired and arbitrarily chosen admittance matrix for the overall network of FIG. 1, is expressed as a matrix of n^2 real rational functions in s . This involves no loss of generality since, as is well known, the desired parameters can be expressed to as close an approximation as desired merely by increasing the degree of these polynomials.

Next it is necessary to factor Y so as to obtain a common denominator D , which is also a polynomial in s , such that

$$Y = \frac{1}{D} [N_{ij}] \quad (5)$$

where $[N_{ij}]$ is an $n \times n$ matrix of polynomials in s .

The submatrix Y_{AA} may also be expressed as an $n \times n$ matrix in ratios of polynomials in s such that

$$Y_{AA} = \frac{1}{q} [x_{ij}] \quad (6)$$

where q is another common denominator polynomial in s having only distinct negative-real zeros and $[x_{ij}]$ is an $n \times n$ matrix of polynomials in s .

With this nomenclature, Equation 3 may be rewritten

$$\frac{1}{qD} [qN_{ij} - Dx_{ij}] = Y_{AC} [U - RY_{BC}]^{-1} RY_{BA} \quad (7)$$

The next step of the synthesis of $\hat{Y}$ is to define two $n \times n$ matrices of polynomials P_1 and P_2 such that

$$P = P_1 P_2 = [qN_{ij} - Dx_{ij}] \quad (8)$$

Substituting Equation 8 in Equation 7, there is obtained

$$\frac{1}{qD} P_1 P_2 = Y_{AC} [U - RY_{BC}]^{-1} RY_{BA} \quad (9)$$

Equation 9 will be satisfied with the following values for the submatrices in $\hat{Y}$:

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$$Y_{AC} = \frac{1}{\alpha_1 q} P_1 \quad (10)$$

$$Y_{BA} = \frac{1}{\alpha_2 q} R^{-1} H P_2 \quad (11)$$

$$U - RY_{BC} = H \frac{D}{\alpha_1 \alpha_2 q} \quad (12)$$

where P_1 and P_2 are $n \times n$ matrices of polynomials in s as defined in Equation 8, q and D are polynomials in s as defined in Equations 5 and 6, respectively, α_1 and α_2 are arbitrary real constants to be chosen as will be described below, and H is an arbitrary nonsingular $n \times n$ matrix of constants which also will be more fully discussed below.

In order to implement the synthesis technique implicit in Equations 8, 10, 11 and 12, it is first necessary to choose the submatrix Y_{AA} such that—

(1) Its coefficient matrices as defined in Equation 4 satisfy the dominant-diagonal condition with inequality, that is, the diagonal elements are greater than the sums of the magnitudes of the off-diagonal terms in the corresponding rows. One simple way of assuring this result is to choose Y_{AA} such that it has only diagonal terms (all off-diagonal terms being zero); and

(2) The term $[qN_{ij} - Dx_{ij}]$ can be written as the product $P_1 P_2$ such that each of Equations 10 and 11 can be satisfied with realizable submatrices, that is, ones that permit the satisfaction of the dominant-diagonal condition in the coefficient matrices of $\hat{Y}$.

These two conditions can always be met by choosing the matrix Y_{AA} with only diagonal terms, and multiplying each diagonal term in Y_{AA} by a sufficiently large real positive constant. It will be noted that the factors P_1 and P_2 of P can always be obtained if (1) the degree of each polynomial in $[x_{ij}]$ is equal to the degree of q , and (2) the determinant of P has at least K distinct real zeros where $K \geq n$ Deg. q , n is the number of ports, and Deg. q is the degree of the polynomial q . Increasing the diagonal multiplier in Y_{AA} has the effect of producing the proper zeros of the determinant of P for some finite value of the diagonal multiplier, and hence the above criterion can always be met.

If this procedure is followed, at each stage of an iterative decomposition n distinct real zeros of the determinant of P can be removed as a linear factor of the matrix polynomial P . The factor remaining is a matrix polynomial with degree reduced by unity.

The parameters α_1 and α_2 are then chosen sufficiently large to insure the satisfaction of the dominant-diagonal condition in the first n rows of the matrix $\hat{Y}$ as expressed in Equation 2. As can be seen in Equations 2, 10 and 11, increasing α_1 and α_2 reduces the Y_{AB} and Y_{AC} terms. They can be reduced until the diagonal terms in Y_{AA} as chosen above satisfy the dominant-diagonal condition. Since the matrices Y_{BB} and Y_{CC} are unrestricted by Equation 3 they may be chosen so that the dominant-diagonal condition is met in the last $2n$ rows of $\hat{Y}$ as expressed in Equation 2.

It will be noted that the matrix Y , representing the overall network parameters for the network of FIG. 1, may be arbitrarily prescribed in all of its elements. Thus, in accordance with the present invention, it is possible to synthesize any conceivable network parameters. In addition, various other properties may be obtained by properly choosing the matrix H .

The structure of FIG. 1 is the simplest of the many possible structures and hence has been considered first. It is obtained by letting H be the identity matrix, in which case Equations 10, 11 and 12 reduce to

$$Y_{AC} = \frac{1}{\alpha_1 q} P_1 \quad (10a)$$

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$$Y_{BA} = \frac{1}{\alpha_2 q} R^{-1} P_2 \quad (11a)$$

$$Y_{BC} = R^{-1} \left[1 - \frac{D}{\alpha_1 \alpha_2 q} \right] \quad (12a)$$

By choosing H in other ways, however, it is possible to realize other network advantages. In FIG. 5, for example, there is shown one modification of the network shown in FIG. 1 in which similar elements have like reference numerals. Subnetwork 10 is shown in FIG. 5 in block form, it being understood that this subnetwork is identical to that shown in FIG. 1. In addition, n two-port networks 50, 51, . . . 52, 53 are connected such that the n active networks 14, 15, . . . 16 are connected in a ring with one of networks 50, 51, . . . 52, 53 joining the output of each of the amplifiers in the ring to the input of the next succeeding amplifier. Thus network 50 connects the output of amplifier 14 to the input of amplifier 15, network 51 connects the output of amplifier 15 to the input of the next succeeding amplifier, not shown, network 52 connects the output of the $(n-1)$ st amplifier, not shown, to the input of the n th or last amplifier 16, and network 53 connects the output of the last amplifier 16 to the input of the first amplifier 14 to complete the ring.

It is apparent from Equation 12 that the diagonal terms in Y_{BC} can be expressed as

$$1 - R_i \hat{y}_{n+1, 2n+i} = h_{n+1, 2n+i} \frac{D}{\alpha_1 \alpha_2 q} \quad (i=1, 2, \dots, n) \quad (13)$$

and the non-zero off-diagonal terms required by FIG. 5 as

$$R_i \hat{y}_{n+1, 3n} = h_{n+1, 3n} \frac{D}{\alpha_1 \alpha_2 q} \quad (14)$$

$$R_i \hat{y}_{n+1+i, 2n+i} = h_{n+1+i, 2n+i} \frac{D}{\alpha_1 \alpha_2 q} \quad (i=1, 2, \dots, n-1) \quad (15)$$

The non-zero elements of H are chosen so that H is nonsingular, that is, so that its determinant is not zero. The elements in Y_{BC} can be calculated by Equations 14 and 15 and Y_{BA} from Equation 11.

It is apparent that there are many more degrees of freedom in choosing the elements of $\hat{Y}$. For example, the off-diagonal terms of Y_{AA} may be specified, Y_{BB} and Y_{CC} may be specified, H may be differently specified, and so forth. It is clear that other desirable properties may be realized with networks of the form of FIGS. 1 and 5 and still utilizes only resistive and capacitive elements in subnetwork 10. It is to be understood that the above-described synthesis techniques are merely illustrative of these many other variations which also come within the spirit and scope of the present invention.

The following steps are sufficient for realizing a subnetwork 10 (FIG. 1) which will (1) exhibit an arbitrarily chosen short-circuit admittance matrix for the overall network, (2) require only n active elements, and (3) require in addition only resistors and capacitors for its realization. These steps are:

(1) Choose Y_{AA} such that—

- Its coefficient matrices satisfy the dominant-diagonal condition with inequality, and
- The matrix $[qN_{ij} - Dx_{ij}]$ can be factored into two matrices P_1 and P_2 having degrees not exceeding the degree of q .

(2) Let

$$Y_{AC} \text{ equal } \frac{1}{\alpha_1 q} P_1$$

(3) Let

$$Y_{BA} \text{ equal } \frac{1}{\alpha_2 q} R^{-1} P_2$$

(4) Choose Y_{BC} to satisfy the relationship

$$[U - RY_{BC}] = H \frac{D}{\alpha_1 \alpha_2 q}$$

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(5) Choose α_1 and α_2 sufficiently large to satisfy the dominant-diagonal condition in the first n rows of coefficient matrices of $\hat{Y}$.

(6) Specify Y_{BB} and Y_{CC} such that the dominant-diagonal condition is satisfied in the last $2n$ rows of the coefficient matrices of $\hat{Y}$.

(7) Construct the resistance-capacitance subnetwork specified by $\hat{Y}$.

It is to be noted that when the above procedure is followed, the last step can always be achieved.

It will be further noted that the synthesis technique has been described with reference to current-to-voltage amplifiers. This procedure was chosen only for convenience and it is apparent that any of the four types of amplifiers shown in FIGS. 2A through 2D would be suitable. With the voltage-to-voltage amplifier of FIG. 2D, for example, Equation 3 takes the form

$$Y = Y_{AA} + [Y_{AC}R + Y_{AB}][-Y_{BB} - Y_{BC}R]^{-1} Y_{BA} \quad (16)$$

Similar equations could be written for either of the other two forms of amplifiers and the realization techniques are similar in all essential respects.

To further illustrate the synthesis procedure, a particular two-port network will be synthesized, utilizing the structure shown in FIG. 1. The resulting structure is shown in FIG. 6 and is achieved in the following manner.

For simplicity, it is assumed that the gain constants of the active elements 60 and 61 are each unity, that is, $R_1 = R_2 = 1$. Let the desired overall properties at the two external ports 62 and 63 be represented by the following matrix:

$$Y = \frac{1}{s+3} \begin{bmatrix} 1 & (s+3) \\ (s-3) & 2 \end{bmatrix} \quad (17)$$

This expression for Y has been chosen because of the simplification in the mathematics thereby obtaining. In an actual network, each of the terms could be a polynomial in s of any degree. It is to be noted, however, that Equation 17 specifies a network of a type not heretofore realized without the use of inductors and having the following interesting properties: (1) the transmission from port A2 (terminals 63) to port A1 (terminals 62) is completely independent of frequency; (2) the transmission from port A1 to port A2 provides no changes in amplitude with frequency but a change of phase with frequency; and (3) the driving-point impedances at each of ports A1 and A2 are inductive and resistive.

To perform the synthesis, it is first necessary to choose a Y_{AA} which satisfies the dominant-diagonal condition and, furthermore, permits the factoring of P_1 and P_2 . The following matrix satisfies these conditions:

$$Y_{AA} = \frac{1}{s-3} \begin{bmatrix} 10(s+1) & 0 \\ 0 & 10(s+2) \end{bmatrix} \quad (18)$$

The factors required are

$$P_1 = \begin{bmatrix} (s+3) & 0 \\ 0 & (s+3) \end{bmatrix}; P_2 = \begin{bmatrix} -(10s+9) & (s+3) \\ (s-3) & -(10s+18) \end{bmatrix} \quad (19)$$

From Equations 10a, 11a and 12a

$$Y_{AC} = \frac{1}{\alpha_1} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (20)$$

$$Y_{BA} \frac{1}{\alpha_2} \begin{bmatrix} -3 & 1 \\ -1 & -6 \end{bmatrix} + \frac{s}{\alpha_2(s+3)} \begin{bmatrix} -7 & 0 \\ 2 & -4 \end{bmatrix} \quad (21)$$

$$Y_{BC} = U \left[1 - \frac{1}{\alpha_1 \alpha_2} \right] \quad (22)$$

It is now necessary to expand Equation 18 in a form similar to Equation 4 in order to obtain coefficient matrices. The required expansion is:

$$Y_{AA} = \begin{bmatrix} 3.33 & 0.00 \\ 0.00 & 6.67 \end{bmatrix} + \frac{s}{s+3} \begin{bmatrix} 6.67 & 0.00 \\ 0.00 & 3.33 \end{bmatrix} \quad (23)$$

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From Equations 20, 21 and 23 it can be seen that the dominant-diagonal condition will be met with the constants α_1 and α_2 having the values 2.70 and 1.35, respectively. Using these values, the matrix $\hat{Y}$ can be expanded in the form

$$\hat{Y} = K_0 + K_1 \frac{s}{s+3} \quad (24)$$

with the following coefficient matrices:

$$K_0 = \begin{bmatrix} 3.33 & 0.00 & 2.22 & -0.74 & 0.37 & 0.00 \\ 0.00 & 6.67 & 0.74 & -4.44 & 0.00 & 0.37 \\ -2.22 & 0.74 & & 0.00 & 0.73 & 0.00 \\ -0.74 & -4.44 & 0.00 & & 0.00 & 0.73 \\ 0.37 & 0.00 & 0.73 & 0.00 & & 0.00 \\ 0.00 & 0.37 & 0.00 & 0.73 & 0.00 & \end{bmatrix} \quad (25)$$

$$K_1 = \begin{bmatrix} 6.67 & 0.00 & -5.19 & 1.48 & 0.00 & 0.00 \\ 0.00 & 3.33 & 0.00 & -2.96 & 0.00 & 0.00 \\ -5.19 & 0.00 & & 0.00 & 0.00 & 0.00 \\ 1.48 & -2.96 & 0.00 & & 0.00 & 0.00 \\ 0.00 & 0.00 & 0.00 & 0.00 & & 0.00 \\ 0.00 & 0.00 & 0.00 & 0.00 & 0.00 & \end{bmatrix} \quad (26)$$

It will be noted that no entries have been made in the diagonal positions in Y_{BB} and Y_{CC} . Any entries desired may be made here provided only that they satisfy the dominant diagonal condition. For this reason we may synthesize the network $\hat{Y}$ without regard to these diagonal elements. In this example, these items will not be specified in order to simplify the mathematical problem but it is to be understood that in the general case, it may be desirable to specify them in some particular manner to obtain some particular network properties in addition to those specified in Equation 17.

The values of the elements of the various two-port networks in FIG. 6 are easily obtainable from Equations 25 and 26 as described in the afore-mentioned article by Slepian and Weinberg. They are given below, with conductance values in mhos and capacitances in farads.

$G_1=4.44$	$G_{17}=0.74$
$G_2=10.37$	$G_{18}=0.74$
$G_3=10.37$	$G_{19}=0.74$
$G_4=4.44$	$G_{20}=0.74$
$G_5=1.41$	$G_{21}=1.45$
$G_6=2.96$	$G_{22}=1.45$
$G_7=2.96$	$G_{23}=1.45$
$G_8=1.41$	$G_{24}=1.45$
$G_9=1.48$	
$G_{10}=1.48$	$C_1=3.46$
$G_{11}=8.89$	$C_2=3.46$
$G_{12}=5.93$	$C_3=0.99$
$G_{13}=5.93$	$C_4=0.99$
$G_{14}=8.89$	$C_5=1.98$
$G_{15}=0.37$	$C_6=1.98$
$G_{16}=1.11$	$C_7=0.12$

It is to be understood that the above-described arrangements are merely illustrative of the numerous and varied other arrangements which might comprise applications of the principles of the invention. Such other arrangements may readily be devised by those skilled in the art without departing from the spirit and scope of this invention.

What is claimed is:

1. A wave transmission network having n ports and comprising at least n active elements and a $3n$ -port passive network including only resistors and capacitors,

where n is greater than one, a first n of said $3n$ ports comprising the ports of said wave transmission network, means for connecting another n of said $3n$ ports to the individual inputs of said n active elements, and means for connecting the remaining n of said $3n$ ports to the individual outputs of said n active elements.

2. The wave transmission network according to claim 1 wherein said $3n$ -port passive network includes a plurality of two-port passive networks including only resistors and capacitors, means connecting one of said two-port networks between each of said first n ports and each of said other n ports of said $3n$ -port network, means connecting one of said two-port networks between each of said first n ports and each of said remaining n ports of said $3n$ -port network, and means connecting one of said two-port networks between corresponding ones of said other n ports and said remaining n ports of said $3n$ -port network.

3. The wave transmission network according to claim 2 further including means connecting one of said two-port networks between each of said other n ports and the one of said remaining n ports preceding the corresponding one of said remaining n ports.

4. A wave transmission network including n ports, at least n active circuit elements, and circuit means including at least $2n^2+n$ two-port networks interconnecting said n ports, the inputs of said active circuit elements, and the outputs of said active circuit elements, said two-port networks each including only resistors and capacitors.

5. The wave transmission network according to claim 4 wherein said active circuit elements comprise signal amplifiers.

6. The wave transmission network according to claim 5 wherein said n active circuit elements are connected in a ring in which a two-port network including only resistors and capacitors connects the output of each of said active circuit elements to the input of the next succeeding active circuit element in said ring.

7. A wave transmission network including n ports and at least n active circuit elements, a two-port network including only resistors and capacitors connecting each of said n ports and the inputs of each of said active circuit elements, a two-port network including only resistors and capacitors connecting each of said n ports and the outputs of each of said active circuit elements, and a two-port network including only resistors and capacitors connecting the output of each of said active circuit elements to the input of the corresponding active circuit element.

8. An active wave transmission network comprising n external ports having n^2 arbitrarily chosen parameters associated therewith, where n is greater than one, at least n signal amplifiers each having a substantially constant gain factor, and a $3n$ -port passive transducer including only resistors and capacitors interconnecting said n external ports, the inputs of said amplifiers, and the outputs of said amplifiers, said $3n$ -port passive transducer being constructed to realize said n^2 arbitrarily chosen parameters at said n external ports.

9. The active wave transmission network according to claim 8 wherein said amplifiers comprise current-to-voltage amplifiers.

10. The active wave transmission network according to claim 8 wherein said amplifiers comprise voltage-to-current amplifiers.

11. The active wave transmission network according to claim 8 wherein said amplifiers comprise current-to-current amplifiers.

12. The active wave transmission network according to claim 8 wherein said amplifiers comprise voltage-to-voltage amplifiers.

13. In combination, a passive network having $3n$ pairs of terminals and including only resistors and capacitors, where n is greater than one, means for connecting an amplifier between each of a first n of said $3n$ pairs of terminals and a corresponding pair of a second n of said

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$3n$ pairs of terminals, utilization means having n pairs of terminals, and means for connecting said utilization means to the remaining n of said $3n$ pairs of terminals.

14. The combination according to claim 13 wherein said passive network includes a plurality of four-terminal networks each including only resistors and capacitors, means for connecting one of said four-terminal networks between each of said first n of said $3n$ pairs of terminals and said remaining n of said $3n$ pairs of terminals, and means for connecting one of said four-terminal networks between each of said second n of said $3n$ pairs of terminals and said remaining n of said $3n$ pairs of terminals.

15. The combination according to claim 13 including n four-terminal networks each including only resistors and capacitors, and means for connecting one of said four-terminal networks around each of said amplifiers in a feedback connection.

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16. The combination according to claim 13 including $2n$ four-terminal networks each including only resistors and capacitors, means for connecting each of a first n of said four-terminal networks between the output of each of said amplifiers and the input of the next succeeding one of said amplifiers to form a major feedback loop including all of said amplifiers, and means for connecting each of the remaining n of said four-terminal networks in a minor feedback loop around a different one of said amplifiers.

References Cited in the file of this patent

UNITED STATES PATENTS

2,817,822 Meyers ----- Dec. 24, 1957