

May 9, 1961

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2,983,904

SORTING METHOD AND APPARATUS

Filed Oct. 4, 1957

3 Sheets-Sheet 1

FIG. 1

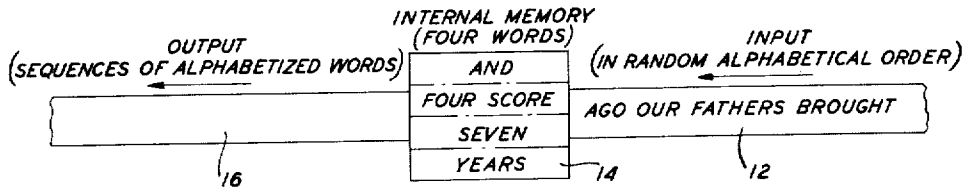


FIG. 2

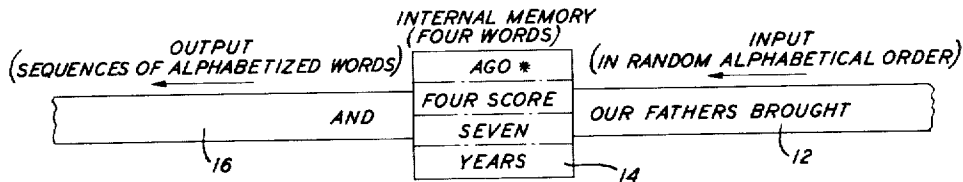


FIG. 3

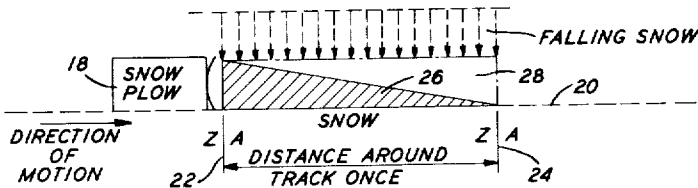


FIG. 4

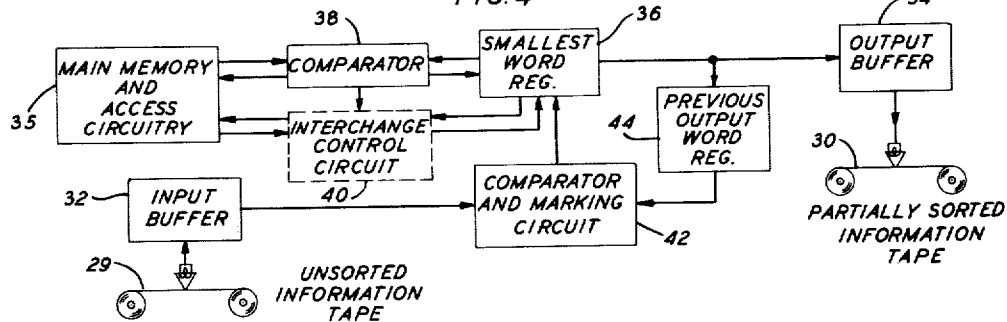
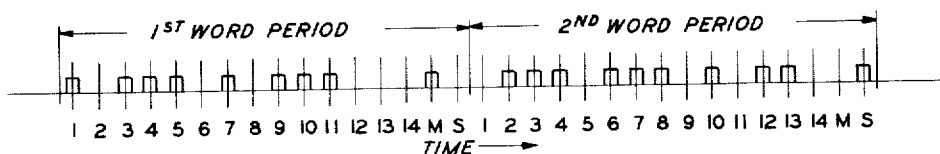


FIG. 5



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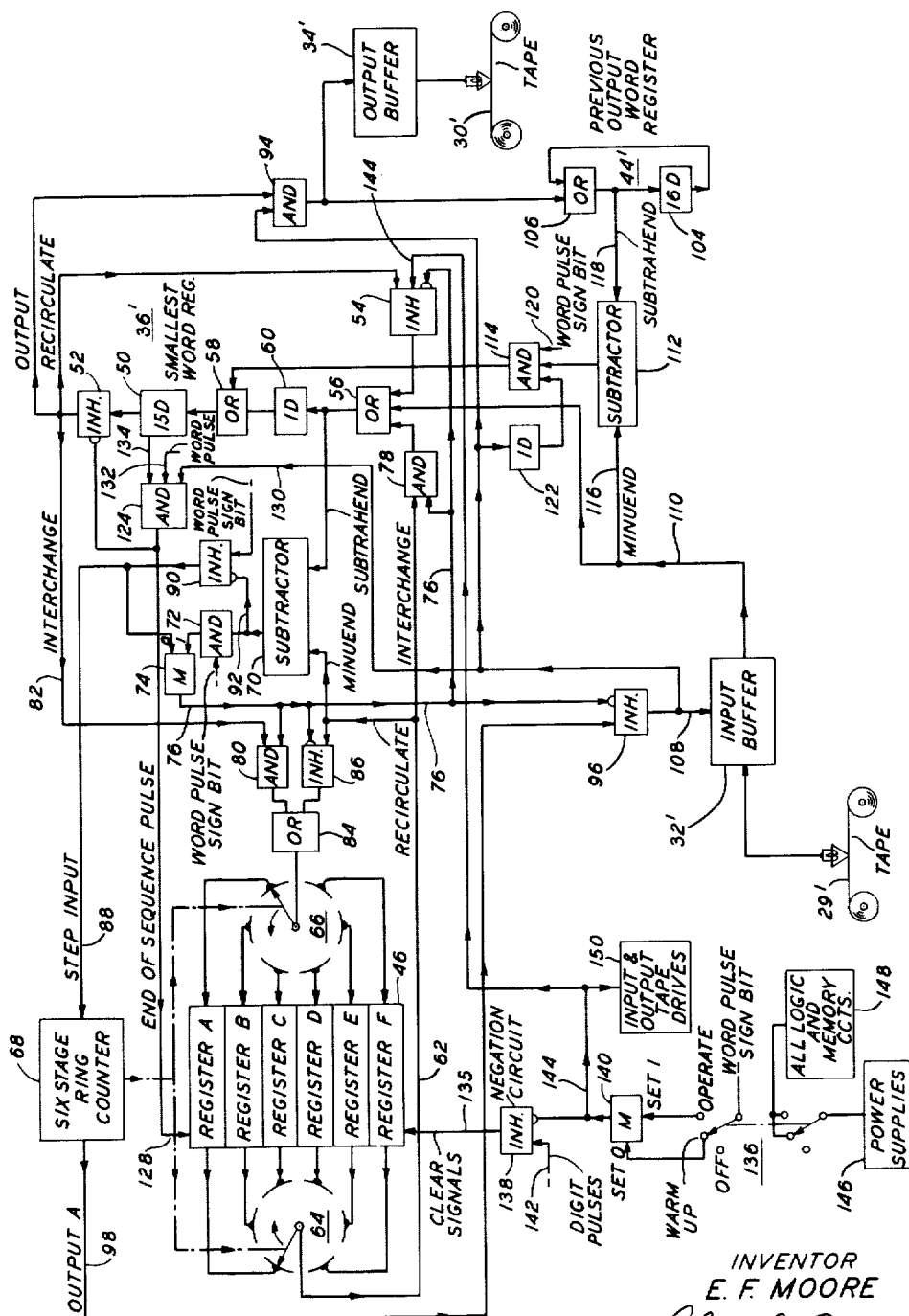
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3 Sheets-Sheet 2

FIG. 6



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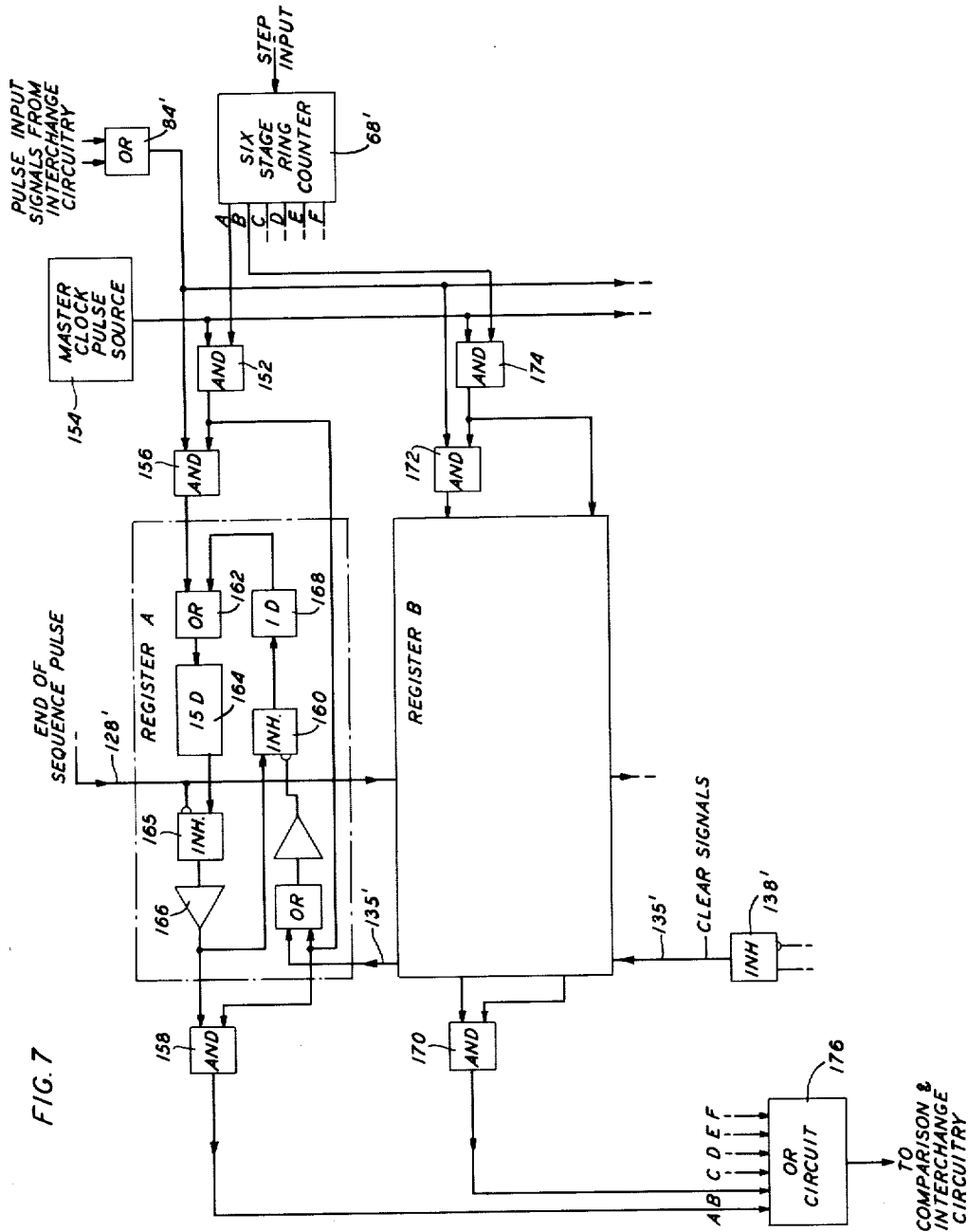
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SORTING METHOD AND APPARATUS

Filed Oct. 4, 1957

3 Sheets-Sheet 3



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1

2,983,904

SORTING METHOD AND APPARATUS

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Filed Oct. 4, 1957, Ser. No. 688,355

7 Claims. (Cl. 340—172.5)

This invention relates to a method and apparatus for sorting, and has for its principal object the reduction of the time required for sorting operations.

Sorting is a frequently performed operation used in financial and accounting data processing, as opposed to scientific computation. Sorting has been performed for many decades on punched card machines, and the two standard methods now generally in use are adaptations of punched card methods. These two methods are designated "digital sorting" and "merging or collation sorting."

When digital information having several digit places is sorted by the digital method, the digital information is fed through the machine a number of times equal to the number of places in the digital numbers constituting unsorted input information. The numbers are fed into the machine in the form of a single deck of cards in the case of punched card machines, and come out in ten different packs of cards corresponding to the ten possible decimal digits. On the first run through the computer, the numbers are sorted by the least significant digit, and on the last run, they are sorted by the most significant digit.

The other method, called "merging-sorting," or "collation sorting," normally involves combining several input sorted sequences into a single sorted output sequence including all of the original information. If a merging-sorting operation is to be started from a single unsorted list, a data processing circuit would store words in its internal memory, sort these words internally, and then release all of these words in alphabetical sequences, each having a length equal to or smaller than the number of words in the internal memory of the computer. On subsequent runs the alphabetical sequences are combined to produce longer sequences.

The digital technique is best suited to the sorting of numbers having only a few digit places. Merging-sorting, however, is applicable to information having many digit places, and is particularly useful in combining two lists which are already alphabetized.

An important object of the present invention is to increase the length of sequences for use in merging-sorting operations.

This object is accomplished in accordance with the present invention by inserting unsorted words into the internal memory of the computer, and then taking the information out one word at a time. In addition, each time a word is removed from the internal memory, an additional word from the unsorted list is inserted into the memory. By this technique, the average length of sorted sequences is doubled, as contrasted with the system mentioned above in which the internal memory is first filled and then entirely emptied before additional words from the unsorted list are entered in the memory.

In accordance with a feature of the invention, a data processing apparatus for sorting information into sequences has a high speed memory having a capacity for several words, includes circuitry for successively transmitting selected output words and for receiving an unsorted word each time that an output word is transmitted, and also includes circuitry for sorting the currently stored

2

words including a new input word to select each successive output word.

In accordance with another feature of the invention, the data processing apparatus described above includes additional circuitry for distinctively identifying stored words which have a value such that they cannot be included in the current output sequence.

Other objects, features, and various advantages of the invention may be readily apprehended from a consideration of the following detailed description, and the accompanying drawing, in which:

Figs. 1 and 2 are diagrams indicating the mode of operation of the present sorting apparatus;

Fig. 3 is a diagram showing the analogy of the present sorting system with a snowplow on a circular track;

Fig. 4 is a block diagram of the sorting apparatus in accordance with one illustrative embodiment of my invention;

Fig. 5 is a pulse diagram showing two successive serial binary "words";

Fig. 6 is a logic circuit diagram showing one instrumentation of the circuit of Fig. 4; and

Fig. 7 is a more detailed showing of a portion of the circuit of Fig. 6.

The sorting method, in accordance with the present invention, can best be explained by means of an example. A familiar set of words will be taken as they appear in their well known order, and will be sorted into alphabetical sequences. As mentioned above, this is the first step toward sorting the words into alphabetical order.

Referring to Fig. 1, the input words, which are taken from Lincoln's Gettysburg Address, are received from a tape input 12 at the right of the figure. The first four words are stored in the internal memory 14, and output words are applied to the tape 16. It may be noted that the words in the internal memory are sorted alphabetically. In Fig. 2, the first word "and" has been printed on the output tape 16, and the next unsorted input word "ago" has been inserted in the internal memory 14. It may also be noted that the word "ago" has been marked with an asterisk to indicate that it comes before the word "and" in the alphabet, and therefore that it must be included in the next subsequent sequence of words. This convention for the use of asterisks will be employed in the next few paragraphs of the description.

Next, the word which follows alphabetically the last word on the output tape is read out, and once again the internal memory is refilled and re-alphabetized.

Output	Internal Memory	Input
and fourscore	ago* our seven years	fathers brought forth

Up till now the procedure has merely been reading out the list of those words which were in the internal memory at the beginning. However, reading out the word which follows alphabetically the last one now causes a newcomer to appear.

Output	Internal Memory	Input
and fourscore our	ago* fathers* seven years	brought forth on this

Continuing the above process for two more steps produces at the fifth output word the end of an alphabetical sequence. Specifically, no word is present in the internal memory which follows the word "years."

Output	Internal Memory	Input
and fourscore our seven years	ago* brought* fathers* forth*	on this continent a

3

When this occurs, the next step is to begin a new sequence (which is separated from the old by a "/"), by reading out the word which comes first in alphabetical order. In addition, all the asterisks are deleted.

Output	Internal Memory	Input
and fourscore our seven years/ago	brought fathers forth on	this continent a new

After two more steps, the following condition develops. 10

Output	Internal Memory	Input
and fourscore our seven years/ago brought fathers	continent* forth on this	a new nation conceived

After three more steps the end of the second sequence is reached. This second sequence contains six words.

Output	Internal Memory	Input
and fourscore our seven years/ago brought fathers forth on this	a* continent* nation* new*	conceived in liberty

Continuing with the next alphabetical sequence, the condition shown below is eventually reached.

Output	Internal Memory	Input
and fourscore our seven years/ago brought fathers forth on this/a conceived continent in	and* liberty nation new	dedicated to the

And the third alphabetical sequence contains nine words:

Output	Internal Memory	Input
and fourscore our seven years/ago brought fathers forth on this/a conceived continent in liberty nation new the to	and* dedicated* proposition* that*	all men are

The foregoing example is sufficient to show how the method works, and to illustrate the fact that there are always at least as many words in each alphabetical sequence as there are words in the internal memory. This can be seen by noting that all of the words which are in the internal memory at the beginning of each alphabetical sequence will surely be included in the sequence. In addition, however, there can be more words in each sequence if, as happened in each of the foregoing examples, new words from the input happen to fall within the part of the alphabet that has not yet been read out.

Concerning the average length of sequences, it will be shown in the following paragraphs that they are normally twice as long as the number of words in the internal memory of the data processing apparatus. The sequences obtained from the first portion of Lincoln's Gettysburg Address were not quite as long, having lengths of five, six, and nine words, for an average of six and two-thirds words. This is in contrast to the expected average of eight words, which is to be expected from an apparatus having an internal memory of four words.

Determining the average number of words included in sequences is a probability problem which is readily solved by analogy to the situation shown in Fig. 3. Fig. 3 represents a snowplow 18 traveling around a circular track while snow is falling at a constant rate. In the diagram of Fig. 3, the line 20 represents the circular track unrolled, so that the vertical lines 22 and 24 represent the identical point on the circular track. The individual flakes of snow correspond to the words coming in at random to be sorted, and the snowplow corresponds to the orderly progression of this method of sorting through the alphabet. The path representing the alphabet is circular because the letter A immediately follows the letter Z; that is, a new alphabetical sequence is started as soon as the old one is completed.

The problem consists of finding the ratio between the amount of snow removed on one trip around the track, 75

4

which corresponds to the length of one alphabetical sequence, to the amount of snow on the track at any one time, corresponding to the internal memory of the data processing apparatus. The snowplow problem can be solved geometrically by inspection. The snow corresponding to the internal memory of the apparatus has a triangular cross-section, as shown at 26 in Fig. 3. The amount of snow removed by the snowplow in one trip around the alphabetical track has a cross-section including both the triangle 26 and the additional triangle 28. The amount of snow removed is therefore twice the amount of snow on the track at any one time. This figure confirms the statement made above to the effect that the alphabetical sequences are normally twice the length of the internal word capacity of the data processing apparatus. In view of the analogy to the snowplow situation as discussed above, the present sorting technique has been informally termed a "snowplow" method of sorting.

The block diagram of Fig. 4 represents an illustrative system for instrumenting the snowplow method of sorting described above. The system of Fig. 4 includes a tape input 29 for supplying unsorted input information and an output tape 30 for receiving partially sorted sequences. In addition, input and output buffering circuits 32 and 34 are required. The internal memory and access circuitry is designated 35 in Fig. 4. The smallest word from the main internal memory is routed to the "smallest word register" 36 during each operation. The comparator 38 and interchange control circuit 40 are utilized in the routing of words to the smallest word register 36. Input words are applied to the comparator and marking circuit 42. In this circuit, input words are compared with the previous output word which is held in register 44. The system also includes circuitry for identifying words which are smaller than the previous output word and for marking them in a distinctive manner.

The illustrative instrumentation of the "snowplow" method of sorting is a serial binary data processing system. For convenience, the "words" which are sorted in the present illustrative system are actually binary numbers, and they are sorted in accordance with their numerical value. Two representative words, or groups of binary digits, are shown in the pulse diagram of Fig. 5. In this illustrative diagram, pulses or spaces representing successive binary digits of progressively increasing significance appear in time slots designated 1 through 14. In addition, time slots are provided for a marking signal and for a sign bit. In the two words shown in Fig. 5, these time slots are designated M and S, and correspond to the fifteenth and sixteenth binary digits included in each word.

Fig. 6 is a detailed logic circuit diagram of an illustrative embodiment of the invention. Before considering the circuit configuration or the mode of operation of the circuit of Fig. 6, the nature of the circuit components shown as blocks in this figure should be considered.

In Figs. 6 and 7 the circuits are shown in terms of "building blocks," or basic package circuit units which may be employed in a digital computer. While the specific circuits may be implemented in many different ways, one satisfactory set of circuits is disclosed in an article by J. H. Felker entitled "Regenerative Amplifier for Digital Computer Applications" which appeared at pages 1584 through 1596 of the November 1952 issue of the Proceedings of the I.R.E., Volume 40, No. 11. The basic logic circuit components which are disclosed on pages 1594 and 1595 of this article are listed below, together with their properties.

OR units yield a pulse output if a pulse is present at any of the inputs to the OR unit.

AND units require the energization of all input leads to produce an output pulse.

Inhibit units are designated by boxes with the legend INH inside a box. An inhibit unit is generally similar to an AND unit in that all of the normal inputs to the unit must be energized to produce an output pulse. How-

ever, a pulse on the inhibit input lead, marked with a small semicircle at the point where the inhibit input lead is connected to the box representing the inhibit circuit, overrides all other signals and blocks the output of the unit.

Memory units are designated by boxes including the letter "M." Memory units may be set to either of two conditions, the "0" state or the "1" state. When set to the "0" state, the memory unit has no output. When the "set 1" lead has been energized, however, the memory unit generates pulses in successive digit intervals until the memory unit is reset to the "0" state. When both input leads are energized simultaneously, the memory unit assumes the "0" state and has no output.

Delay units are indicated by boxes with the letter "D" therein together with an indication of the number of digit periods of delay introduced by the unit.

The circuit of Figs. 6 and 7 is synchronous, and accurate timing throughout the circuit is maintained by a master clock, as discussed in the Felker article cited above. In synchronous data processing circuits, it is useful to have pulses available which occur in the same digit period of each word. Such pulses are designated "word pulses" because they occur once during each word. For specific example, a "sign bit word pulse" occurs once each word in the time slots designated S in Fig. 5. Word pulse generation circuitry is normally in the form of a ring counter having a number of states equal to the number of digits in each word. Clock pulses are applied to the step input of the ring counter, and word pulses associated with each time slot of the word appear at the output leads from successive stages of the ring counter. In view of the conventional nature of such circuits, they are not shown in Figs. 6 and 7.

Now, returning to the details of Fig. 6, unsorted digital input signals are applied to the circuit from the tape input 29' and the input buffer circuit 32'. Sorted sequences of words are applied to the output tape circuit 30' via the output buffer circuit 34'. The buffer circuits are required to couple the synchronous data processing circuit to the input and output tapes. The buffer circuits may each include several registers, circuitry for transferring information successively from one register to the next, and feedback circuitry for controlling the tape driving speeds.

It will be assumed that the digital information is in serial binary form, as indicated in Fig. 5, at the output from the input buffer circuit 32. Digital information is arranged in sequences corresponding to the value of the binary number represented by the groups of pulses. In this regard, it may be noted that the least significant digits appear first in time, and that the mark and the sign digits appear last in time. The internal memory of the sorting apparatus includes space for storing seven words, or numbers. The main portion of the memory 46 includes six registers A through F. One additional register 36' is designated the "smallest word" register, and constitutes a delay loop including the delay line 50, the inhibit units 52 and 54, the OR circuits 56 and 58, and the one-digit period delay circuit 60.

In comparing the logic circuit of Fig. 6 with the block diagram of Fig. 4, it may be seen that a number of components in Fig. 6 which correspond directly to the circuits shown in Fig. 4 bear corresponding primed reference numerals. In addition, it may be noted that the memory circuit 46 and associated circuits including switches 64 and 66 in Fig. 6 correspond generally to block 35 in Fig. 4; subtractors 70 and 112 and their associated circuits correspond generally to blocks 38 and 42, respectively, in Fig. 4; and the memory circuit 74, together with considerable additional circuitry in Fig. 6, corresponds to the interchange control circuit 40 of Fig. 4.

Considering the operation of Fig. 6, it will be assumed that a new word from the input buffer circuit 32' has

been applied to the smallest word register 36' through the OR circuit 56. The next operation involves comparing the new word with each of the words stored in registers A through F in the memory circuitry 46. In each case, as the comparison proceeds, the smaller of the two words is entered in the smallest word register. This may or may not require an interchange of digital information between the smallest word register 36' and one of the registers A through F, depending on the relative magnitudes of the two words. Each of the registers A through F is coupled successively to the memory output circuit 62 and the input OR circuit 84 by switching circuits 64 and 66, respectively, which are shown in Fig. 6 as commutators. The operation of the switching circuits 64 and 66 is controlled by a six-stage ring counter 68.

When the switching circuits 64 and 66 are in the states shown in Fig. 6, register A is connected to the output circuit 62 and the input OR circuit 84. The digital information in register A is then compared with that in the smallest word register 36' by the subtractor 70. In the subtractor circuit, the information from register A is the minuend and the information from register 36' constitutes the subtrahend to be subtracted from the minuend to produce a difference. If the number from register 36' is smaller than the number from register A, it is not necessary to interchange the two numbers. If the number in register A is smaller than that in register 36', however, the two numbers should be interchanged. The interchange operation is triggered by a sign bit output from subtractor 70, indicating that the output number is negative and thus, that the word from register 36' is greater than that from register A. The sign bit of the number from subtractor 70 is sampled by the AND gate 72 which has a sign bit word pulse as an additional input. If the sign bit is present, the memory circuit 74 is set to the "1" state and produces a series of digit pulses during the next word period.

The output lead 76 from the memory circuit 74 constitutes an interchange control lead which applies signals to the necessary logic circuits to effect the interchange of numbers between register A and register 36'. Thus, for example, the interchange control lead 76 is connected to the AND circuit 78 to permit the coupling of digital information from register A on lead 62 to the register 36' via AND circuit 78 and OR circuit 56. The lead 76 is also coupled to the inhibit unit 54 to block the recirculation of the information previously stored in the smallest word register 36'. In a similar manner, lead 76 is connected to AND circuit 80 to gate information from the smallest word register 36' on lead 82 through the AND circuit 80 and the OR circuit 84 into register A. Interchange control signals are also coupled from lead 76 to the inhibiting input terminal of the inhibit unit 86 to block the recirculation of information from register A.

The ring counter 68 has six stages which control the coupling of registers A through F to the external comparison and interchange circuitry. The state of ring counter 68 is advanced by pulses applied to it on lead 88. The advance pulses are developed by the inhibit unit 90, which is coupled to the output of the subtractor 70. The normal input to the inhibit unit 90 is a sign bit word pulse. If no pulse appears on the inhibiting input lead 92 to the inhibit unit 90, the sign bit word pulse is transmitted through inhibit unit 90 to the step input lead 88 of the ring counter 68.

It may be recalled that the interchange operation occurs in response to an output sign bit pulse from subtractor 70 indicating that the number in register A, or one of the other lettered registers, is smaller than that in register 36'. This pulse from subtractor 70 is also applied on lead 92 to the inhibit unit 90, and blocks the transmission of an output pulse from the inhibit unit 90 during the word period immediately preceding the one in which an interchange operation occurs. During the word period in which interchange occurs, the word from register A appears at both the subtrahend input and at the minuend

input of the subtractor 70. Under these circumstances, no sign bit appears at the output of the subtractor, and the inhibit unit 90 produces an output to step the ring counter 68. Thus, the ring counter 68 is advanced either once every second word period or once every word period, depending respectively on whether or not an interchange operation occurs.

Following the complete cycle of the six-stage ring counter 68, the smallest of the seven words included in registers A through F and register 36' is located in register 36'. At this point, it is desirable to gate this smallest word out to the tape 30' and to insert a new word into the data processing circuit. The AND circuit 94 is energized by the inhibit unit 96 to perform the desired gating function. The output lead 98 from state A of the six-stage ring counter 68 is connected to the normal input of the inhibit unit 96, and the interchange control lead 76 from the memory unit 74 is connected to the inhibiting input terminal of the inhibit unit; state A refers to the time condition of the counter 68 in which the output thereof is coupled to both the register A and the lead 98, and which output consists of a continuous sequence of digit pulses in successive digit periods. (This last-mentioned connection blocks signals from inhibit unit 96 during a possible second word period in which signals may be interchanged between register A and register 36'.) Accordingly, during the first word period in which the ring counter 68 is in state A, the word from the smallest word register 36' is gated out to the output buffer circuit 34' and to the tape 30'. It may be noted that the output from the AND circuit 94 is also coupled to the previous word register 44' including the delay line 104 and the OR circuit 106.

Simultaneously with the gating of an output word through the AND gate 94, the control lead 108 to the input buffer circuit 32' produces a new serial binary input word on lead 110. As mentioned above, the new word is transmitted through the OR circuit 56 into the smallest word register 36' where it is immediately compared with the word from register A. However, it will be recalled from the description of Fig. 2 that it is helpful to identify words which are smaller than the previous output word. In Fig. 2 and in the description following the discussion of Fig. 2, these words were identified by an asterisk. In the circuitry of Fig. 6, these words are identified by the insertion of a pulse in a time slot designated the "mark" time slot, which is reserved for this purpose. It may be noted from Fig. 5 that the mark time slot appears in the next more significant digit position following the remainder of the binary word. Thus, when a mark pulse is present in a word, it appears to be larger than any unmarked word. The reason for the selection of this particular digit place is for convenience in the selection of the smallest word to be entered in register 36'. By making all of the words which are to be utilized in the next sequence appear to be large words, the smallest word register 36' will automatically receive the proper word to complete the current sequence.

The circuit for marking input signals which are smaller than the previous output word includes the subtractor 112 and the AND circuit 114. The new word is applied to the minuend input lead 116 of the subtractor 112 and the previous output word is applied to the subtrahend input lead 118 of the subtractor 112. A sign bit word pulse is applied to the AND gate 114 on lead 120 to examine the sign of the output from subtractor 112. If the new word is smaller than the previous output word, the resultant sign bit is gated through the AND circuit 114 and is inserted in the mark time slot of the new word by the OR circuit 58. The third input to the AND circuit 114 is derived from the output of inhibit unit 96 coupled through the one-digit period delay line 122. This input precludes the transmission of a mark signal except during the first word period in which the ring counter 68 is in the A state. Otherwise, signals

could readily be inserted into the register 36' from AND circuit 114 during word periods when no new word is appearing on lead 110 at the output of buffer circuit 32'.

When all of the words in registers A through F and register 36' are marked, it is desirable to eliminate all of the "mark" pulses in the stored words and start a new sequence of words. This operation is implemented by the AND circuit 124, the inhibit unit 52, and the lead 128 connected to inhibit circuits included in each of registers A through F. Following a complete cycle when the smallest word is being gated through AND unit 94 to the output buffer circuit 34', lead 130 to the AND circuit 124 is energized. In addition, a word pulse occurring in the mark digit position is applied to lead 132 at the input of AND unit 124. A tap 134 at the end of the delay line 50 samples the mark digit position of the word being gated out of the smallest word register 36'. If this smallest word has a pulse in its mark position, each of the six words in registers A through F is also characterized by having a pulse in its mark digit position. Accordingly, a pulse at the output of the AND circuit 124 is applied both to inhibit unit 52 to eliminate the mark in the smallest word and also is applied on lead 128 to inhibit circuits associated with registers A through F to eliminate the mark pulses from the words stored in these registers.

In starting sequences through the apparatus, before any information is admitted to registers A through F and register 36', input words which are made up entirely of the binary symbol "0" are employed. At the end of a message, a similar group of closing signals made up entirely of the binary symbol "1" are employed to indicate the end of the list. Although this precludes the use of sequences having all "1's" or all "0's" as words on the unsorted tape, the circuitry is improved and simplified by this convention. Regarding other limitations, it may also be noted that the logic circuitry is arranged to sort only only positive numbers, as the sign bit is reserved for use at the output of the subtractors.

When the circuit of Fig. 6 is first energized, it is desirable to clear the registers in memory circuit 46 and the register 36'. This is accomplished through the use of a control switch 136, the inhibit unit 138, and the memory circuit 140. The switch 136 has three positions, the "off" position, the "warm-up" position, and the "operate" position. The circuit operation when the switch is turned from the "off" to the "warm-up," and from the "warm-up" to the "operate" position, will be presented in the first and second following paragraphs.

When the switch 136 is turned from the "off" to the "warm-up" position, the memory circuit 140 is set to the "0" state. Under these conditions, digit pulses applied to the normal input lead 142 of inhibit unit 138 are transmitted on lead 135 to clear registers A through F. The lead 144 at the output of memory circuit 140 is also coupled to a normal input of the inhibit unit 54 in the delay loop of the register 36'. With no pulses appearing on lead 144, transmission of signals through the register 36' is prevented. Accordingly, all of registers A through F and 36' are cleared. Meanwhile, the contacts associated with the lower deck of switch 136 have permitted the interconnection of the power supplies designated 146 with the electrical circuits shown in Fig. 6 and designated 148 in the lower left-hand corner of Fig. 6. It is to be understood, of course, that the single lead is representative of the various required connections from power supplies to the active circuit components.

Now, when the switch 136 is turned to the "operate" position, the next subsequent sign bit word pulse sets memory circuit 140 to the "1" state, blocks the transmission of pulses through inhibit unit 138, and enables the circulation of signals through registers A through F and register 36'. In addition, the input and output tapes

150 are enabled by signals from lead 144. The data processing circuit is now in condition to receive input signals from the buffer circuit 32'.

The circuit of Fig. 7 is a detailed logic circuit of a portion of the circuit of Fig. 6. More specifically, the switching circuitry associated with the memory circuit 46 is shown in somewhat greater detail. The six-stage ring counter 68 of Fig. 6 is shown at 68' at the right-hand side of Fig. 7. When the ring counter is in state A, the AND circuit 152 is enabled during each digit period by signals from the master clock pulse source 154. The pulses at the output of AND circuit 152 enable AND circuits 156 and 158 to couple the information from register A to the external interchange circuitry. In addition, the output signals from AND unit 152 are applied to the inhibit unit 160 to prevent recirculation of the signals in register A.

When the ring counter 68' is in a state other than the A state, digital information circulates through the delay loop of register A including the OR circuit 162, the delay line 164, the inhibit unit 165, the amplifier 166, the inhibit unit 160, and the one-digit period delay unit 168. The connection from lead 128' to the inhibit unit 165 for the elimination of mark pulses, and the connection from lead 135' to inhibit unit 160 to clear register A are also shown in Fig. 7. The location of the delay unit 168 in the recirculation path of register A permits switching and circulation of digital information through the interchange circuitry during the guard space provided by the sign bit which is located between successive binary words. The AND circuit 170 associated with register B corresponds to the AND register 158 of register A. In addition, the AND circuits 172 and 174 correspond to the AND circuits 156 and 152, respectively, of register A. The OR circuit 176 receives signals from the AND units 158 and 170, for example, at the outputs of registers A through F, and couples these signals to the comparison and interchange circuitry. The remaining lettered registers C through F also tie in with the ring counter 68', the OR circuit 176, and the other principal circuit components as indicated schematically in Fig. 7.

In the circuit of Figs. 6 and 7, it has been assumed that the logic circuits themselves include no delay, and that the delay is all lumped in the delay circuits. At high speeds of operation, some time will, in fact, be required for the operation of the logic circuits. Under these circumstances, the delay circuits are normally reduced in value where necessary to compensate for the small delay of the logic circuits so that pulses are synchronized at the inputs of the logic circuits.

More particularly, if the units 52 and 124 should in actual operation include a finite amount of delay, it is necessary that the word pulse applied to lead 132 of the unit 124 occur before the mark time period by whatever fraction of a time period is required to pass through the units 52 and 124. Similarly, under such circumstances, the tap 134 is located near the end of the delay line 50, such that the pulse appearing on lead 134 occurs in time coincidence with the word pulse appearing on lead 132.

In the illustrative apparatus shown in Figs. 6 and 7, input binary numbers were sorted in accordance with the magnitude of the number. It is to be understood that other items may be sorted in accordance with other properties. For example, punched cards can be sorted in accordance with information appearing in any desired area or field of the card. Similarly, names or other text material may be sorted in alphabetical sequences as indicated in Figs. 1 and 2 of the drawings. It is also noted that the order of the sequences can be arranged to suit the sorting requirements of the user. Thus, for example, when numbers are being sorted, the numbers may be arranged in increasing or decreasing sequences.

It is to be understood that the above-described ar-

rangements are illustrative of the application of the principles of the invention. Numerous other arrangements may be devised by those skilled in the art to implement the "snowplow" method of sorting without departing from the spirit and scope of the invention.

What is claimed is:

1. In a data processing circuit for sorting input numbers into sequences in numerical order, single serial storage means for supplying input numbers, an output circuit, a principal number register for receiving and storing a plurality of said input numbers from said single serial storage means, an additional register for storing the next number to be applied to said output circuit, means for successively comparing each number in said principal register with the number in said additional register, means for interchanging the positions of the compared numbers when the number in the principal register is less than the number in said additional register, means for transmitting the number in said additional register to said output circuit following each of said succession of comparisons, means for marking each number in said additional register which is smaller than the last output number to make it appear larger than any input number, and means for deleting the marks applied to each number when all of the numbers in said two registers are marked.

2. In a data processing circuit for sorting input numbers into sequences in numerical order, means for supplying input numbers, an output circuit, a principal number storage means for a plurality of said numbers, an additional storage means for storing the next number to be applied to said output circuit, means for marking each number in said additional storage means which is smaller than the last output number to make it appear larger than any input number, and means for deleting the marks applied to each number when all of the numbers in said two storage means are marked.

3. In a data processing circuit for sorting input numbers into sequences in numerical order, means for supplying input numbers, an output circuit, a principal number register for storing a plurality of said input numbers, an additional register for storing the next number to be applied to said output circuit, means for successively comparing each number in said principal register with the number in said additional register, means for interchanging the positions of the compared numbers when the number in the principal register is less than the number in said additional register, and means for transmitting the number in said additional register to said output circuit following each of said succession of comparisons.

4. In a data processing circuit for sorting input digital words into sequences in accordance with a predetermined order, means for supplying input words, an output circuit, a principal storage means for a plurality of said words, an additional storage means for storing the next word to be applied to said output circuit, means for successively comparing each word in said principal register with the word in said additional register, means for interchanging the positions of the compared words when the word in the principal register precedes the number in said additional register in accordance with said predetermined order, means for transmitting the word in said additional register to said output circuit following each of said succession of comparisons, means for marking each word in said additional storage means which precedes the last output word in said order to make it appear to follow any possible input word, and means for deleting the marks applied to each word when all of the words in said two storage means are marked.

5. In a data processing circuit for sorting input digital words into sequences in accordance with a predetermined order, means for supplying input words, an output circuit, a principal storage means for a plurality of said words, an additional storage means for storing the

11

next word to be applied to said output circuit, means for marking each word in said additional storage means which precedes the last output word in said order to make it appear to follow any possible input word, and means for deleting the marks applied to each word when all of the words in said two storage means are marked.

6. In a data processing circuit for sorting input digital words into sequences in numerical order, means for supplying input words, an output circuit, a principal storage means for a plurality of said words, an additional storage means for storing the next word to be applied to said output circuit, means for successively comparing each word in said principal register with the word in said additional register, means for interchanging the positions of the compared words when the word in the principal register precedes the word in said additional register, and means for transmitting the word in said additional register to said output circuit following each of said succession of comparisons.

7. In combination in a sorting apparatus, an input circuit comprising only a first single serial storage means for successively supplying input binary words which are to be sorted, an output circuit comprising only a second single serial storage means for receiving and storing sorted sequences of input words, previous output word register means coupled to said output circuit for storing the most recent one of the words received by said

12

output circuit, first means coupled to said input circuit for storing only one input word, second means for storing a plurality of input words, means for comparing the value of said one input word in said first means with the value of the word stored in said previous output word register means and for increasing the value of said one input word if the value of said one input word is less than the value of the word stored in said previous output word register means, means for then successively comparing the value of said one input word with the values of the words stored in said second means, and means for interchanging the positions of the compared words in said first and second means when the word in said second means is less than the word in said first means.

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