Oct. 25, 1960 G. N. PACKARD 2,957,945

TIMING CIRCUIT

Filed Dec. 24, 1957 2 Sheets-Sheet 1

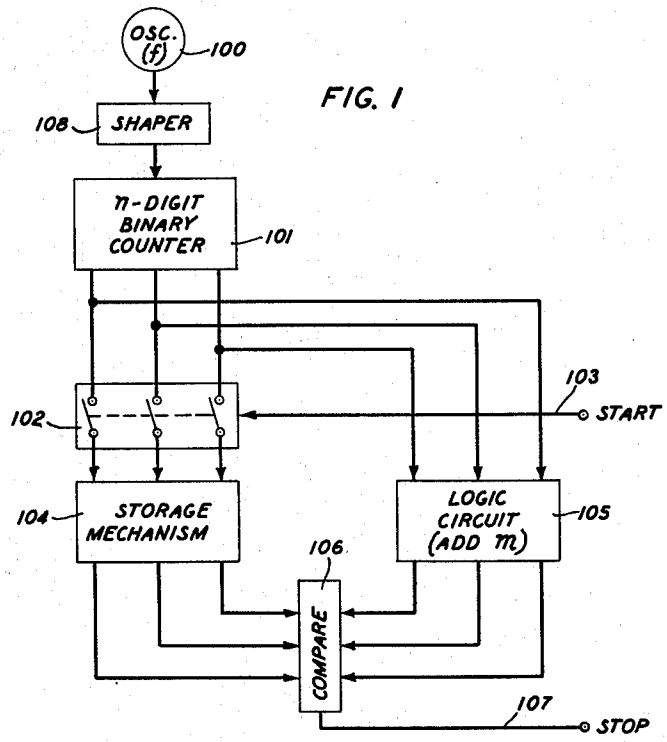

FIG. 1

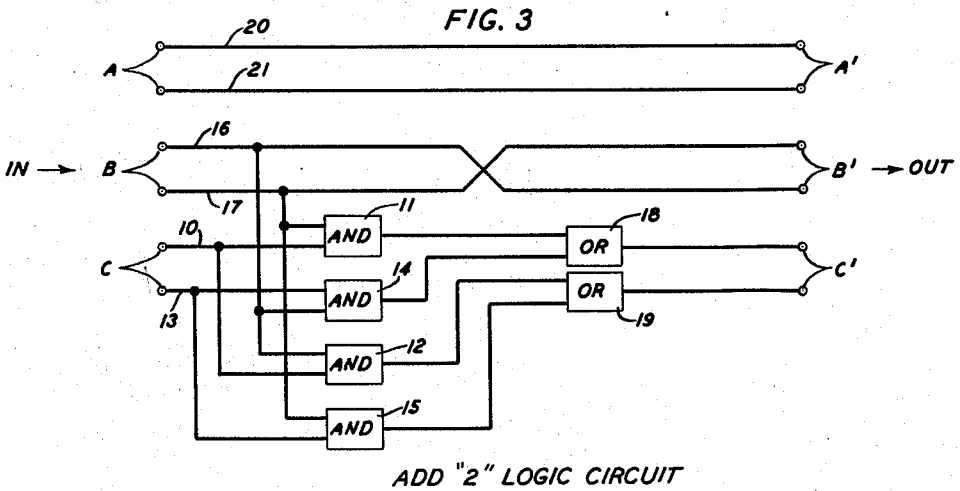

FIG. 3

ADD "2" LOGIC CIRCUIT

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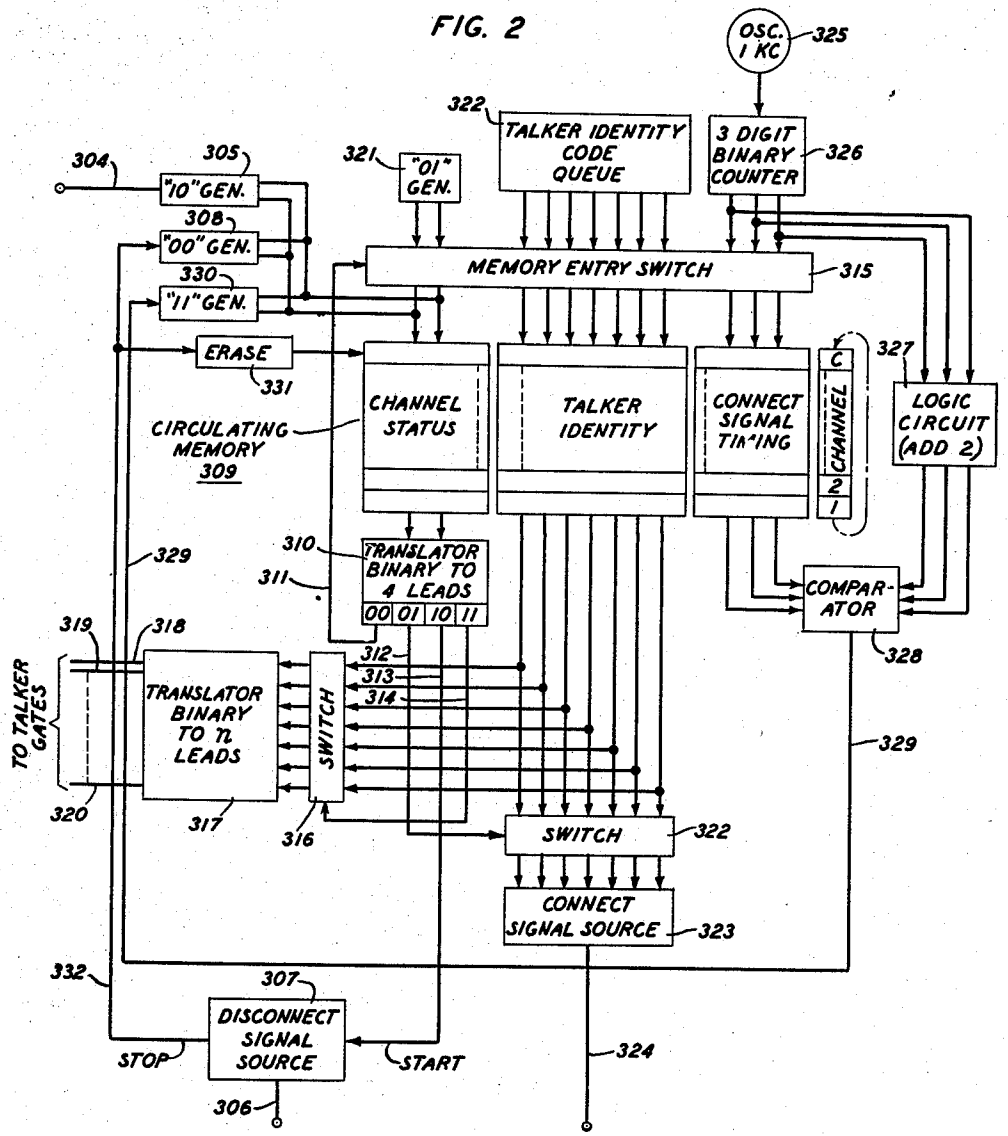
FIG. 2



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TIMING CIRCUIT

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8 Claims. (Cl. 179—15)

This invention relates to timing circuits and, more particularly, to means for simultaneously timing a plurality of overlapping and randomly initiated operations.

It is frequently desirable to time accurately a large number of operations which are initiated in a random fashion. In a time assignment speech interpolation system, for example, where a large number of speech signal sources are connected to a lesser number of transmission channels on a time division basis, it is necessary to identify each speech signal sample before it is transmitted. This is conveniently accomplished by first transmitting a source-identifying code over the transmission channel and following this code with the appropriate speech signal. In this way, the identity of the proper listener can be ascertained at the receiving end of the transmission channel.

In order to properly identify such a speech signal source, however, it is necessary that the source identity code be sustained for a minimum interval to insure proper reception and recognition at the receiving terminal. On the other hand, this identity code should be as short in duration as is possible consistent with recognition in order to avoid excessive waste of channel time and "freeze-out" of the speech signal. It is therefore necessary to provide means for timing the duration of the identity codes in order to meet both of the above requirements.

The timing means which is suitable for controlling the duration of identity code signals in a time assignment speech interpolation system must be capable of simultaneously timing the duration of a large number of different identity codes. Furthermore, a new identity code must be transmitted each time a speech signal source becomes newly active. Since speech spurts occur on a random basis for large numbers of talkers, the identity codes are also initiated on a random basis and may very well be overlapping in time.

Time assignment speech interpolation systems, however, are not the only systems requiring simultaneous timing. Any other common control or programing system such as, for example, computers or telephone central office control equipment, also require such timing functions. Previous timing schemes require completely regular sequences of operations, and thus are not suitable for randomly initiated operations, or require separate timing means for each of the operations to be controlled, and thus are cumbersome, expensive and unreliable.

It is an object of the present invention to control a large number of simultaneous or overlapping operations with a minimum of equipment.

It is a further object of the invention to time a plurality of randomly initiated intervals with a high degree of accuracy and precision.

It is a more specific object of the invention to terminate, after a specific predetermined interval, a large number of operations which are initiated on a purely random basis.

In accordance with the present invention, a plurality of successive and regularly recurring binary timing codes

are generated. A single one of these codes occurring at the beginning of each interval to be timed is gated into a storage mechanism. The storage mechanism, or memory, is of the type which has the capacity to store a large number of separate bits of binary information and, furthermore, is one which regularly presents these bits of information on a single set of output leads. The output of the code generator is also introduced into a logic circuit. The logic circuit merely serves to add a given fixed binary number to any binary number presented at its input. A comparison or coincidence circuit compares the outputs of the storage mechanism and the logic circuitry and generates a signal to terminate the timed interval when these outputs are identical.

The operation of the multiple timing circuit of the present invention can be better understood by recognizing the basic timing information provided by a regularly recurring cycle of binary codes. The combination of the present invention serves to recognize the particular code at which timing is to begin and to generate the proper code for terminating the timed interval. The duration of the timed interval is then the difference between the total time required for the generation of a complete cycle of the binary codes and the time required to generate the number of codes corresponding to the number added by the logic circuitry. That is, coincidence in timing codes will not occur until the binary code generator goes through the entire code sequence and returns to the number which is less than the original code by a number equal to the number added.

Since any number of discrete codes can be generated, any number of different intervals can be simultaneously timed. The duration of these intervals can be chosen to equal any integral multiple of the basic timing length of a single code element by adding the proper number. Furthermore, these intervals are not constrained to be initiated at any predetermined times. They may occur at random and in any succession possible.

These and other objects and features, the nature of the present invention and its various advantages, will appear more fully upon consideration of the attached drawings and the following detailed description of the drawings.

In the drawings:

Fig. 1 is a block diagram of a multiple timing circuit in accordance with the present invention;

Fig. 2 is a block diagram of a time assignment speech interpolation system utilizing a timing circuit in accordance with the present invention; and

Fig. 3 is a block diagram of a logic circuit suitable for performing the logical function of adding two to its input.

Referring more particularly to Fig. 1, there is shown a multiple timing circuit in accordance with the present invention comprising an oscillator **100** which produces at its output oscillations at a frequency f. These oscillations are introduced into pulse shaper **108** which shapes the sinusoidal oscillations from oscillator **100** into square top pulses having a repetition rate equal to the frequency of oscillation. These pulses are introduced into binary counter **101**.

Binary counter **101** is of any form known in the art such as, for example, a plurality of binary cells or flip-flops, and recurrently produces on its output leads the binary representations of the numbers one through 2^n, in succession, where n represents the number of digits in the binary code which is used to represent these numbers. The number n may have any value desired. In the illustrative embodiment of Fig. 1, n is assumed to be equal to three and, thus, binary counter **101** has three output leads. In this case, counter **101** will generate the binary members one through eight in succession. The out-

put of binary counter **101** is introduced into a gate circuit **102** which provides switch connections between the individual ones of its three input leads and the corresponding ones of its three output leads. Gate circuit **102** is operated by a signal on lead **103**.

The output of gate **102** is introduced in a storage mechanism **104**. Storage mechanism **104** is of the type which will store a plurality of binary bits of information for an indefinite length of time. Furthermore, the information content of storage mechanism **104** is continuously or regularly presented on three output leads. Thus, the binary code introduced into storage mechanism **104** is presented, for at least a portion of the time, on its three output leads.

The output of binary counter **101** is also introduced into logic circuit **105**. Logic circuit **105** is a circuit arrangement capable of performing the logical operation of adding a fixed number to any binary number presented at its input. Thus, logic circuit **105** has been represented by the logical operation of "add m" where m can be any number less than 2^n. There is presented on the output of logic circuit **105** the binary representation of a number which is greater than the binary number introduced at its input by a quantity m.

The output of logic circuit **105** and the output of storage mechanism **104** are both introduced into a compare circuit **106**. Compare circuit **106** can be any type of coincidence recognizing gate arranged to produce an output if, and only if, the input on each lead is identical to the input on a paired lead. Compare circuit **106** therefore makes a digit-by-digit comparison between the output of logic circuit **105** and the output of storage mechanism **104**. When these outputs are identical, a distinctive signal such as, for example, a change from no pulse to pulse, is introduced on lead **107**.

The operation of the timing circuit shown in Fig. 1 is as follows. Simultaneously with the initiation of the operation to be timed, a signal is introduced on lead **103**. This signal operates gate **102** to gate a single binary number from binary counter **101** to storage mechanism **104**. This binary number will be that number at which counter **101** happens to be at the particular instant that the start signal on lead **103** enables gate **102**. Assuming that the timed operation can start at any time, the actual choice of binary numbers is completely random and may comprise any number included in the output of counter **101**.

This particular binary number is stored in storage mechanism **104** and is presented on its output leads. At the same time, logic circuit **105** will add the binary number m to this particular binary code. Since the input of logic circuit **105** is connected directly to the output of binary counter **101**, logic circuit **105** will receive a new binary code each time counter **101** is advanced one step. The output of logic circuit **105** will therefore comprise a series of binary codes identical to the output of counter **101** but advanced in time by an amount required to generate the binary number m. Compare circuit **106** compares the binary code stored in storage mechanism **104** with the series of binary numbers provided on the output leads of circuit **105**. When a position is reached in this series at which the output of logic circuit **105** is identical to the number stored in storage mechanism **104**, compare circuit **106** will produce an outupt on lead **107** which may be utilized to terminate the timed operation.

It can be seen that the duration of the timed interval is related to the frequency f of oscillator **100**, the number n of digits produced by counter **101** and the number m added by logic circuit **105** by

$$T=\frac{1}{f}(2^n-m)$$

where T is the length of this period and the other symbols are as defined above. It can be seen that by choosing suitable values for f, n and m, a timing interval of any desired length may be provided. This interval is the time required for binary counter **101** to proceed in its count from any given number through nearly a complete cycle to a number which is less than the given number by a number m.

If storage mechanism **104** is designed to store more than one binary code at a time and to present all of the stored codes on its output leads within the time period required for each step of binary counter **101**, the timing circuit of Fig. 1 can be used to simultaneously time a large number of operations which are initiated in a random manner. Such a timing circuit will be described in connection with a time assignment speech interpolation system such as that disclosed in a copending patent application of F. A. Saal and I. Welber, Serial No. 686,468, filed September 26, 1957, since matured into U.S. Patent 2,935,569, issued May 3, 1960. It is to be understood, however, that the timing arrangements are by no means limited to a time assignment speech interpolation system. They are equally applicable to any other common control or programing systems such as computers or electronic switching systems for telephone central offices.

When making use of expensive transmission facilities such as the channels in a transatlantic cable, it is most economical to make full use of all of the available channel time. Various systems for saving channel time have been proposed which utilize the statistical fact that telephone conversations use the facilities in one direction on the average for less than one-third of the time. Therefore, by interconnecting the two parties only when the line is active, large savings in channel time may be effected. The terminal switching facilities which perform this function have been termed "time assignment speech interpolation" systems or, more conveniently, "TASI" systems. Such a TASI system can therefore utilize a fixed number of transmission channels to accommodate a far larger number of talkers, on the order of three times as many talkers as channels.

Some of the TASI systems heretofore proposed, such as that disclosed in the above-identified application by Saal and Welber, have interconnected talker lines and transmission channels by means of time separation multiplex switching (TSM switching). These systems utilize the principle that speech, or any other signal, can be adequately represented by samples spaced in time, provided the sampling rate is at least twice the highest frequency component of the signal to be represented. The interconnection of talker lines and transmission channels are therefore made by simultaneously gating a particular talker line and a particular transmission channel onto a common multiplex bus for the same sample interval. By interleaving speech samples from all the active talkers and gating them to proper transmission channels at a sufficiently high rate, speech signals on all of the talker lines can utilize the same multiplex bus and yet each be accurately reproduced on the individual transmission channels.

In TSM switching TASI systems, the activity of the individual talkers is ascertained by systematically scanning speech detectors connected to the individual talker lines and synchronously generating a talker identity code for each active talker. A circulating or re-entrant memory is used to register the assignment of a particular active talker to a particular idle channel. The contents of the memory are then used to control the multiplex switching operation. A complete TASI system embodying the operation described above is disclosed in the above-mentioned application by Saal and Welber, Serial No. 686,468, filed September 26, 1957.

In such a TASI system, it is an essential function to coordinate talker-to-channel assignments at the transmitter with channel-to-listener assignments at the receiver. For this purpose, in-band multifrequency signaling tones are transmitted over an idle channel to indicate the proper listener connection to be made to that channel. These tones, however, must be sustained for a sufficient

length of time to insure their accurate reception, i.e., on the order of 10 milliseconds with present filters of economical design. Furthermore, large transmission systems having many talkers demanding connection at one time require a connect signaling arrangement which will accommodate more than one talker simultaneously.

In accordance with the present invention, a timing code is generated and associated with each talker identity code as the talker becomes active and is registered in the circulating memory. These timing codes are also introduced into a logic circuit which adds a fixed number to the timing code. In accordance with the operation described above, a comparison made between the output of a logic circuit and the contents of a memory will indicate, at the instant that the timing codes are identical, that the signal interval is over.

It is apparent that since a lesser number of transmission channels are provided than the total number of talker-listener pairs to be accommodated, it is not only necessary to make assignments of talkers to channels, but it was necessary to change these assignments when active talkers become inactive and other talkers become active. A portion of a TASI transmitter will be described which is suitable for making these assignments and for generating the necessary signals.

Proceeding to Fig. 2, a talker identity code queue **322** is shown. Queue **322** stores the identity codes of those talkers which have become active in the order in which their activity was initiated. Queue **322** thus serves as a programer for the TASI transmitter illustrated in Fig. 2. The means by which these talker identity codes are generated and introduced into queue **322** forms no part of the present invention and will not be described here. It is sufficient for the purposes of the present invention to assume that queue **322** generates seven digit binary codes which identify particular talker lines and which indicate an active condition on those talker lines.

For convenience, circulating memory unit **309** will now be described. Memory unit **309** is a re-entrant type of memory unit such as, for example, a plurality of parallel delay loops having a capacity of *c* words of 12 "bits" each, where *c* is the total number of transmission channels available. These 12 bits are circulated in synchronism with each other at a rate of eight thousand revolutions per second. Seven of these 12 bits represent the particular talker identity code provided by queue **322**. Three more of these bits represent connect signal timing information which will be more fully described below. The remaining two bits called "channel status bits" carry information as to the present status of the channel which is associated with that particular time slot in the memory unit, indicated by the number in the channel boxes along the right side of memory **309**. The function of the channel status digits will now be described.

The two channel status digits permit the representation in binary form of any one of four different states or conditions of each individual transmission channel. For convenience, these states and the corresponding binary code representations have been chosen as follows:

State:	Code
Channel available for use ("Idle")	00
Channel being signaled over for connection ("Connection")	01
Channel being held for disconnection ("Disconnection")	10
Channel being used for speech ("Busy")	11

A translator **310** is provided for taking these two digit binary representations and providing an output signal on one-out-of-four output leads corresponding to the particular binary number introduced at its input. Thus, a binary "00" produces a signal on output lead **311**, a binary "01" produces an output on lead **312**, a binary "10" produces an output on lead **313** and a binary "11" produces an output on lead **314**.

Memory unit **309** is illustrated as a plurality of successive "slots" numbered along the right hand side to correspond with the *c* channels of the transmission system. These "slots" (between successive horizontal lines) are illustrative of the time slots which appear in a circulating delay type of memory unit. Since memory unit **309** is a circulating or re-entrant type of memory, channel one shown in the slot labeled "1", that is, the "bottom" slot, in the next time interval appears in the position of the slot labeled "*c*," that is, the "top" slot. At the same time, all of the other channels advance one time slot so that channel two is now in the bottom slot and channel *c* is now in the slot second from the top. This circulation continues at the rate of eight thousand revolutions per second.

The circuitry which is shown as being connected to the bottom slot, for example, translator **310**, is actually connected to a fixed position in the circulating memory loop such that all other channel time slots proceed past this position in regular succession. Translator **310**, for example, therefore "sees" the channel status digits of channel one, then channel two and so forth, down to channel *c*, and then to channel one again. Furthermore, translator **310** sees the output of a bottom slot as it passes from this slot to the top slot. In this way, control functions which are governed by the output of the bottom slot are operative upon the information in the top slot.

As described above, a binary "00" in the channel status portion of memory unit **309** will produce an output from translator **310** on line **311**. This output on line **311** operates a memory entry switch **315** which comprises 12 separate switches connecting 12 input leads to 12 corresponding output leads. Memory entry switch **315** thus gates the talker identity code from queue **322** into the top slot position in memory **309**. Since memory **309** is of the circulating or re-entrant type, the channel status digits which produce this output on lead **311** are taken from the same time slot into which switch **315** introduces this talker identity code. Since each time slot of circulating memory unit **309** is uniquely related to a particular transmission channel, this particular talker identity code has now been assigned to a particular channel.

Circulating memory unit **309** will continuously circulate this talker identity code and maintain this assignment of the particular talker to the particular channel for an indefinite length of time. A definite removal or erasure of this assignment is required to disassociate this talker and this channel.

If the binary number "11" is in the channel status digit portion of the memory unit **309**, an output is produced by translator **310** on output line **314**. This output operates a switch **316** which samples the talker identity code in memory unit **309** and delivers this code sample to a translator **317**. This sampling operation is nondestructive and hence the talker identity code will continue to circulate in memory unit **309**. Translator **317** translates the seven digit talker identity code to an output on one out of *n* output leads, where *n* is the total number of talker lines connected to the TASI system. Thus, the binary number one represented by "0000001," produces an output on lead **318**. A binary two ("0000010") produces an output on lead **319** and a binary *n* produces an output on lead **320**. The signals on these output leads operate the corresponding talker gates which connect the individual talkers to a time division bus from which they are synchronously gated to the proper transmission channel. If this channel gating arrangement is synchronized with memory unit **309**, it can be seen that the talker identity code in memory unit **309** operates to gate the talker corresponding to that code onto the time separation multiplex bus at the same instant and for the same interval that the TSM bus is connected to the transmission channel assigned to that particular time slot in the memory.

Before the TASI transmitter illustrated in Fig. 2 can

begin sending a particular talker's speech spurt, however, it must first indicate the proper listener for which that particular speech spurt is intended. Connect signaling is therefore required in the TASI transmitter to perform this function.

To accomplish connect signaling, binary signal generator 321 continuously produces on two output leads the binary number "01". As described above, this binary code indicates that a channel is being signaled over for connection. When memory entry switch 315 is enabled by a pulse on output lead 311 of translator 310, it gates this "01" binary code into the channel status digit portion of memory unit 309. Furthermore, this "01" code is introduced into the same time slot in memory 309 that the talker identity code is introduced from queue 322. Thus, there is associated with the identity of this talker and the transmission channel assigned to this particular time slot, the information that this particular channel is being used for connect signaling.

This connect signaling code upon arriving at the bottom of circulating memory unit 309 is introduced into translator 310 and produces an output on output lead 312. The output on lead 312 enables switch 322 which samples that particular talker identity code and delivers the sample to connect signal source 323. Connect signal source 323 produces a multifrequency tone signal which is frequency code to the same talker identity as is introduced at its input. Such a connect signal source is disclosed in the copending application of R. L. Carbrey, Serial No. 430,181, filed May 17, 1954. It comprises seven frequency sources separately gated by the digits of the talker identity code and fed into a summing amplifier. Any other frequency coding source would, of course, also be suitable.

Connect signal source 323 produces on connect signal bus 324 this frequency coded signal. Connect signal bus 324 may in turn be connected to the time separation multiplex bus and be gated to the proper transmission channel in synchronism with the operation of circulating memeory unit 309. Thus, prior to the actual transmission of the speech spurt over a particular transmission channel, a frequency coded signal is transmitted over that same channel indicating to the receiver to which listener that channel is to be connected.

For the receiver to properly identify this connect signal, it has been found that the multifrequency tone must be sustained for a period of about five to 10 milliseconds. It is this timing which it is the object of this invention to accomplish.

In accordance with the present invention, a one thousand cycle oscillator 325 is used to drive a three-digit binary counter 326. Binary counter 326 continuously produces on its three output leads the binary representations of the numbers one through eight, respectively, in succession. When memory entry switch 315 is operated by a pulse on lead 311, indicating that an idle channel is available, this three-digit binary code is gated into the connect signal timing portion of memory unit 309 simultaneously with the talker identity code and the "01" channel status digits. Thus, there is associated with each talker identity code as it is registered in the memory unit 309 a unique three-digit binary code which is indicative of the particular instant at which that talker identity code is registered. The output of binary counter 326 is also introduced into a logic circuit 327 which performs the logical function of adding "two" to the number presented at its input. There are thus produced on three output leads of logic circuit 327 the binary representations of the numbers one through eight in succession, but these numbers appear in time two units before the corresponding number appears on the output of binary counter 326.

After leaving logic circuit 327, each of these advanced timing codes is introduced into a comparator circuit 328. The connect signal timing digits stored in memory unit 309 are also introduced into comparator circuit 328. The function of comparator circuit 328 is to make a digit-by-digit comparison between the three-digit code introduced from logic circuit 327 and the three-digit codes introduced from memory unit 309. This comparison may be accomplished by any one of the means well known in the art such as, for example, by the use of "coincidence" gates.

Since the information in memory unit 309 is circulating at an eight thousand cycles per second rate, each timing code stored in memory unit 309 is presented to comparator circuit 328 eight thousand times in each second. The output codes from logic circuit 327, however, will be presented to comparator circuit 328 only one thousand times per second. Each individual output code from logic circuit 327 will therefore be held in comparator circuit 328 for a period of eight complete revolutions of circulating memory unit 309. Each output code from logic circuit 327 will then be compared with the entire contents of the connect signal timing portion of memory unit 309.

The output of logic circuit 327 and the particular connect signal timing code stored in memory unit 309 will coincide only after binary counter 326 has made a complete cycle and arrives at the number which is two less than the particular timing code gated into circulating memory 309. The interval required for this to occur can easily be controlled by adjusting the oscillating frequency of oscillator 325 and the particular number which is added in logic circuit 327. In the illustrative embodiment in Fig. 2, where oscillator 325 has a frequency of one thousand cycles per second, a new timing code is generated once each millisecond and the time required to run through a complete cycle of binary codes is eight milliseconds. The duration of the timed interval will therefore be six milliseconds, that is, eight minus two.

Upon recognizing identical binary codes at its two inputs, comparator circuit 328 produces a pulse output on lead 329. This pulse is used in a control circuit 330 to erase the "01" connect signal status digits from the channel status portion of memory unit 309 and to write in its place the digits "11." This indicates to the memory unit that the connect signaling interval is over and that it may now begin transmitting the actual spurt of speech. This erase and write function may be accomplished, for example, by momentarily opening up the memory loops for the channel status digits in memory unit 309 and inserting the new code. The "11" digits in translator 310 cause switch 316 to be operated and by way of translator 317 cause the proper talker gates to be operated.

The connect signal timing portion of the memory unit 309 and the timing code have been provided to allow more than one talker to be signaled for connection at one time. This is necessary because, in a large system, many talkers will initiate speech spurts within the same connect signaling interval. If a single-acting timer were used, the last talker to become active would be required to wait until all previously active talkers had received connect signaling service. This unduly long wait would constitute an additional "freeze-out" and impair service accordingly.

In accordance with the illustrative embodiment of the present invention, binary counter 326 and logic circuit 327 have been provided to enable an unlimited number of talkers to be signaled for connection simultaneously. These connect signaling intervals may be initiated at random throughout the entire cycle of binary counter 326 and more than one such interval can be initiated on the same connect signal timing code.

To complete the description of the TASI transmitter shown in Fig. 2, the process for disconnection of a no longer active talker will now be described. A pulse on lead 304 occurring in the time slot assigned to a particular talker indicates that that talker is no longer active

and that disconnection is now desired. This pulse on lead **304** operates a signal generating circuit **305** which erases the "11" active code in the channel status digit portion of memory unit **309** and substitutes therefor the channel status code "10" indicating that the channel is now being used for disconnect signaling. This channel status code "10," upon arriving at translator **310**, produces an output on lead **313**. This output is used by disconnect signal source **307** to produce a disconnect signal which is transmitted to the receiver to terminate this assignment. Specific circuitry for accomplishing this result is disclosed in the copending application of F. A. Saal and I. Welber, Serial No. 686,468, filed September 26, 1957. In any event, the disconnect signal is initiated by a pulse on lead **313** and appears on lead **306**. Like lead **324**, lead **306** may be connected to the time division bus and be synchronously gated to the proper transmission channel or may be coded and transmitted over a separate transmission channel.

At the termination of a disconnect signaling interval, a pulse is produced on lead **332**. The pulse on lead **332** operates a signal generator **308** and, simultaneously an erase circuit **331**. Erase circuit **331** erases the entire contents of that particular time slot of memory unit **309**. Signal generating circuit **308** substitutes in the channel status portion the digit "00." This "00" code indicates that the channel is now idle and may be reassigned.

In Fig. 3 there is shown a logic circuit which is suitable for adding the number two to a three-digit binary number and thus is suitable for logic circuit **327** in Fig. 2. The operations necessary for adding two to a three-digit binary number are as follows. The least significant digit of the binary number always remains the same. The second least significant digit of the binary number is always inverted, that is, if the digit is a one it becomes a zero and if the digit is a zero, it becomes a one. The most significant digit of the three-digit binary number remains the same if the second least significant digit is a zero and is inverted if the second least significant digit is a one. The circuitry of Fig. 3 is arranged to perform these operations on three binary digits A, B and C where A is the least significant digit and C is the most significant digit. Each of these digits is preferably represented by the voltage conditions on two separate conductors. For example, to represent a one, one of the conductors might have a positive voltage thereon. The other conductor would have no voltage. To represent a zero, the first conductor would have no voltage thereon and the second conductor would have a positive voltage of the same magnitude as before.

In the logic circuit of Fig. 3, the least significant digit A of the input binary number remains the same and becomes the least significant digit A′ of the output binary number. The second least significant digit B of the input binary number is inverted merely by transposing the first and second conductors **16** and **17**, respectively, carrying the voltage representing this digit, to provide the second least significant digit B′ of the output binary number.

The most significant digit C of the input binary number is treated in the following way. The voltage on a first conductor **10** is simultaneously introduced into two "AND" gates **11** and **12** and the voltage on the second conductor **13** is simultaneously introduced into two more "AND" gates **14** and **15**. "AND" gates **11**, **12**, **14** and **15** are of any well-known configuration producing an output if and only if a positive voltage is introduced on both their input conductors. Such a gate may, for example, be made up of unilateral conducting devices, transistors or vacuum tubes. The voltage on the first conductor **16**, representing the digit value of the second least significant digit B, is simultaneously introduced into the other input conductor of "AND" gates **12** and **14**, while the voltage on second conductor **17** is simultaneously introduced into the remaining input conductor of "AND" gates **11** and **15**. The outputs of "AND" gates **11** and **14** are introduced into "OR" gate **18** while the outputs of "AND" gates **12** and **15** are introduced into another "OR" gate **19**. The outputs of "OR" gates **18** and **19** comprise the most significant digit C′ of the output binary number.

From the arrangement in Fig. 3 it can be seen that the most significant digit C′ of the output number remains the same as the input digit C if the second least significant input digit B is a zero. That is, a zero voltage condition appearing on conductor **16** disables gates **12** and **14**, and a positive voltage appearing on conductor **17** enables gates **11** and **15**. On the other hand, if the second least significant digit B is a one, that is, if a positive voltage appears on conductor **16** and zero voltage appears on conductor **17**, then gates **12** and **14** are enabled and gates **11** and **15** are disabled. In this case, the voltage representations of digits C are transposed and the output digit C′ is inverted.

While only a single logic circuit has been described in connection with the present disclosure, many other circuits known in the art may be substituted to perform this function, i.e., to add a fixed number to a varying input number.

It is to be understood that the above-described arrangements are only illustrative of the numerous and varied other arrangements which could represent applications of the principles of the invention. Such other arrangements may readily be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. Means for simultaneously timing a plurality of overlapping operations comprising recycling code generating means for progressively generating a plurality of discrete code groups, means for storing only selected ones of said code groups, each of said stored code groups being selected at the beginning of a respective one of said operations, means for translating each of said generated code groups into another one of said code groups, means for comparing said translated code groups with each of said stored code groups and means responsive to coincidences between said translated code groups and each of said stored code groups for terminating the respective one of said operations.

2. Means for accurately timing a predetermined interval between two successive operations comprising means for generating a plurality of binary code groups in regular succession, means for storing one of said code groups in response to a first one of said operations, means responsive to said code group generating means for advancing each position in said succession to another of said code groups, means for comparing the contents of said storing means and the output of said translating means, and means for initiating a second one of said operations in response to a coincidence of inputs to said comparing means.

3. A timing circuit for simultaneously timing a plurality of intervals comprising means for successively generating a sequence of binary numbers, means for storing that number of said sequence which is instantaneously generated at the beginning of each of the timed intervals, logic circuitry means for translating each number of said sequence into a different number of said sequence, means for introducing said initial sequence into said logic circuitry means, means for comparing the output of said logic circuitry means and the contents of said storing means, and means for terminating respective ones of said intervals in response to coincidences between said output and said stored codes.

4. In a time assignment signal interpolation system, means for timing the duration of connect signaling comprising means for generating a plurality of regularly spaced dissimilar code groups, means for associating unique ones of said code groups with newly active signal

sources in said system, means for translating said code groups into different code groups, means for deriving a control signal each time the output of said translating means is identical with one of said associated code groups, and means for signaling a connection until each of said control signals is derived.

5. The combination according to claim 4 wherein said translating means comprises means for adding a predetermined code group to the output of said code group generating means.

6. In a signal interpolation system, a plurality of signal sources and corresponding utilization circuits, a lesser plurality of transmission channels, means, including a circulating memory unit, for assigning active ones of said signal sources to idle ones of said transmission channels, and mean for transmitting signals indicating said assignments to said utilization circuits for a predetermined interval, said signal transmitting means comprising a cyclic code generator, means for registering a particular code in said memory unit to correspond to each one of said assignments and to control said signals, binary code addition means adapted to add a fixed binary number to the output of said cyclic code generator, and means for comparing the output code of said addition means and the codes in said memory for terminating said signals when said codes are identical.

7. In a time assignment speech interpolation transmitter, circulating memory means for registering the identifications of active talkers, a timing code generator, means for associating unique ones of said timing codes with said identifications, means for adding a fixed code to said timing codes, means, controlled by said identifications for generating an identity code, means for gating said identifications to said identity code generating means, means controlled by said memory means for enabling said gating means, and means controlled by the output of said adding means for disabling said gating means.

8. Circuit means for simultaneously timing a plurality of randomly initiated operations which comprises recycling binary counting means, means for assigning the output number from said counting means at the initiation of each of said operations to said operation, means for adding a preselected binary number to each output number from said counting means to form a sequence of numbers advanced by said preselected number with respect to said output numbers, means for comparing each of said advanced numbers with each of said assigned numbers to determine coincidences, and means for terminating each assigned operation when and only when a coincidence occurs between the assigned number and one of said advanced numbers.

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