June 9, 1959 M. K. ZINN 2,890,333

DELAY NETWORK

Filed Aug. 19, 1955

FIG. 1

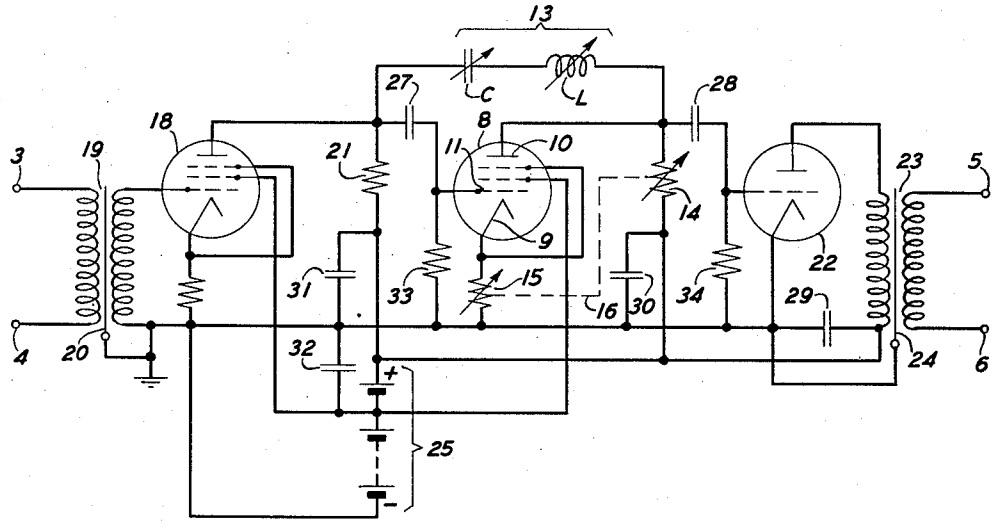
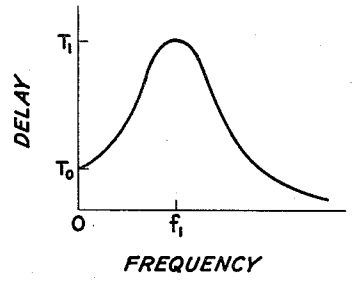


FIG. 2



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2,890,333

Patented June 9, 1959

2,890,333

DELAY NETWORK

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Application August 19, 1955, Serial No. 529,432

3 Claims. (Cl. 250—27)

This invention relates to wave transmission networks and more particularly to adjustable delay networks.

The principal object of the invention is to introduce an adjustable delay in a wave transmission circuit. Another object is to provide such a delay without introducing insertion loss. A further object is to control the delay by adjusting only resistors.

In wave transmission systems such, for example, as television, telephoto or radio systems it is often required to introduce a corrective delay characteristic which can be easily and quickly adjusted in magnitude or shape. It is also desirable that no insertion loss be associated with the delay.

The adjustable delay network in accordance with the present invention is of the all-pass type and thus introduces no loss. The network comprises an electron tube having a cathode, a plate and a grid, a reactive feedback impedance connected between the plate and the grid, and an adjustable output resistor connected between the plate and the cathode. The conductance of the resistor and the transconductance of the tube are substantially equal, thus making the insertion loss zero. Means, preferably under a unitary control, are provided for adjusting both the conductance and the transconductance while maintaining their equality. The conductance is controlled by adjusting the resistor. The transconductance may be adjusted by means of a second adjustable resistor which controls the bias on the grid of the tube. These two resistors may be ganged together under a unitary control. Thus, by operating this single control, the magnitude or shape of the delay characteristic can be adjusted as desired. The delay shape depends upon the choice of the reactive impedance. For example, a hump of delay may be provided. A further adjustment of the delay shape may be provided, if desired, by making the reactive impedance adjustable.

For best results, the delay network is preferably inserted between high impedance at both ends. It may, for example, be employed as an interstage between two other electron-tube stages. The input stage may be a pentode and the output stage of any type having a high grid impedance.

The nature of the invention and its various objects, features and advantages will appear more fully in the following detailed description of a typical embodiment illustrated in the accompanying drawing, of which

Fig. 1 is a schematic circuit of an adjustable delay network in accordance with the invention employed as an interstage between two other stages; and

Fig. 2 shows one type of delay-frequency characteristic obtainable with the network of Fig. 1.

As shown in Fig. 1, the over-all circuit comprises three electron-tube stages connected in tandem between a pair of input terminals **3**, **4** and a pair of output terminals **5**, **6**. The signal wave to be equalized is impressed upon the input terminals **3**, **4** and a suitable load may be connected to the output terminals **5**, **6**. The central stage constitutes the delay network proper. It comprises an electron tube **8** having a cathode **9**, a plate **10** and a control grid **11**. As shown, the tube **8** is a pentode, which has three grids. It will be understood, however, that a triode or other type of tube may be employed instead. A reactive feedback impedance **13** is connected between the plate **10** and the grid **11**, and an adjustable output resistor **14** between the plate **10** and the cathode **9**. A second adjustable resistor **15** is connected in the cathode circuit to control the bias on the grid **11** and, thereby, the transconductance of the tube **8**. The resistors **14** and **15** are preferably ganged together for operation under a single control, as indicated by the dashed line **16**.

The impedance connected to the input end of the delay network is provided by the first stage. As shown, this stage comprises a pentode tube **18**. The input of the tube **18** is connected to the input terminals **3** and **4** through a transformer **19** which has a grounded shield **20** between the windings. The first two stages are coupled through a shunt resistor **21** which ordinarily has a high resistance. The last stage, comprising a triode tube **22**, furnishes the desired high impedance at the output end of the delay network. The output of the tube **22** is connected to the output terminals **5** and **6** through a second transformer **23** with a grounded shield **24** between the windings.

The operating voltages for all three stages are obtained from the source **25**, shown as a battery. The customary by-pass capacitors **27**, **28**, **29**, **30**, **31**, and **32**, of high capacitance, are inserted to separate the power supply from the signal circuits. The resistors **33** and **34** provide grid leaks.

If the feedback impedance **13** has a pure susceptance js, the output resistor **14** a conductance b, and the tube **8** a transconductance g, the voltage transfer ratio R of the delay network is given by

$$R=\frac{js-g}{js+b} \tag{1}$$

Since b and g are maintained equal for all adjustments, it is seen that the modulus of R is always unity. Therefore, like an all-pass network, there is no loss at any frequency.

However, by suitably selecting the impedance **13**, any of a large variety of delay-frequency characteristics may be provided. For example, if the impedance **13** is constituted by the series combination of a capacitor of value C and an inductor of value L, as shown in Fig. 1, a hump of delay is obtained. A typical shape is shown in Fig. 2, in which delay is plotted against frequency. The delay T_0 at zero frequency is

$$T_0=2C/b \tag{2}$$

The maximum delay occurs approximately at the resonant frequency f_1, given by

$$f_1=\tfrac{1}{2}\pi\sqrt{LC} \tag{3}$$

The amount of the delay T_1 at this frequency is

$$T_1=4Lb \tag{4}$$

It is thus seen that T_0 varies directly with C and inversely with b, and T_1 varies directly with both L and b. Therefore, assuming that C and L are fixed, the height and shape of the characteristic may be adjusted by changing the value of b. This is done by adjusting the value of the resistor **14**. The shape may be further changed, if desired, by adjusting the value of C or L. These elements may be made adjustable for this purpose, as indicated by the arrows. In order to keep the loss zero, the value of the transconductance g is maintained equal to b as b is varied. This is accomplished by adjusting the value of the resistor **15**, which is preferably ganged to the resistor **14**, as indicated.

It is to be understood that the above-described arrangement is illustrative of the application of the principles of the invention. Numerous other arrangements may be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. An adjustable all-pass delay network comprising an electron tube having a cathode, a plate, and a grid, a reactive feedback impedance connected between the plate and the grid, an adjustable output resistor connected between the plate and the cathode, an adjustable resistor connected to the cathode to control the transconductance of the tube, the conductance of the output resistor and the transconductance being substantially equal, and unitary means for adjusting the resistors while maintaining the equality of the conductance and the transconductance.

2. An adjustable all-pass delay network including three electron-tube stages connected in tandem, the central stage comprising an electron tube having a cathode, a plate, and a control grid, a reactive feedback impedance connected between the plate and the grid, an adjustable output resistor connected between the plate and the cathode, a second adjustable resistor connected to the cathode to control the transconductance of the tube, the conductance of the output resistor and the transconductance being substantially equal, and unitary means for adjusting the resistors while maintaining this equality.

3. An adjustable delay network comprising an electron tube having a cathode, a plate, and a grid, a circuit having a reactive impedance connected between said plate and said grid, a first adjustable resistor connected between said plate and said cathode, a second adjustable resistor connected to said cathode for controlling the grid bias voltage of said tube, and a unitary control for the two resistors to maintain the conductance of said first resistor at all times substantially equal to the transconductance of said tube.

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