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2,883,562

CIRCUIT FOR PRODUCING TIMING CONTROL SIGNALS

Filed April 27, 1954

2 Sheets-Sheet 1

FIG. 1

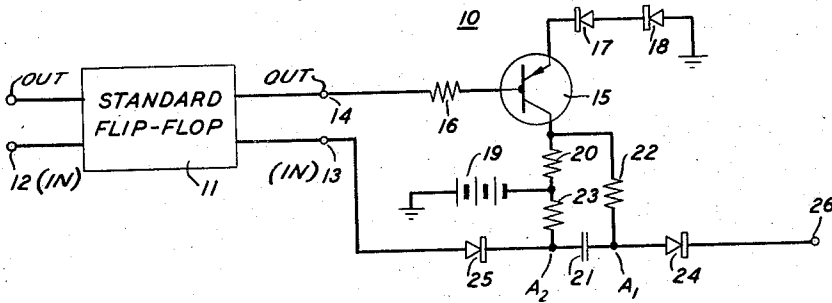


FIG. 2A

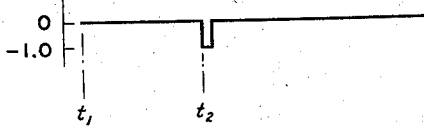


FIG. 2B

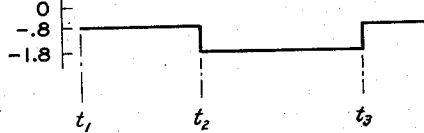


FIG. 2C

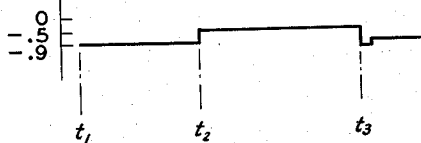


FIG. 2D

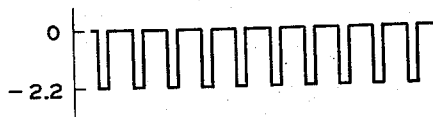


FIG. 2F

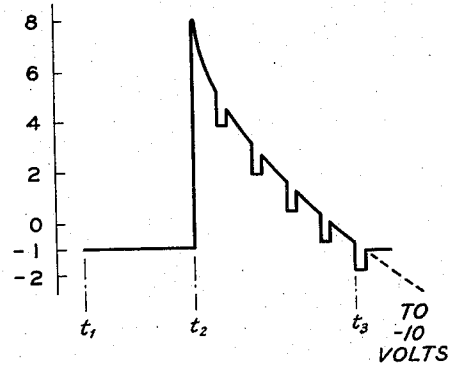
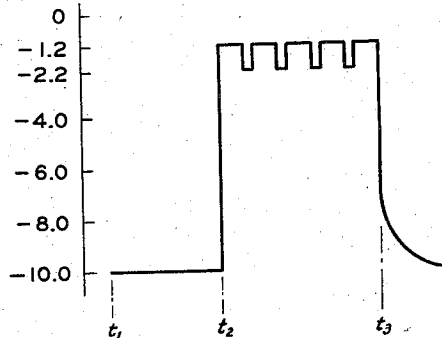


FIG. 2E



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FIG. 3

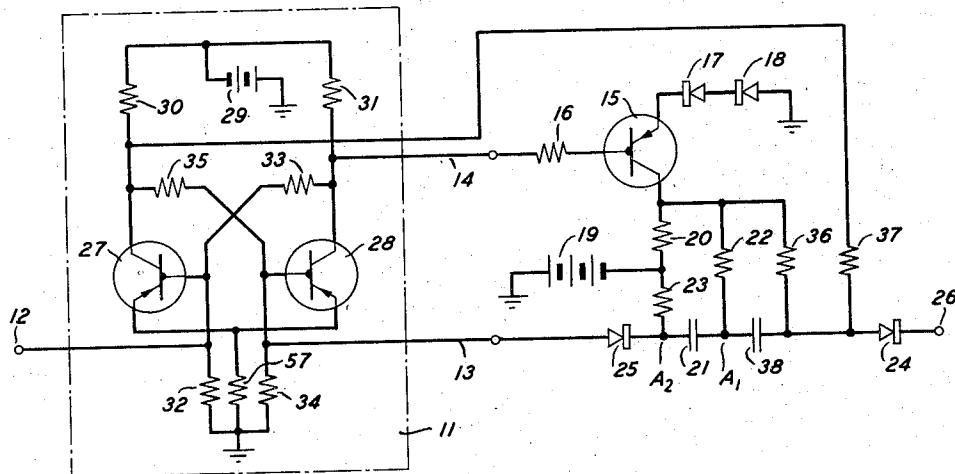
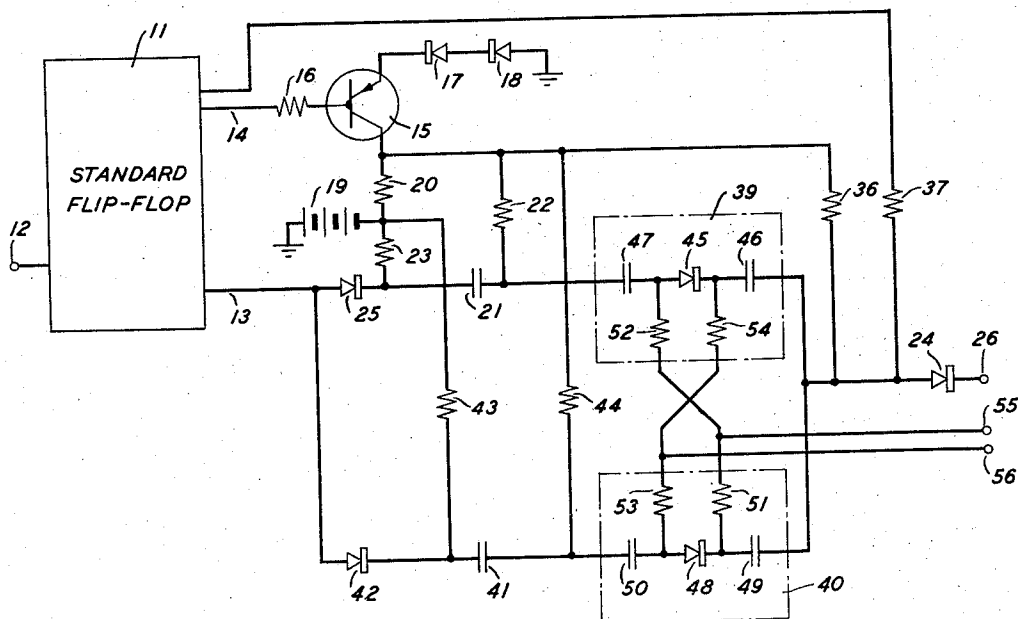


FIG. 4



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CIRCUIT FOR PRODUCING TIMING CONTROL SIGNALS

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Application April 27, 1954, Serial No. 425,964

9 Claims. (Cl. 307—88.5)

This invention relates to clock circuits and particularly to a clock circuit including a gate circuit for controlling the timing interval thereof.

The action of a clock circuit is like that of a monostable multivibrator circuit in that each has a stable period during which the circuit is considered to be "off" and no timing function is performed, and an unstable period during which the circuit is considered to be "on" and performing a timing function. The output signal of the clock circuit is of one potential during the "off" period and of a different potential during the "on" period. The "on" period is activated by an external triggering pulse applied to the circuit and the period persists for a predetermined interval after which the circuit reverts to the "off" state. In many instances, it is possible to use such a monostable circuit as a clock circuit, particularly where a relatively short "on" period is acceptable and where the duration of the "on" period is not required to be accurately determined. However, where it is necessary to provide a clock circuit having a timing interval of relatively long duration and of an accurately determined period some means other than a conventional monostable multivibrator circuit must be provided.

It is an object of this invention to improve the accuracy of the timing intervals produced by a clock circuit.

A specific object of the invention is to provide an improved clock circuit in which the timing function is performed independently of the circuitry utilized for producing the output signals.

The invention is directed to a clock circuit comprising a flip-flop circuit and a timing-gate circuit. A flip-flop is one type of driven multivibrator which is defined in the IRE Standard on Electronic Computers: Definition of Terms, 1950, as an electronic circuit having two stable states and ordinarily two input terminals (or types of input signals) each of which corresponds with one of the two states. The circuit remains in either state until caused to change to the other by application of the corresponding signal. In accordance with the invention one input signal is applied directly to the flip-flop, triggering the circuit into its "on" state.

The other input signal is chosen from a continuous chain of low-duty cycle pulses which is applied to the flip-flop through an RC timing-gate circuit. This applied pulse is that one from the chain of pulses first occurring after the instant when the capacitor in the RC timing-gate circuit is discharged sufficiently to permit substantial transmission of the pulse therethrough. With the application of this gated external pulse, the flip-flop is triggered into its "off" state and the timing interval is ended. The discharge period of the RC timing gate is measured from the occurrence of the "on" triggering pulse and is controlled by a switching circuit associated with an output terminal of the flip-flop.

One advantage of this arrangement is that the timing function is performed in a circuit distinct from the flip-flop and is not limited by any circuit conditions in the flip-flop. The timing function may, therefore, be of a

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duration as long as minutes and as short as microseconds without requiring any adjustment of the flip-flop.

Another advantage of the arrangement is that the timing intervals are reliably determined by the application of external pulses of high peak power. This ensures more positive crossings of threshold potentials than is possible by sole means of a slow charging transient voltage which is the means normally used in flip-flops.

A further advantage of this arrangement is that the clock circuit may have a plurality of distinct timing intervals of long and short duration without requiring any adjustment of the flip-flop circuit itself.

The invention, its objects and advantages will be better understood by referring to the following disclosure and the drawings forming a part thereof wherein:

Fig. 1 is a circuit diagram, partially in schematic and partially in block form, showing a clock circuit in accordance with the invention;

Figs. 2A through 2F are wave forms to aid in understanding the operation of the clock circuit of Fig. 1;

Fig. 3 shows in schematic circuit form an alternate embodiment of a clock circuit in accordance with the invention; and

Fig. 4 is a circuit diagram, partially in block and partially in schematic form, of another embodiment of a clock circuit in accordance with the invention.

With specific reference to Fig. 1, there is shown therein a clock circuit 10 in accordance with the invention which illustrates by way of example the principles of the invention. The clock circuit 10 shown therein includes a standard flip-flop 11 which is activated into its "on" state by a triggering pulse applied at terminal 12. An output wave from the flip-flop 11 appears in terminal 14 and is applied to the base electrode of a junction transistor 15 through a resistor 16. The emitter electrode of the transistor 15 is biased below ground potential by two series connected diodes 17 and 18, and the collector electrode is biased to a negative potential, e.g., 10 volts below ground, by a constant potential source 19 connected through a resistor 20. This transistor is made alternately conducting and nonconducting in accordance with the changes in the output wave from the flip-flop and the transistor operating in this manner acts as a switch for charging and discharging a capacitor 21. One plate of the capacitor is connected in current path relationship with the collector electrode of transistor 15 through resistor 22 and the other plate of which is connected in current path relationship with the negative terminal of source 19 through resistor 23. The plates of capacitor 21 are in addition connected respectively to diode 24 and diode 25 which together with the capacitor 21 forms a series current path between a terminal 26 and an input terminal 13 to the flip-flop. The diodes 24 and 25 in cooperation with capacitor 21 form a gate path between terminal 26 and terminal 13 which is normally open, that is nonconducting, except under the condition in which capacitor 21 is substantially discharged; in which condition a signal applied at terminal 26 is transmitted through the gate path to lead 13.

The operation of the circuit of Fig. 1 will be explained by reference to Figs. 2A through 2F. During the clock "off" period, t_1 to t_2 , the output signal appearing in terminal 14 as shown in Fig. 2B holds the transistor 15 nonconducting. Under this condition the collector electrode is held at -10 volts by the constant potential source 19. During the same period the potential on terminal 13 is as shown in Fig. 2C. Timing pulses as shown in Fig. 2D applied to terminal 26 are not transmitted through diode 24 during the clock "off" period because the diode is held in a high impedance condition by the voltage established at junction A_1 by resistor 22. The voltage at A_1 shown

in Fig. 2E and during the "off" period is substantially -10 volts. During the same period diode 25 is conducting by virtue of the bias established across it by the potentials on terminal 13 and battery 19; and junction A_2 is at approximately -1 volt as shown in Fig. 2F. Thus, as shown by a comparison of voltages at junctions A_1 and A_2 , the capacitor 21 is charged by about nine volts during the clock "off" period from time t_1 to t_2 . At time t_2 a triggering pulse, as shown in Fig. 2A, is applied at terminal 12 switching the flip-flop into its other stable state thereby lowering the potential applied to the transistor 15 and raising slightly the potential applied to diode 25 as shown in Figs. 2B and 2C respectively. With these changes in potential, transistor 15 is suddenly made conducting and the collector electrode is established at -1.2 volts, a sudden rise in potential of approximately nine volts from the nonconducting state. This nine-volt rise is communicated directly to both plates of capacitor 21, raising the potential of junction A_1 to -1.2 volts and A_2 to +8.0 volts as shown in Figs. 2E and 2F, thereby applying a restraining bias to and blocking the diode 25. Simultaneously, diode 24 is unblocked and the input pulses Fig. 2D applied at terminal 25 are transmitted through junction A_1 as shown in Fig. 2E, to junction A_2 as shown in Fig. 2F. These pulses are blocked at this point by diode 25.

All of this action takes place very quickly after the application of the triggering pulse to terminal 12 and starts the clock "running." The junction A_1 is held at -1.2 volts by the low resistance 22 and the potential at junction A_2 drops slowly from +8 volts towards -10 volts as the capacitor 21 charges through resistor 23 towards the potential of source 19 as shown in Fig. 2F. When at a time t_3 the potential at junction A_2 reaches the threshold voltage of diode 25, near -1 volt, the diode 25 is unblocked and timing pulses are transmitted through diode 25 to the input terminal 13 as shown in Fig. 2C thereby triggering the flip-flop back to its original "off" state, "stopping the clock," returning the transistor 15 to its cutoff condition. The collector electrode of transistor 15 drops quickly to -7 volts carrying with it the potential of junction A_1 , and then more slowly to -10 volts as shown in Fig. 2E as capacitor 21 charges through resistors 20 and 22 to the potential of source 19. When junction A_1 falls to -7 volts, diode 24 is again blocked and transmission of input pulses through the diode ceases. During the same period, diode 25 is held unblocked and junction A_2 is maintained at about -1 volt by conduction through the diode. When junction A_1 reaches -10 volts the clock circuit is again ready for use.

From the above description it can be seen that the timing interval of the circuit is primarily dependent upon values assigned to resistor 23 and capacitor 21, and by changing these values the duration of the timing interval may be made very short in the range of microseconds or very long in the range of minutes without adjusting any of the other circuitry associated with the clock circuit.

In addition, stability of the timing circuit is assured by the fact that the timing interval is entirely dependent upon an RC constant and is substantially independent of any actual voltages. That is, the RC timing transient represents a charging excursion of nine volts (from +8 to -1 volt as shown in Fig. 2R) that takes place in the capacitor 21 out of an eventual (if uninterrupted) excursion of eighteen volts. The gating of the input signal occurs at the midpoint of the voltage excursion which means that the timing interval is approximately 0.63 RC where R is the value of resistor 23 and C is the value of capacitor 21. As this expression for the timing interval is independent of actual voltage values, it is evident that close control of the voltages associated with the circuit is not essential.

Fig. 3 shows another embodiment of the invention as used in actual practice wherein the circuit of the flip-flop 11 is shown in detailed schematic form. The flip-

flop 11 comprises two junction type transistors 27 and 28, the collector electrodes of each being connected to the negative terminal of a source of constant potential 29 through resistors 30 and 31 respectively. The base electrode of transistor 27 is connected to ground potential through resistor 32 and to the collector electrode of transistor 28 through resistor 33. Similarly, the base electrode of transistor 28 is connected to ground potential through resistor 34 and to the collector electrode of transistor 27 through resistor 35. The emitter electrodes of the two transistors are connected to ground potential through resistor 57. The flip-flop has two stable states and in each stable state one of the two transistors must be fully "on" and the other transistor must be fully "cut-off." To change states negative triggering pulses are applied to the base electrode of the off transistor. Input terminal 12 is connected to the base electrode of transistor 27 to apply a negative pulse thereto to switch transistor 27 on, cut-off transistor 28, and start the clock running. Input terminal 13 is connected to the base electrode of transistor 28 to apply a negative pulse to switch the transistor 28 on, cut-off transistor 27, and stop the clock. In this manner the circuit of Fig. 3 which includes all of the circuit elements of Fig. 1 is made to operate in a manner similar to that of Fig. 1.

As an additional feature, the circuit of Fig. 3 includes a resistor 36 connected between the collector electrode of transistor 15 and the anode of diode 24 and a resistor 37 connected between the collector of transistor 27 and the same terminal of diode 24 thereby forming a voltage divider. In addition, a direct current blocking capacitor 38 is connected between junction A_1 and the voltage divider connection to diode 24 to comprise a buffer gate circuit that is operated independently of the voltages at junction A_1 . This buffer gate circuit assures suitable blocking and unblocking operation of diode 24 in conformance with the above-described plan which is substantially independent of the voltage excursion of the capacitor 21 and junction A_1 .

A further embodiment of the invention which permits a selection of timing intervals in accordance with control voltage applied to the circuit is shown in Fig. 4. Fig. 4 includes the flip-flop 11 of Fig. 3 (here shown in block form), the amplifier including transistor 15 and the buffer gate including diode 24. However, in this embodiment the trigger pulses through diode 24 may reach input lead 13 through two alternative paths. The one path includes a selector gate 39, capacitor 21 and diode 25 with resistors 22 and 23 connected between the plates of capacitor 21 and the collector electrode of transistor 15 and the source 19 respectively. The second path includes a selector gate 40, a capacitor 41 and a diode 42 with resistors 43 and 44 connected between the plates of capacitor 41 and the collector electrode of transistor 15 and source 19 respectively. The selector gate 39 comprises a diode 45 and direct current blocking capacitors 46 and 47 connected to the respective electrodes thereof. The selector gate 40 includes a diode 48 and direct current blocking capacitors 49 and 50 connected to the respective electrodes thereof. A pair of series-connected resistors 51 and 52 join opposite electrodes of the diodes 45 and 48, and a pair of series-connected resistors 53 and 54 connect the other two electrodes of diodes 45 and 48. Control signals are applied to the selector gates through terminals 55 and 56 which are connected respectively to the junction of resistors 51 and 52 and to the junction of resistors 53 and 54. Control signals which establish the voltage on terminals 55 and 56 at one polarity operate to enable selector gate 39 and block selector gate 40 so that the clock circuit timing function is performed by capacitor 21 and resistor 23. When applied control signals give terminals 55 and 56 an opposite polarity the selector gate 39 is blocked and selector gate 40 enabled permitting capacitor 41 and resistor 43 to perform the timing

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function of the clock circuit. It is obvious that by selecting different RC constants for each pulse path, the clock circuit may be given different timing intervals.

While many value for circuit elements may be used, in the embodiment of the invention shown in Fig. 3, the values used are:

15	-----	M1778.
16	-----	51,000 ohms.
17	-----	IN138 (Western Elec.).
18	-----	IN138 (Western Elec.).
19	-----	10 volts.
20	-----	51,000 ohms.
21	-----	8 microfarads.
22	-----	0.1 megohm.
23	-----	10 megohms.
24	-----	IN138 (Western Elec.).
25	-----	IN138 (Western Elec.).
27	-----	M1778.
28	-----	M1778.
29	-----	3 volts.
30	-----	6200 ohms.
31	-----	6200 ohms.
32	-----	11,000 ohms.
33	-----	6200 ohms.
34	-----	11,000 ohms.
35	-----	6200 ohms.
36	-----	2 megohms.
37	-----	0.1 megohm.
38	-----	0.1 microfarad.
57	-----	2000 ohms.

It is understood that the foregoing embodiments are merely illustrative of the application of the principles of the invention. Numerous other arrangements might be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. A gate circuit adapted to control the period of one output state of a multivibrator having an input terminal and an output terminal, said gate circuit comprising an input terminal to which are applied triggering pulses, first and second unidirectional conducting devices and a capacitor, said first device being connected between one plate of said capacitor and said input terminal of said gate circuit, said second device being connected between the other plate of said capacitor and the input terminal of said multivibrator, a source of potential connected to charge said capacitor and to bias said first device in a non-conducting state during the period of a second output state of said multivibrator, switch means having a conduction terminal connected to said capacitor and a control terminal connected to said multivibrator output terminal thereby to respond to said one output state of said multivibrator for biasing said first device in a conducting state and said second device in a non-conducting state and responsive to said one output state of said multivibrator for providing a discharge path for said capacitor whereby said second device is made conducting after a predetermined time interval and the triggering pulses are applied through said gate circuit to the input terminal of said multivibrator.

2. A clock circuit comprising a flip-flop circuit having an input terminal and an output terminal, a current path for applying timing pulses to said input terminal including first and second diodes and a capacitor connected therebetween in series relationship, a source of constant potential connected to charge said capacitor to a potential of one polarity and for biasing said first diode in a non-conducting state during one output state of said flip-flop circuit, amplifier means having a current electrode connected to said capacitor and a control electrode connected to said output terminal of said flip-flop circuit thereby to respond to the other output state of said flip-flop circuit to charge said capacitor to a potential of the other polarity whereby said first diode is made

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conducting and said second diode is made nonconducting, and responsive to said other output state of said flip-flop circuit for providing a discharge path for said capacitor whereby said second diode is made conducting after a predetermined time interval and timing pulses can be applied through said diodes and capacitor to the input terminal of said flip-flop circuit.

3. A clock circuit according to claim 2 wherein said source of steady potential is of negative polarity and said amplifier means includes a current device having a control electrode, a first current electrode and a second current electrode, a bias circuit connected between the first current electrode and a fixed potential point, means connecting said second current electrode to the source of constant potential and to the capacitor, and means for connecting the control electrode to the output terminal of said flip-flop circuit whereby said current device is conducting during said other output state and said second electrode is substantially at the potential of said first electrode, and said current device is nonconducting during said one output state and said second electrode is at the potential of the source of constant potential.

4. In combination with a source of a sequence of pulses and a pulse utilization circuit, a gating network interposed between said source and said utilization circuit for preferentially passing selected members of said pulse sequence to said utilization circuit, said network comprising a first unidirectional conducting device, a timing capacitor having two terminals, and a second unidirectional conducting device, said first device, capacitor and second device being connected together in tandem in the order named between said source and said utilization circuit, a source of steady potential having a first and a second terminal, said first terminal being connected to a fixed potential point, a timing resistor interconnecting the second terminal of said steady potential source with one capacitor terminal, two current limiting resistors connected in series between said second terminal of said potential source and another capacitor terminal, a switch having two conduction terminals and a control element, one of said conduction terminals being connected to a common point of said two limiting resistors, the other of said conduction terminals being connected to said fixed potential point, said timing resistor and capacitor being proportioned to provide a preassigned decay time, said unidirectional conducting devices being poled in the same direction relative to the path of pulse current from said pulse source to said utilization circuit whereby under one charge condition of said capacitor said devices operate to block transmission of pulses from said pulse source to said utilization device and under another charge condition said devices permit passage of pulses from said pulse source to said utilization device, and means including said utilization circuit to supply a varying voltage to said control element for altering the conduction condition of said switch.

5. The combination according to claim 4 in which said utilization circuit comprises a flip-flop circuit having an input terminal and an output terminal, and said switch comprises amplifying means including said two conduction terminals and said control element, said one amplifying conduction terminal being connected to said common point of said two limiting resistors, said other amplifying conduction terminal being connected to said fixed potential point, and said control element being connected to said output terminal of said flip-flop circuit, said gating said input terminal of said flip-flop circuit, said control network being connected between said pulse source and element being responsive to two different states in said flip-flop circuit for altering the conduction condition of said two amplifying terminals, said control element being responsive to one of said two flip-flop circuit states for establishing said one charge condition of said capacitor whereby said devices block transmission of pulses from said pulse source to said input terminal of said flip-flop

circuit for the entire duration of said one state of said flip-flop circuit and for a time determined by the effective values of said timing resistor and capacitor.

6. The combination according to claim 5 which includes a biasing circuit comprising at least one diode and connected between said other amplifying conduction terminal and said fixed potential point, said one diode having its anode connected to said fixed potential point.

7. A clock circuit comprising a flip-flop circuit including first and second input terminals and first and second output terminals, means for supplying first triggering pulses to said first input terminal to institute a first stable state in said flip-flop circuit, means for supplying second triggering pulses to said second input terminal to change said flip-flop circuit into a second stable state, said last-mentioned means including serially a first diode, a first capacitor and a second diode, a source of constant potential including a ground terminal and a negative terminal, first and second resistors connected in series between said negative source terminal and one terminal of said first capacitor, and a third resistor connecting said negative source terminal to a point common to said second diode and a second terminal of said first capacitor, a semiconductor device having base, emitter and collector electrodes, said base electrode being connected to said first flip-flop output terminal, said emitter electrode being connected to ground and said collector electrode being connected to a common point of said first and second resistors, a second capacitor connected between said one terminal of said first capacitor and said first diode in said series circuit and fourth and fifth resistors having terminals connected to a terminal common to said second capacitor and said first diode, said fourth resistor having its opposite terminal connected to said collector electrode, said fifth resistor having its opposite terminal connected to said second output terminal of said flip-flop circuit, said semiconductor device being responsive to said second stable state in said flip-flop circuit to enable said first capacitor to charge from said potential source to a voltage of one polarity and to bias said first diode in a nonconducting state thereby blocking pulse transmission in said second triggering pulse supplying means to said second input terminal of said flip-flop circuit, said semiconductor device being responsive to said first stable state to remove the bias from said first diode and to enable said first capacitor to charge to a voltage of different polarity to make said second diode conducting after a predetermined time interval thereby enabling pulse transmission in said second triggering pulse means to said second input terminal of said flip-flop circuit.

8. A clock circuit comprising a flip-flop circuit including first and second input terminals and first and second output terminals, means for supplying first triggering pulses to said first flip-flop input terminal to institute a first stable state in said flip-flop circuit, means including a first diode for supplying second triggering pulses to said second flip-flop input terminal to change said flip-flop circuit into a second stable state, first and second series current paths connected in parallel between said second flip-flop input terminal and said first diode, said first path including a second diode, a first capacitor, and a first pulse selector gate, said second path including a third diode, a second capacitor and a second pulse selector gate, a source of constant potential including a ground terminal and a negative terminal, first and second resistors connected in series between said negative terminal and a terminal common to said first capacitor and first gate, a third resistor connecting said negative terminal and a terminal common to said first capacitor and second diode, said first resistor and a fourth resistor connected in series between said negative terminal and a

terminal common to said second capacitor and second gate, a fifth resistor connecting said negative terminal to a point common to said third diode and second capacitor, means connected to said first and second gates and reversible in polarity to make alternately one of said last-mentioned gates conducting and the other nonconducting, sixth and seventh resistors, each having one terminal connected to a point common to said first diode and said first and second gates, said sixth resistor having its opposite terminal connected to said first flip-flop output terminal, and amplifier means having a control electrode connected to said second flip-flop output terminal and a first current electrode connected to the opposite terminal of said seventh resistor and a point common to said first, second and fourth resistors, said amplifier means being responsive to said second stable state in said flip-flop circuit to charge said first and second capacitors to a potential of one polarity and to bias said first diode in a nonconducting state thereby blocking transmission of the second triggering pulses to said first and second paths, said amplifier means being responsive to said first stable state in said flip-flop circuit to remove the bias from said first diode and to enable said first and second capacitors to charge to a potential of a different polarity for making said second and third diodes conducting so that when said reversible polarity means renders one of said first and second gates conducting and the other of said last-mentioned gates nonconducting transmission of the second triggering pulses is enabled through the series path including said last-mentioned one gate to said second flip-flop input terminal.

9. The clock circuit according to claim 8 in which each of said first and second gates includes in series two capacitors and a diode interposed therebetween, and a pair of resistors each having one terminal common to one of said last-mentioned capacitors and one electrode of said last-mentioned diode, said reversible polarity means comprising two terminals each connected to a point common to the opposite terminals of two of said resistors connected to different electrodes of the respective diodes included in said gates, and said amplifier means comprising a semiconductor device including base, emitter and collector electrodes, said base electrode being connected to said second flip-flop output terminal, said emitter electrode being connected to ground, and said collector electrode being connected to the opposite terminal of said seventh resistor and said point common to said first, second and fourth resistors, said semiconductor device being responsive to said second stable state in said flip-flop circuit to enable said first and second capacitors to charge from said potential source to a voltage of one polarity and to bias said first diode in a nonconducting state thereby blocking transmission of the second triggering pulses to said first and second paths, said semiconductor device being responsive to said first stable state in said flip-flop circuit to remove bias from said first diode and to enable said first and second capacitors to charge to a potential of a different polarity for making said second and third diodes conducting so that when said reversible polarity means renders one of said first and second gates conducting and the other of said last-mentioned gates nonconducting transmission of the second triggering pulses is enabled through the series path including said last-mentioned one gate to said second flip-flop input terminal.

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