

Sept. 3, 1957

W. J. ALBERSHEIM

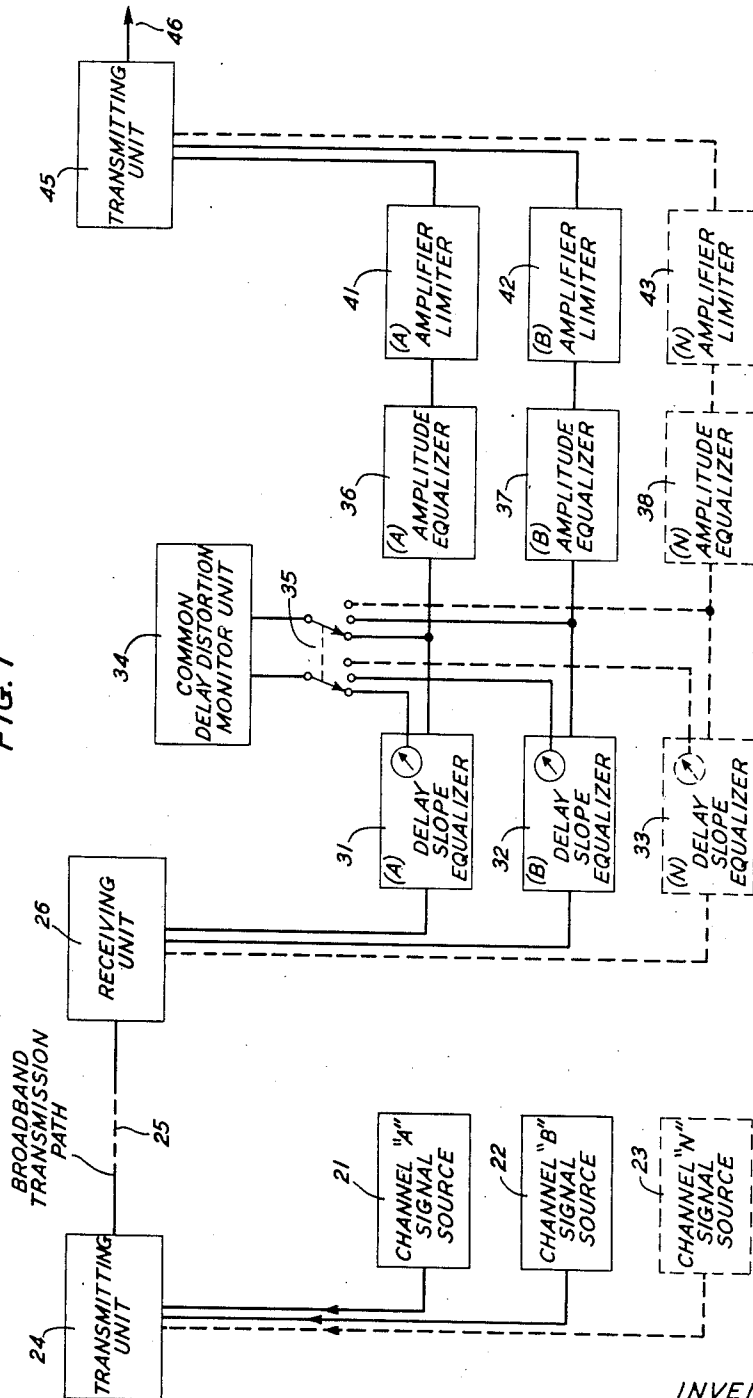
2,805,398

AUTOMATIC DISTORTION CORRECTION

Filed Dec. 31, 1953

8 Sheets-Sheet 1

FIG. 1



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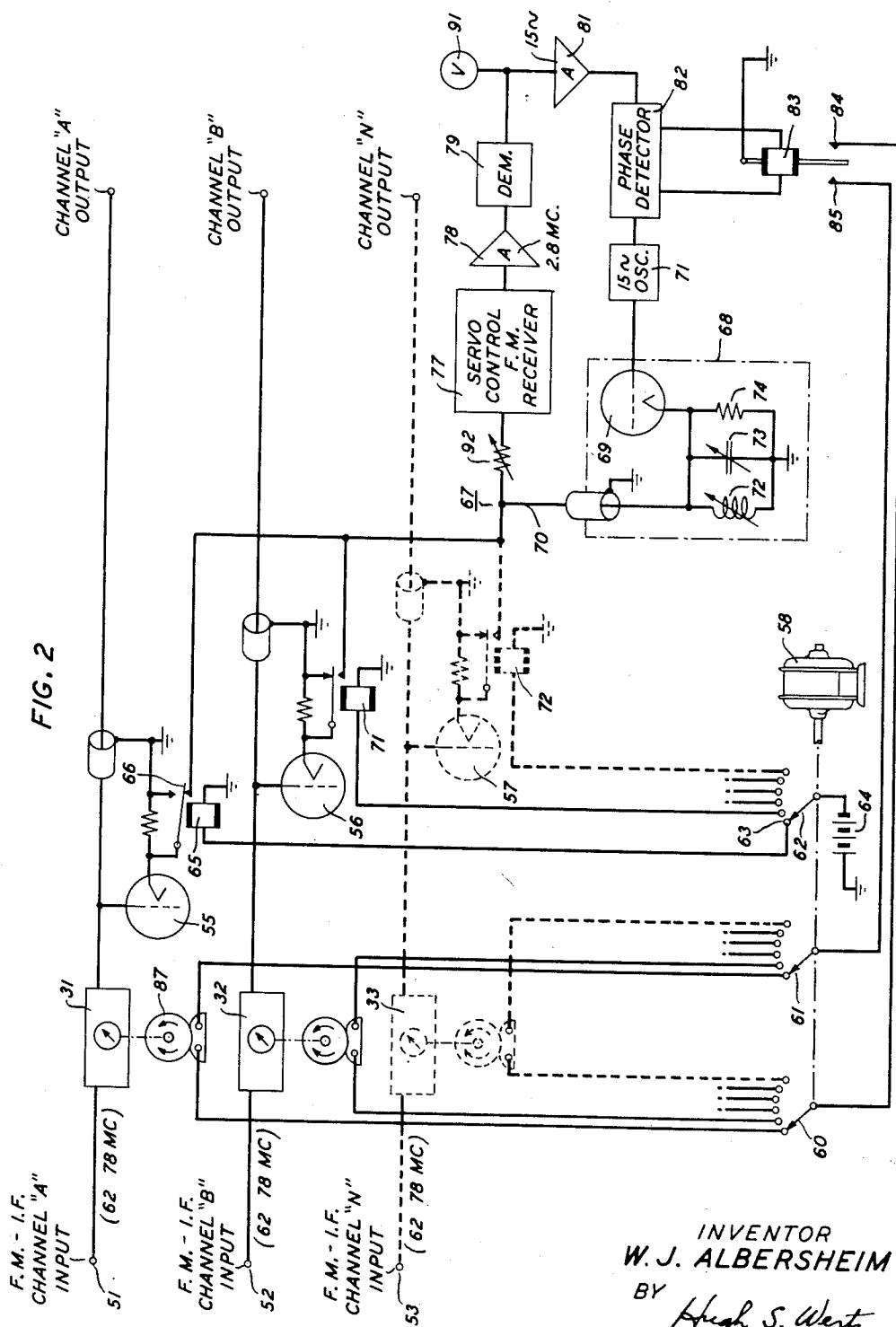
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8 Sheets-Sheet 2



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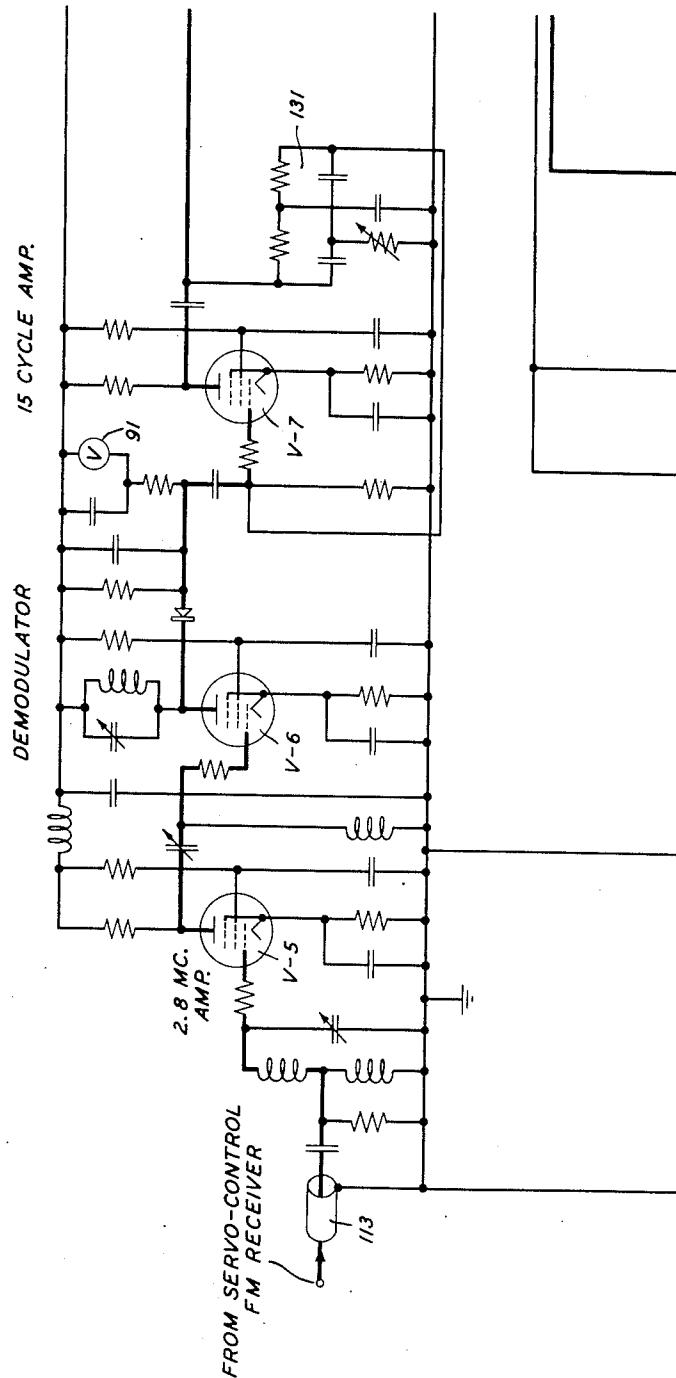
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8 Sheets-Sheet 3

FIG. 3

FIG. 4	FIG. 5
FIG. 6	FIG. 7

FIG. 4



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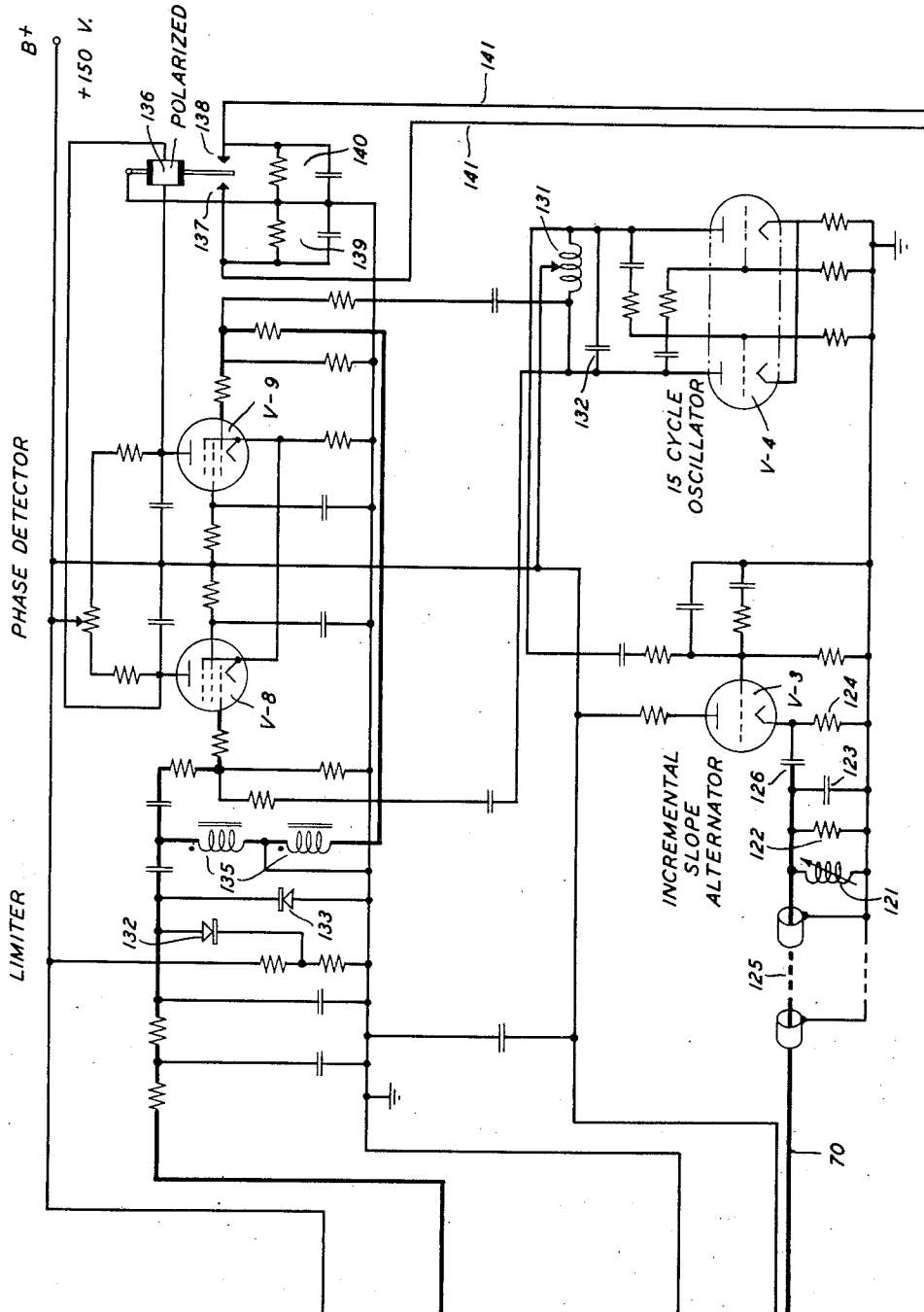
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AUTOMATIC DISTORTION CORRECTION

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8 Sheets-Sheet 4

FIG. 5



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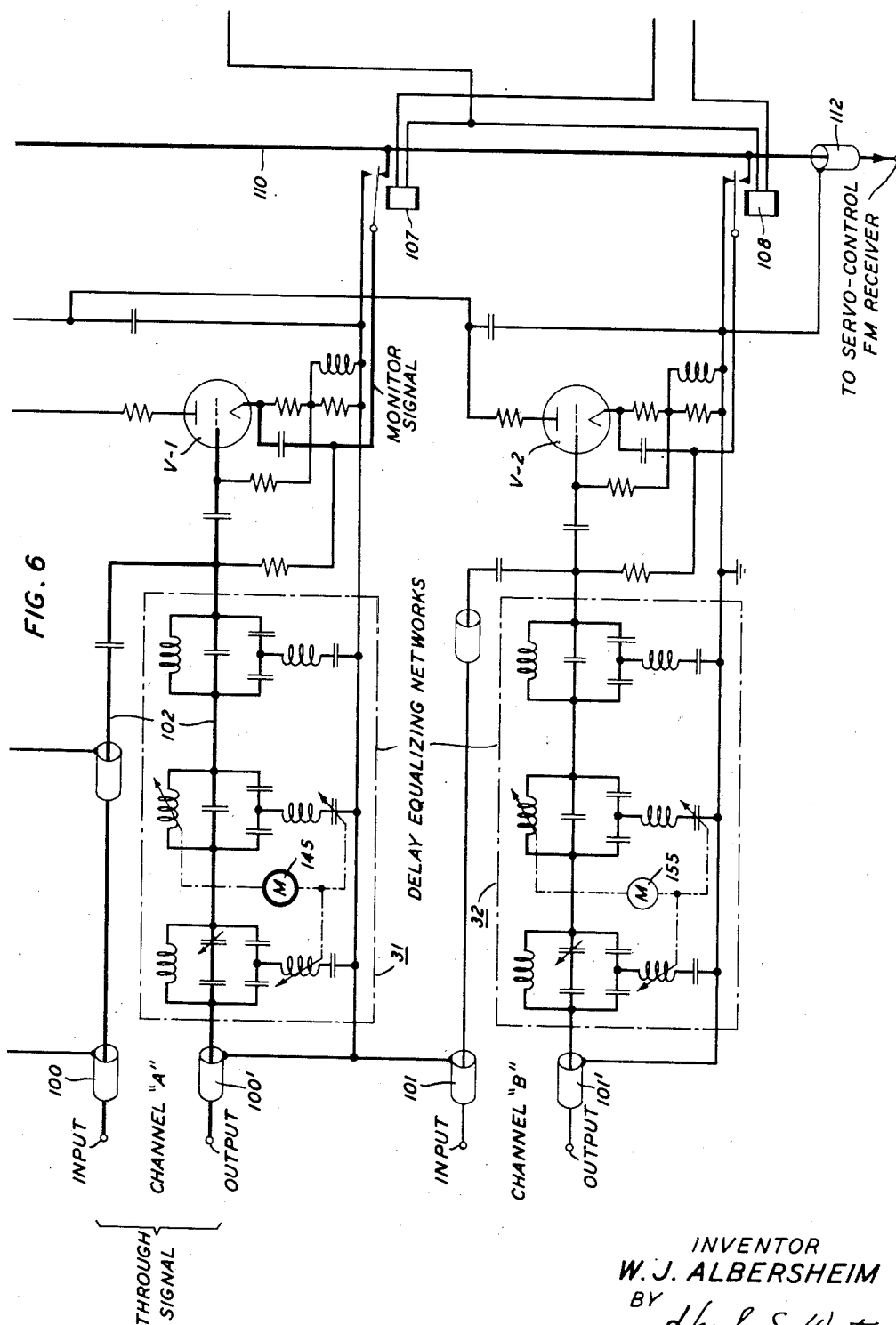
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AUTOMATIC DISTORTION CORRECTION

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8 Sheets-Sheet 5



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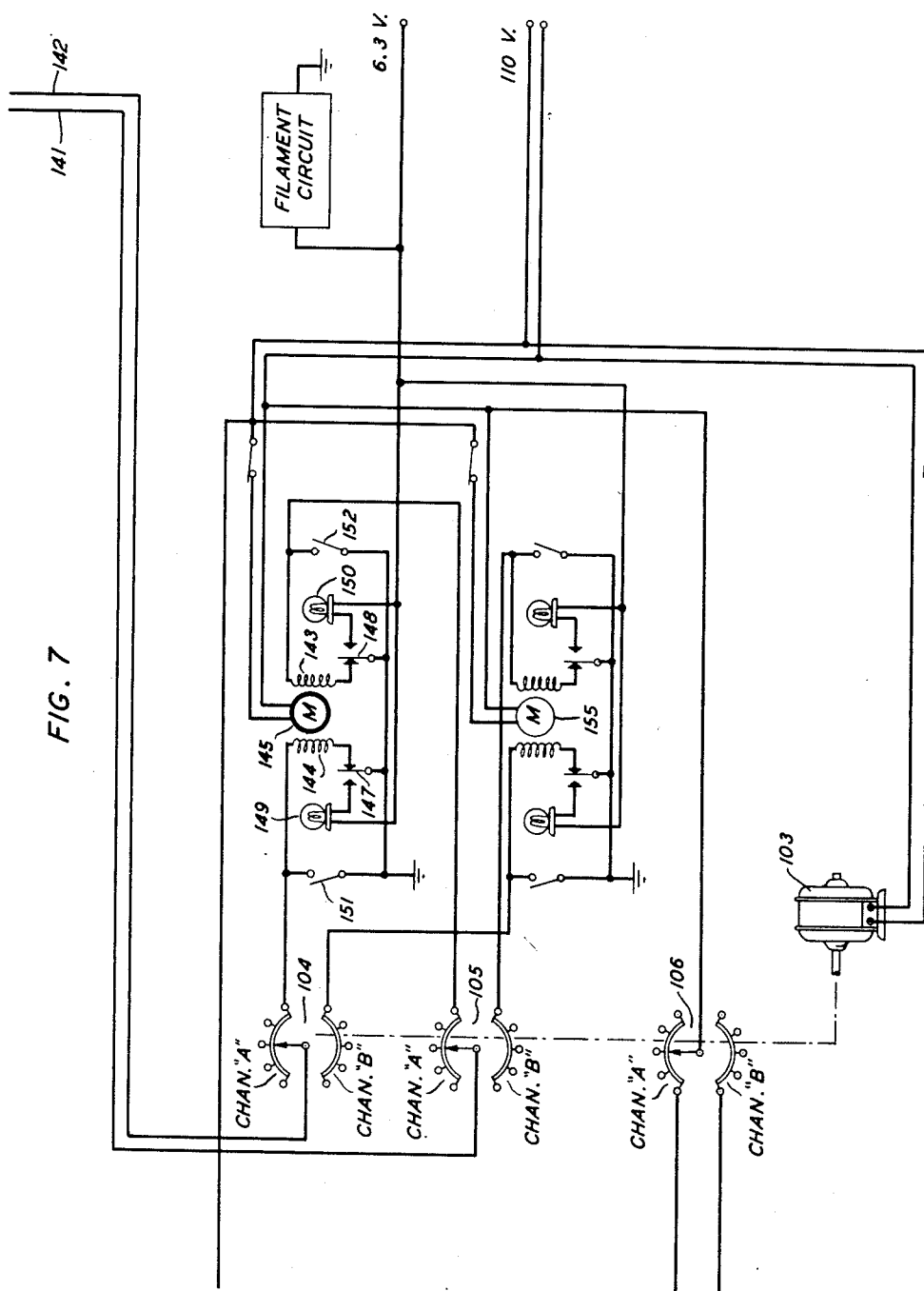
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8 Sheets-Sheet 6



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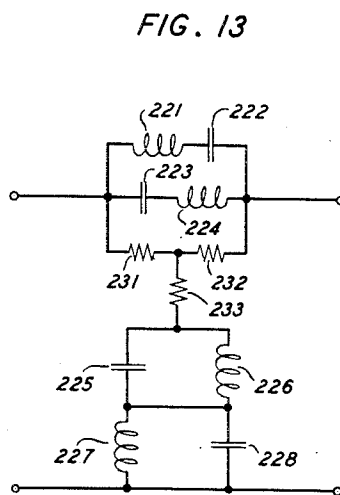
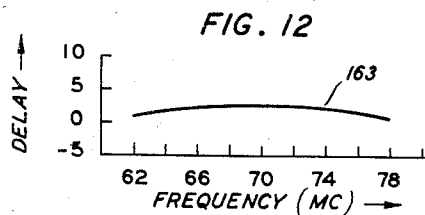
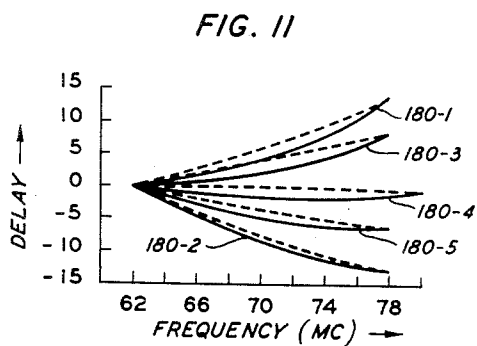
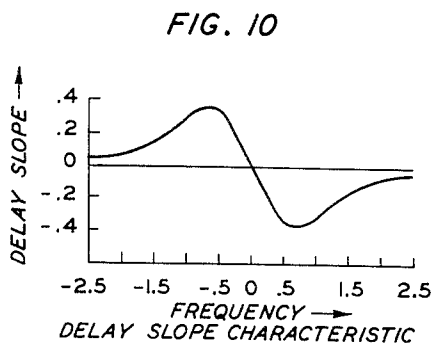
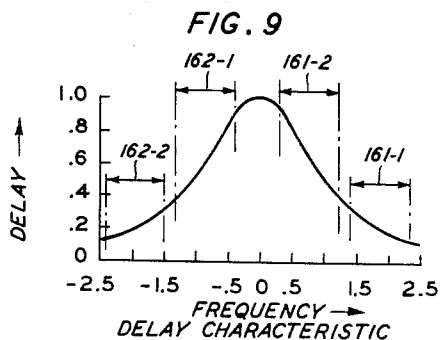
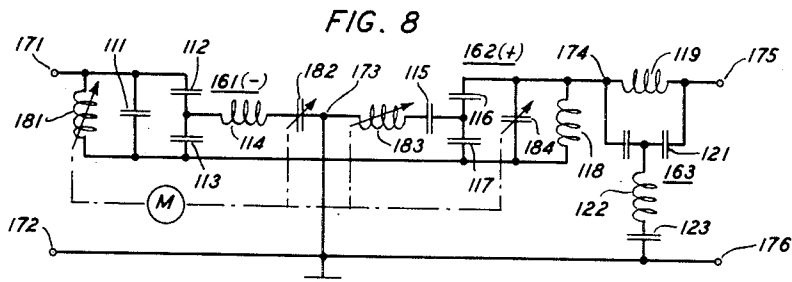
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AUTOMATIC DISTORTION CORRECTION

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FIG. 14

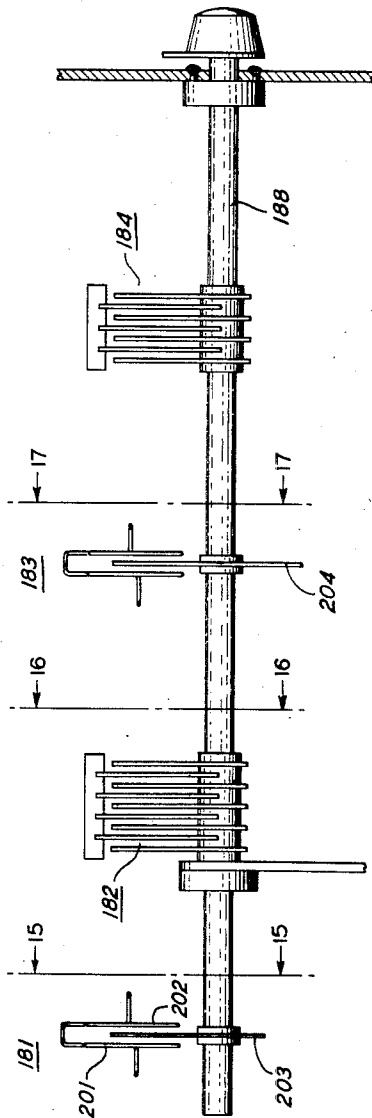


FIG. 17

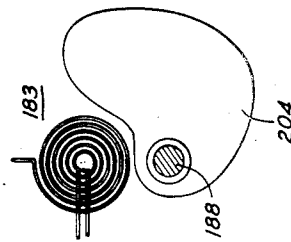


FIG. 16

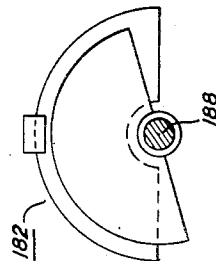
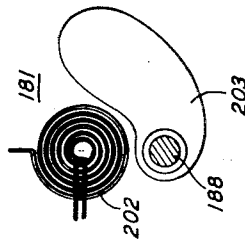


FIG. 15



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AUTOMATIC DISTORTION CORRECTION

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Application December 31, 1953, Serial No. 401,660

3 Claims. (Cl. 333—2)

This invention relates to electrical transmission systems in which a broad band of frequencies is transmitted over substantial distances and to components thereof, and, more particularly, to distortion correction in such systems.

Transmission channels of great length are in every day use for long distance telephone calls and intercity television circuits. The broad band high frequency facilities which are now employed for many of these long distance circuits tend to be moderately sensitive and are subject to various types of distortion. This distortion may be quite severe and often varies substantially with the daily changes of temperature, for example.

The principal object of the present invention is to automatically and positively correct distortion in extended transmission systems.

In a specific aspect, the invention relates to the correction of delay distortion. It is well known that in many transmission systems electromagnetic waves of different frequencies are not propagated at the same velocity. Furthermore, in a long, broad band, high frequency transmission system, substantial distortion of the transmitted signal may result from the cumulative effect of this phenomenon. Particular difficulty has been observed in microwave relay systems with this variable phase delay distortion of frequency modulated signals. Because of the isolated location of many of the unattended amplification stations it has previously been proposed to compensate for the frequent changes in delay distortion by introducing delay equalization networks manually at the microwave transmission line terminals. It has been found, however, that the frequency modulation amplifier-limiters at the repeater points will "freeze in" delay distortion if it is allowed to accumulate to a large value before equalization. While this adverse effect could be overcome by automatic delay equalization, prior art automatic equalization systems have many undesirable features such as the use of pilot tones, the use of fixed delay equalizers, and their applicability to but a single channel. Therefore, because of the large number of channels requiring equalization and the high cost of equalizers for each of these channels, in addition to their other disadvantages, automatic equalization has been considered impractical up to the present time.

Accordingly, a further object of the present invention is to simplify and reduce the cost of the automatic phase delay equalizing equipment suitable for operation with a large number of channels.

In accordance with the present invention, distortion of a particular type may be eliminated from a transmission path by using a variable correction network for this type of distortion which is automatically adjusted by a servomechanism operated by a monitor circuit. In the monitor circuit positive and negative increments of the particular type of distortion are alternately introduced at a predetermined frequency rate, and a circuit tuned to this frequency rate identifies the residual distortion and develops a signal of appropriate sign and magnitude

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which activates the correcting servomechanism. In accordance with the preferred embodiment of the invention, phase delay distortion in a plurality of channels is corrected by individual equalizers for the separate channels, which are controlled by a common branch circuit.

Other objects and certain additional features and advantages will be developed in the course of the detailed description of the drawings. In the drawings:

Fig. 1 is a block diagram of a transmission circuit which embodies the principles of the present invention;

Fig. 2 is a functional showing of the common monitor branch circuit and the associated switching circuitry for delay equalization of several channels;

Fig. 3 indicates how Sheets 3 through 6 of the drawings should be assembled to form a complete circuit diagram;

Figs. 4 through 7, which are Sheets 3 through 6 of the drawings, constitute a detailed circuit diagram of the equalizing arrangement shown functionally in Fig. 2;

Fig. 8 is a constant impedance variable delay slope equalizer;

Figs. 9 through 12 are characteristic plots of phase delay and phase delay slope versus frequency for equalization networks of the type employed in the present invention;

Fig. 13 is a constant impedance amplitude equalizer; and

Figs. 14 through 17 show the physical mounting arrangement of the variable reactance elements of the delay slope equalizer.

Fig. 1 shows by way of example and for purposes of illustration a broad band transmission path and an associated delay distortion correction means in block diagram terms. More specifically, the equipment represented by Fig. 1 includes several signal sources indicated at 21, 22 and 23. The intermediate frequency outputs from these three channels are combined in the transmitting unit 24 to form a single, broad band, frequency modulated, signal output. The dotted linkage 25 between the transmitting unit 24 and the next succeeding receiver unit 26 is an extended transmission path. This transmission path could for example be a radio link between a terminal station of a microwave relay system and a first intermediate amplification station. Alternatively, this transmission path could be a coaxial cable or an elongated hollow conducting wave guide. In the receiver unit 26 the received signal is broken down into the several intermediate frequency channels corresponding to the original intermediate frequency signals from signal sources 21, 22 and 23. These intermediate frequency signals may, for example, have a band width of 15 to 20 megacycles at a carrier frequency of somewhat less than 100 megacycles. These individual intermediate frequency signals are then coupled to the delay slope equalizers 31, 32 and 33. After passing through the delay slope equalizers the transmission channel is coupled to a shunt monitor circuit 34 which is a common delay distortion detection unit for all of the channels of the high frequency system. This common monitor equipment is successively coupled to the various channels by switching means 35 and adjusts the delay slope equalizer of each channel in turn to its correct value to compensate for the distortion introduced by the extended transmission path 25. The exact circuitry whereby this is accomplished will be considered in much greater detail hereinafter.

The individual intermediate frequency signals are then routed to the amplitude equalizers 36, 37 and 38 and then to the amplifying and amplitude limiting units 41, 42 and 43. From the amplitude limiters the intermediate frequency channels are coupled to the transmitting unit

45 where they are recombined and transmitted in the single broad band frequency modulated signal as indicated by the arrow 46.

In Fig. 2 the delay slope equalizers 31 through 33 and the common delay distortion detection unit 34 are shown functionally in somewhat greater detail. The frequency modulated intermediate frequency channel input terminals are shown at 51, 52 and 53. The delay equalizing networks 31, 32 and 33 are still shown in boxes in this schematic drawing but will be shown in greater detail in Figs. 6 and 8 of the present drawings. Channels A, B and N have their respective cathode follower tubes 55, 56 and 57 connected in shunt with the outputs from the equalizers 31, 32 and 33.

These cathode follower units are part of the switching arrangement whereby the common delay distortion detection circuit may be successively switched from one channel to another without reaction back from the common circuit into the main signal channels. The slow speed motor 58 together with the switches 61 and 62 which are coupled thereto control the switching of the common monitor circuit from one of the intermediate frequency channels to the others. Specifically, let us consider the operation of the automatic delay equalization network when channel A is being equalized. Under these circumstances, the switch arm 62 contacts the terminal 63 and applies a potential from the voltage source 64 to the relay 65. The switch contacts 66 are then closed and channel A is coupled to the input terminal 67 of the common monitor branch circuit via the cathode follower tube 55. Note that with the other relays 71 and 72 inactive the outputs from the cathode follower tubes 56 and 57 are grounded and no signal reaches the common monitor circuit input terminal 67, except that from channel A.

In accordance with the present invention the monitor branch circuit detects distortion products which have been introduced by the extended transmission path 25 as mentioned hereinbefore in connection with Fig. 1. The monitor branch circuit determines the sign of the delay slope distortion and corrects it by varying the delay slope equalizing networks 31 through 33. Because it detects distortion products of the communication signals themselves, the common monitor branch circuit may be readily switched from one channel to the next without synchronized switching operations at distant points such as are required in certain other types of test equipment. The physical phenomenon giving rise to the distortion products which are detected by the monitor branch circuit is the fact that the delay distortion of frequency modulation signals produces combination frequencies of various of the input signal frequencies.

The frequency modulated input signals from channel A are routed to terminal 67 where they are subjected to positive and negative increments of delay distortion by the circuit 68. In this incremental delay unit 68 the vacuum tube 69 is alternatively made conducting and cut-off at a 15 cycle rate by the output from the oscillator 71. As the vacuum tube 69 is turned off and on the electrical network is made up of the inductance 72, the condenser 73, and the resistance 74 changes substantially in its delay slope output. The reason for this change lies in the change of the terminal impedance of the network as compared with the characteristic 76 ohm impedance of the properly dimensioned delay line 70 between the input at terminal 67 and the cathode of tube 69.

The intermediate frequency signal is demodulated in the servo-control frequency modulation receiver 77. In the absence of distortion the demodulated "baseband" signal contains only the frequency band extending from 0 to 2 megacycles. If distortion is present, higher combination frequencies are generated as noted above.

These are fed to a narrow band amplifier 78 which selects and highly amplifies frequencies centered near 2.8 megacycles but rejects the 0 to 2 megacycle original sig-

nal components. Now, if there is any distortion present in the intermediate frequency signal of channel A, it will be varied at a 15 cycle rate by the incremental delay unit 68, and amplitude modulated products which vary at a frequency rate of 15 cycles will appear at the output of the amplifier 78. However, if there is no delay distortion in the channel, there will be no delay slope asymmetry, hence no 15 cycle component in the delay distortion at the input terminal 67, and consequently there will be no 15 cycle amplitude modulated output components from the amplifier 78. The demodulator 79 detects any 15 cycle amplitude modulated components which may be present in the output of the amplifier 78. These are amplified in turn by the 15 cycle amplifier 81 and are then routed to the phase detector 82. The phase detector 82 compares the output from the 15 cycle amplifier 81 with the standard 15 cycle signal from the oscillator 71 and operates the polarized relay 83 in one direction or the other depending on the relative polarity of the two signals.

Output contacts 84 and 85 of the polarized relay 83 are connected to switch terminal 60 and 61 which are in turn connected to motor 37 when channel A is being adjusted. Depending on whether the delay distortion present in channel A is positive or negative, the amplitude modulated distortion products appearing at the output of the amplifier 78 are in or out of phase with the 15 cycle oscillator, and the polarized relay 83 contacts one or the other of its contacts. This operates the motor 87 in the proper direction to readjust the delay equalizer 31 to eliminate distortion in the signal channel. When the mean distortion at terminal 67 has been reduced to a negligible amount, there will be no 15 cycle modulated components appearing at the output of the amplifier 81, the polarized relay will remain in its neutral position, and the delay equalizer moves no further. After a suitable period has elapsed for this equalization operation to take place, the timing motor 58 turns the switches 60 and 62 to the next intermediate frequency channel and the whole process is repeated.

The steady component of the output of the demodulator 79 is indicated by the overload control voltmeter 91. Excessive output means that the 2.8 megacycle amplifier is overloaded and its 15 cycle amplitude modulation may be swamped by compression. Such overload may be due to excessive frequency modulation excursion and can be eliminated by attenuating the input to the servo-control frequency modulation receiver by means of the variable resistance 92 for example.

Fig. 3 shows the orientation of Figs. 4 through 7 which are Sheets 3 through 6 of the drawings required to yield a detailed circuit diagram of the monitor branch circuit and associated switching equipment.

The circuit diagram which includes Figs. 4 through 7 is that of a two-channel working model of a delay equalization circuit which was actually constructed and successfully operated. As in Fig. 2 it will be assumed that channel A is being monitored and equalized. The through circuit connections for channels A and B are indicated at the left-hand side of Fig. 6 of the drawings at the coaxial input leads 100—100¹ and 101—101¹, respectively. The constant impedance variable phase delay equalizing networks 31 and 32 are shown inside dotted boxes and will be described in greater detail hereinafter in conjunction with Fig. 8. As an aid to understanding the detailed circuit diagram the signal circuit is indicated by a heavy line which shows the local signal circuit loop 102, and follows in a general way the path of the signal containing the distortion products through the monitor circuit. The timing motor 103, which may for example make one revolution every four minutes, has the brushes on its switching mechanisms 104, 105 and 106 on the commutator segment corresponding to channel A. The switch 106 controls the relays 107 and 108 which select the proper intermediate frequency channel.

With switch 106 closing the circuit to relay 107, channel A is connected through the cathode follower tube V-1 to the bus 110. This bus 110 leads to both the incremental slope alternator including the tube V-3 and to the servo-control conventional FM receiver which is not shown in this circuit.

The incremental slope alternator changes in impedance as the tube V-3 is switched on and off. This yields a variable increment of delay slope which is alternately positive and negative depending on the conduction of the tube. The delay distortion variation is accomplished by varying the resistance mismatch at the end of the reactive network which is made up of inductor 121, resistor 122 and the condenser 123. When the tube V-3 is non-conducting, it is out of the circuit and the termination is merely the resistor 124. When the tube is conducting, however, the apparent resistance at the end of the reactive network is much reduced by the cathode follower properties of the tube V-3. With the input impedance to the reactive network at the coaxial line 125 being 76 ohms the network constants of the incremental slope alternator are selected to be higher and lower than this 76 ohm value depending on whether the tube is conducting or not. The constants of the coaxial line 70 between the relay 107 and the incremental slope alternator are moderately critical; it has an impedance of 76 ohms, a dielectric constant of 2.25, and a length of about 8 feet. A representative set of values for the network elements is as follows:

The variable inductance 121 has a range between .4 and .7 microhenry, the resistance 122 has a value of 150 ohms, the condenser 123 has a value of 15 micromicrofarads, the resistance 124 has a value of 590 ohms and the condenser 126 may have a value of .001 microfarad. The phase delay slope produced by the incremental slope alternator adds to that already present in channel A and thus varies the distortion and the distortion products at a predetermined rate.

This rate is determined by the frequency of the oscillator which includes the twin-triode V-4. This is a conventional 15 cycle push-pull oscillator which has a tuned circuit made up of the inductance 131 and the condenser 132. The output from this oscillator is coupled to the grid of the tube V-3 in the incremental slope alternator, and controls its conduction. Although the oscillator output is sinusoidal, its amplitude is so great that the tube V-3 is either saturated or cut off at any particular instant and thus undergoes sudden shifts in conduction and consequent abrupt changes in incremental delay slope. Another output lead from the 15 cycle oscillator is coupled to the phase detector as will be discussed in greater detail hereinafter.

It is again noted that the intermediate frequency signal of channel A is coupled to the bus 110 by means of the cathode follower tube V-1 so that there will be no reaction back into the through signal circuit loop 102 from the incremental slope alternator in the monitor branch circuit. The bus 110 which carries signal from channel A, as modified by the incremental slope alternator, is connected to the servo-control frequency modulation receiver by the coaxial lead 112 which may be observed in the lower right-hand corner of Fig. 6. This frequency modulation receiver is not shown inasmuch as it is a standard commercial item of electrical equipment. The output from the servo-control frequency modulation receiver is coupled to the 2.8 megacycle amplifier including the vacuum tube V-3 by the coaxial input lead 113 which appears at the left-hand side of Fig. 4. From the output of the 2.8 megacycle amplifier the signal is connected to the demodulator stage including the tube V-6 where the 15 cycle amplitude modulated distortion products are detected. These 15 cycle distortion products are amplified in the stage including the tube V-7. This stage is effectively tuned to 15 cycles by means of the negative feedback bridge circuit 131. By having nega-

tive feedback cutting down the output of the tube V-7 at all frequencies except 15 cycles, the tube gain is peaked at this 15 cycle frequency. The limiter stage, including the diodes 132 and 133, is designed to prevent overloading of the phase detector stage, which might otherwise result from changes in volume of the input signal. The phase detection stage includes the two pentodes V-8 and V-9. The output from the limiter is coupled in push-pull to the two tubes of the phase detector by means of the transformer 136. The output from the 15 cycle oscillator is, however, coupled to the two tubes of the phase detector in parallel. Thus the 15 cycle signal from the distortion products will reinforce the signal from the 15 cycle oscillator in one of the phase detector tubes and will buck it in the other tube. This will cause an unbalanced current to flow through the two tubes and will cause direct current to flow through the polarized relay 136. Thus if the delay distortion has a positive slope, the polarized relay will be actuated in one direction, designated the positive direction, and if it has a negative slope, the polarized relay will be actuated in the negative direction. This effect will be used to vary the delay equalizer network in the proper sense to correct the distortion in the transmission line. When this distortion is corrected there will be no 15 cycle signals from the distortion products, the phase detector will be balanced, and the polarized relay will seek a neutral position.

Assuming the presence of delay slope distortion in channel A, the polarized relay 136 will make contact with one of the two contacts 137 and 138. These contacts are protected by the usual resistance-capacitance networks 139 and 140. Assuming that contact 137 is closed by relay 136, the lead 141 will be grounded. This lead 141 leaves Fig. 5 in the lower right-hand corner and enters Fig. 7 in the upper right-hand corner. It is connected to the rotating brush of the switch 105 which in turn is contacting the upper commutator segment which represents channel A. This commutator segment is connected to one of the two shading coils 143 and 144 of motor 145. This motor 145 also appears in Fig. 6 in equalizer 31 associated with channel A. When both ends of the shaded coil 143 are grounded, the reversible motor 145 will rotate in one direction. Assuming positive delay slope at the input to the monitor circuit, this direction of rotation may be termed positive. This will in turn make the slope of the equalizing network 31 more negative to compensate for the positive delay slope introduced by the transmission line. When the combined slope of transmission line and equalizer is negative, the relay 136 contacts the opposite terminal 138 and grounds the line 142 which is connected to the switch 104. This in turn grounds both ends of the shading coil 144 and causes the motor 145 to rotate in the negative direction. This, of course, changes the slope of the equalizer network 31 to a more positive value and again compensates for the delay slope distortion. The limit switches 147 and 148 prevent over-running of the motor 145 and light up the warning lights 149 and 150 when they are actuated. The switches 151 and 152 permit manual operation of the motor 145 for test and adjustment purposes.

The delay equalization correction of a channel may be accomplished in a relatively short time, normally less than one-half a minute. After such a period has elapsed the timing motor 103 will move the commutator brushes of the switches 104, 105 and 106 around to the next channel. In the present example, when the brushes contact the commutator segment corresponding to channel B, the relay 198 in the lower right-hand corner of Fig. 6 will be energized and channel B will then be connected to the monitor correction circuit. Depending on the sign of the delay distortion present in channel B, the polarized relay 136 will contact one of the contacts 137 or 138 and the motor 155 will be energized in the proper direction. This will in turn vary the delay equalizing network

32 in the proper sense, and the distortion will be equalized. During the periods of time when the monitor and the servo-circuits are disconnected from a particular channel, the equalizer for that channel remains stationary in the corrected position. Although the circuit diagram of Figs. 4 through 7 includes but two channels, a larger number of channels could readily be accommodated merely by suitable changes in the switching circuitry.

A critical group of circuits which form a portion of the system which has been described in Figs. 1 through 7 are the phase delay equalizers. These will now be considered in detail in conjunction with Figs. 8 through 12 and Figs. 14 through 17. The design of the equalizers was based on (1) the desired linear delay vs. frequency characteristic, and (2) the goal of constant impedance throughout the range of adjustment of the equalizers.

Fig. 8 represents a bridged-T envelope delay equalizer having the desired constant impedance. It is made up of a negative slope section 161, a positive slope section 162, and a fixed bulge section 163. The negative slope section 161 is the network between the input terminals 171, 172 and the central terminal 173; the positive slope network 162 is between the center terminal 173 and the terminal 174; and the fixed bulge section 163 is located between the terminal 174 and the output terminals 175 and 176. In accordance with the invention it has been determined that either or both the frequency of peak delay and the maximum delay slope of the networks 161, 162 can be varied without introducing loss or mismatch, by simultaneously varying a capacitor and its conjugate inductor in such a manner that the relationship

$$\frac{L}{C} = R^2$$

is maintained constant, where R is the characteristic impedance of the input and output transmission lines.

The electrical characteristics of the composite equalizer network are developed in the plots of Figs. 9 through 12, and the physical mounting of the variable elements of the equalizer is illustrated in Figs. 14 through 17. Referring first to the plots, Figs. 9 and 10 are generalized characteristics of delay and delay slope, respectively, for a single network such as is shown at 161 or 162.

In Fig. 9, the ranges 161-1 and 162-1 represent one extreme delay slope adjustment of the variable reactance elements 181 and 182 of the negative delay slope equalizer section 161, and of the reactance elements 183 and 184 of the positive slope section 162 of Fig. 8. The positive slope of the composite plot 180-1 in Fig. 11 results from the steep positive slope of 162-1 as compared with the shallow slope of the negative characteristic indicated at 161-1. With the variable equalizer elements adjusted to their extreme negative delay slope position, however, the peak delay frequency of the networks has been shifted to such an extent that the slopes are indicated by the plots 161-2 and 162-2 in Fig. 9, and the composite slope is negative as indicated by plot 180-2 in Fig. 11. The intermediate plots of 180-3, 180-4 and 180-5 represent composite characteristic curves of the equalizing elements 161 and 162 with the variable reactance elements adjusted to various intermediate positions.

The curvature of the positive and negative delay characteristics of the plots 180 of Fig. 11 may be better understood by reference to Fig. 10 which plots delay slope vs. frequency over the same range covered by Fig. 9. This curvature is corrected by the fixed bulge section 163 which has the delay characteristic illustrated in Fig. 12. The dotted characteristics of Fig. 11 are the overall plots of the entire network of Fig. 8, while the solid line plots 180 do not include the fixed bulge section 163.

Figs. 14 through 17 illustrate the arrangement which was employed to maintain the required

$$\frac{L}{C} = R^2$$

relationship, as the reactive elements were varied. The variable condensers 182 and 184 are standard units and are ganged with their rotors mounted on a single control shaft 188. The inductance 181, which is paired with the condenser 182 in the negative slope network 161, is made up of two fixed series aiding pancake coils 201, 202, and a thin vane 203 of conducting material mounted on shaft 188 so that it may be rotated into the space between the coils. This type of variable inductance is described in greater detail in the copending application of W. J. Albersheim and W. F. Bodtman, Serial No. 251,973, filed October 18, 1951, now abandoned. The variable inductance 183 is of similar construction but has a conducting vane 204 of a somewhat different configuration. These vanes 203 and 204 are shaped to maintain the constant relationship of L/C for each of the equalizer sections 161 and 162 as the standard condenser rotors are turned.

The following table indicates the values and the ranges of values for the reactive components of the equalizer network of Fig. 8 which resulted in the series of equalization plots shown in Fig. 11. This particular equalizer was designed for a frequency modulated signal having a 70 megacycle carrier frequency and a bandwidth of approximately 20 megacycles. These values are merely representative of one specific operable version of the equalizer, and no limitation to these values or to this frequency range is intended.

Inductor 181.....	0.143 to 0.318 microhenry.
Condenser 182.....	32 to 120 micromicrofarads.
Inductor 183.....	0.16 to 0.305 microhenry.
Condenser 184.....	3 to 28 micromicrofarads.
Condenser 111.....	20 micromicrofarads.
Condensers 112, 113.....	Both equal to 55 micromicrofarads.
Inductor 114.....	0.274 microhenry.
Condenser 115.....	14.5 micromicrofarads.
Condensers 116, 117.....	Both equal to 50 micromicrofarads.
Inductor 118.....	0.073 microhenry.
Inductor 119.....	0.194 microhenry.
Condensers 120, 121.....	Both equal to 52 micromicrofarads.
Inductor 122.....	0.15 microhenry.
Condenser 123.....	50 micromicrofarads.

The amplitude equalizer 36 of Fig. 1, which is shown in detail in Fig. 13, is optional equipment and need not be used when each repeater station includes a variable delay slope equalizer as illustrated hereinbefore. However, when because of economy or other reasons variable delay slope equalizers are only used at every fifth or tenth repeater, for example, experience has shown that cumulative distortion may cause loss of modulation at high frequencies. With an intermediate frequency carrier of 70 megacycles and a 20 megacycle bandwidth for the frequency modulated signal, substantial loss of level of 8 and 9 megacycle pilot tones has been observed in a microwave system of the type illustrated in Fig. 1. Furthermore, this effect has been particularly noticeable where the delay slope distortion has been permitted to build up to a substantial level before equalization.

Detailed mathematical analysis reveals that an amplitude compensator immediately following the delay slope compensator and before limiting of the intermediate frequency signal will overcome the above-noted loss of modulation. In addition, where the slope of the delay equalizer is equal to g seconds delay per cycle, the required amplitude vs. frequency characteristic of the amplitude compensator should be approximately

$$A = A_0(1 + 0.125g^2D^4)$$

where A_0 is the amplitude at the carrier frequency and D is the frequency expressed as the difference in radians/

sec. from the carrier frequency. The dependence on the square of the delay slope of the required equalizer indicates why amplitude compensation is not required when the delay slope distortion is not allowed to build up to large values.

Specific values for the network of Fig. 13 will now be developed which correspond to specified operating conditions. When the automatic delay equalizer of Figs. 4 and 7 is operated to one of its extreme limits as indicated at 180-1 or 180-5 in Fig. 11, one of the two limit switches 147, 148 of Fig. 7 will be actuated as an indication of this situation. The limit switches may control signal lamps, 149, 150 as shown in Fig. 7, or certain additional automatic switching equipment. In any event, after this condition has persisted for a period of time, a network made up of a fixed delay equalizer plus the amplitude compensator of Fig. 13 is switched into the circuit. The fixed delay equalizer has a slope which may be positive or negative and is slightly less than twice as great as that indicated by the extreme plots 180-1 and 180-5 of Fig. 11. An overall delay slope range of nearly three times the maximum delay slope (about 0.75 millicycle per megacycle) of the variable equalizer is covered by the combination of the fixed and variable equalizers.

To provide amplitude compensation corresponding to the formula $A=A_0(1+0.125g^2D_4)$ the resonant frequencies of the two series tuned circuits 221, 223 and 223, 224 are tuned to 60 and 80 megacycles, which correspond to the opposite edges of the intermediate frequency band. In addition the 76 ohm impedance of the network is maintained by having the ratios of

$$\frac{L-221}{C-225} = \frac{L-224}{C-228} = \frac{L-226}{C-222} = \frac{L-227}{C-223}$$

equal to the square of 76 ohms. The specific values of the reactive elements in the network of Fig. 13 are as follows:

Inductors 221, 224-----	Both equal to .07 microhenry.
Capacitor 222-----	5.6 micromicrofarads.
Capacitor 223-----	10 micromicrofarads.
Capacitors 225, 228-----	Both equal to 121 micromicrofarads.
Inductor 226-----	0.0324 microhenry.
Inductor 227-----	0.058 microhenry.

With the attenuation through the network at the center frequency of 70 megacycles equal to 1 decibel, resistances 231 and 232 will be approximately equal to 4.3 ohms and resistance 233 will be equal to about 1,420 ohms.

Returning to Figs. 1 through 7, a brief review of various aspects of the invention is now in order. From a limited or relatively specific viewpoint the present invention involves a novel automatic variable phase delay distortion equalizer. From a broader aspect, however, the invention is applicable to the correction of other types of distortion in extended transmission systems through the use of incremental distortion units which produce positive and negative increments of the type of distortion which is to be corrected. Certain other specific types of distortion which could be equalized in accordance with these principles are the amplitude variations with frequency of a broadband transmission line, the correction of delay curvature in addition to the delay slope which was considered in detail on the present specification, and the frequency pulling of oscillators mismatched by long lines.

It is to be understood that the above-described arrangements are illustrative of the application of the principles of the invention. Numerous other arrangements such as the correction of distortion by nonlinear circuit elements varied by bias voltage instead of mechanical motion, may be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. In combination, an extended multi-channel trans-

mission system, an independently variable delay slope equalization network coupled to each of said channels, a common monitor circuit for a plurality of said channels including means for directly detecting phase delay distortion products and including means for indicating the sign of the slope of the delay versus frequency characteristic of each channel, means individual to each of said channels for appropriately varying the slope of said variable delay slope equalization networks in accordance with the indicated sign of the slope of the delay versus frequency characteristic, and means for periodically switching said common monitor circuit to each of said plurality of channels.

2. In combination, a transmission system containing substantial phase delay distortion, a variable phase delay slope equalizer coupled to said transmission system, a monitor branch circuit from said transmission system, means coupled to said branch circuit for alternatively adding distortion having a positive delay versus frequency slope and distortion having a negative delay versus frequency slope at a first frequency rate to the distortion of said transmission system as seen by said monitor circuit, circuitual means which is also coupled to said branch circuit and which is tuned to said fixed frequency for determining the sign of the delay versus frequency characteristic slope of said transmission system, and means responsive to the output from said circuitual means for varying said phase delay equalizer and thus minimizing distortion.

3. A constant impedance variable delay slope equalizer comprising a first circuit having a positive delay versus frequency characteristic slope and including a variable inductor and a variable capacitor having a first predetermined ratio of inductance to capacitance, a second circuit coupled to said first circuit, said second circuit having a negative delay versus frequency characteristic slope and also including a variable inductor and a variable capacitor having a second predetermined ratio of inductance to capacitance, and means for synchronously varying said inductors and capacitors in said first and second circuits and concurrently maintaining said first and second predetermined ratios constant.

4. A constant impedance variable delay slope equalizer comprising a first circuit having a positive delay versus frequency characteristic slope and including a first variable inductor and a first variable capacitor having a first predetermined ratio of inductance to capacitance, a second circuit coupled to said first circuit, said second circuit having a negative delay versus frequency characteristic slope and including a second variable inductor and a second variable capacitor having a second predetermined ratio of inductance to capacitance, means for synchronously varying said first and second inductors and capacitors and concurrently maintaining said first and second predetermined ratios constant, and a third circuit coupled to said first and second circuits, said third circuit having a curved delay versus frequency characteristic for compensating for the curvature of the characteristics of said first and second circuits.

5. A constant impedance variable delay slope equalizer comprising a first circuit having a positive delay versus frequency characteristic slope and including a first variable inductor and a first variable capacitor having a first predetermined ratio of inductance to capacitance, a second circuit coupled to said first circuit, said second circuit having a negative delay versus frequency characteristic slope and including a second variable inductor and a second variable capacitor having a second predetermined ratio of inductance to capacitance, said variable capacitors comprising conductive rotor and stator plates, said inductors comprising two series aiding flat pancake coils having a movable conducting vane therebetween, and means including a rotatable rod on which said rotor plates and said conducting vanes are mounted for synchronously varying said first and second inductors and capacitors and concurrently maintaining said first and second predetermined ratios at a constant value.

6. In combination, an extended multichannel transmission system; a constant impedance variable delay slope equalizer coupled to each of the channels of said transmission system, each of said equalizers comprising a first circuit having a positive delay versus frequency characteristic slope and including a variable inductor and a variable capacitor having a first predetermined ratio of inductance to capacitance, a second circuit coupled to said first circuit, said circuit having a negative delay versus frequency characteristic slope and also including a variable inductor and a variable capacitor having a second predetermined ratio of inductance to capacitance, said variable capacitors comprising conductive rotor and stator plates, said inductors comprising two series aiding flat pancake coils having a movable conducting vane therebetween, and means including a rotatable rod on which said rotor plates and said conducting vanes are mounted for synchronously varying said inductors and capacitors in said first and second circuits and concurrently maintaining said first and second predetermined ratios constant; a common monitor circuit for a plurality of said channels including means for directly detecting phase delay distortion products and including means for indicating the sign of the slope of the delay versus frequency characteristic of each of said channels, and means responsive to the indicated sign of the delay versus frequency characteristic for rotating said rod in the appropriate direction to reduce the slope of the delay versus frequency characteristic of a transmission channel and its associated equalizer.

7. In combination, a frequency modulation transmission system containing substantial phase delay distortion; a variable delay slope equalizer coupled to said transmission system at a first point; a monitor branch circuit coupled to said transmission system at another point; said monitor circuit including means for sampling the equalized frequency modulated signals, means for alternately adding distortion having a positive delay versus frequency slope and distortion having a negative delay versus frequency slope at a predetermined frequency to the distortion of said transmission system as seen by said monitor circuit, circuital means tuned to said predetermined fre-

quency for determining the sign of the slope of the delay versus frequency characteristic of said equalized frequency modulated signals; and means responsive to the output from said circuital means for varying said delay equalizer to reduce the slope of the delay versus frequency characteristic of the circuit including the transmission system and the equalizer.

8. In combination, a multichannel signal transmission system containing substantial phase delay distortion; a constant impedance variable delay slope equalizer coupled to each of said channels; a common monitor branch circuit; said monitor circuit including means for sampling the equalized signals, means for alternately adding distortion having a positive delay versus frequency slope and distortion having a negative delay versus frequency slope at a predetermined frequency to the distortion of said transmission system as seen by said monitor circuit, and circuital means tuned to said predetermined frequency for determining the sign of the slope of the delay versus frequency characteristic of said equalized frequency modulated signals; means individual to each channel for varying the delay equalizer associated with the monitored channel and for reducing the slope of the delay versus frequency characteristic of the circuit including the transmission channel and the equalizer in response to the output from said circuital means; and means for periodically switching said common monitor circuit to each of said plurality of channels.

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